ISL6227EVAL2Z Dual Switcher Evaluation Board Setup Procedure

Application Note | July 14, 2008 | AN1068.1

This document describes the setup procedure for the ISL6227 Evaluation Board dual switcher implementation. For information about the DDR application, please refer to Application Note 1067, “ISL6227EVAL1 DDR Evaluation Board Setup Procedure.”

General Description

The ISL6227 can control two output voltages adjustable from 0.9V to 5.5V. The ISL6227 combines two synchronous PWM voltage regulators into a single IC. When the DDR pin is set to high, it transforms the IC into a complete dual switcher application. PWM1 and PWM2 output voltages are set by a simple feedback voltage divider connected across the outputs to GND. The feedback voltage divider outputs are 0.9VDC, which are connected to the VSEN1 and VSEN2 pins.

Automatic mode selection of constant-frequency synchronous rectification at heavy load, and hysteretic diode-emulation at light load, assure high efficiency over a wide range of conditions. The hysteretic mode of operation can be disabled separately on each PWM converter if constant-frequency continuous-conduction operation is desired for all load levels. The mode selection is achieved through the VOUT1 and VOUT2 pin connection. When VOUTx connects to GND, it forces Continuous Current Mode (CCM) operation. When they are connected to their respective outputs, it commands auto mode. Efficiency is further enhanced by using the lower MOSFET $r_{DS(ON)}$ as the current sense element.

Voltage-feed-forward ramp modulation (VIN pin), current mode control, and internal feedback compensation provide fast response to input voltage and output load transients.

In dual switching power supply applications, the ISL6227 monitors the output voltage of both CH1 and CH2 by comparing VSEN pin voltage to internal references. An independent PGOOD (power good) signal is asserted for each channel after its soft-start sequence has completed, and the output voltage is within -11%/+15% of the set point. The soft-start time can be adjusted through the selection of soft-start capacitors.

VSEN pin voltage is also used for overvoltage and undervoltage protections. The overvoltage protection prevents the output from going above 115% of the set point by holding the lower MOSFET on and the upper MOSFET off. When the output voltage decays below the overvoltage threshold, normal operation automatically resumes. Once the soft-start sequence has completed, undervoltage protection will latch the channel off if the output drops below 75% of its set point value in case of a short circuit.

Adjustable overcurrent protection (OCP) monitors the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET. The overcurrent protection threshold level can be adjusted by the resistor from OCSET pin to ground. The current sensing gain can be adjusted through the ISEN pin resistor. If more precise current-sensing is required, an external current sense resistor may be used.

Features

- Provides regulated output voltage in the range of 0.9V to 5.5V
  - High efficiency over wide load range
  - Synchronous buck converter with hysteretic operation at light load
  - Inhibit hysteretic mode on one, or both channels
- Uses MOSFET $r_{DS(ON)}$ for current sensing or uses current-sense resistor for precision overcurrent protection
- Overvoltage, undervoltage and overcurrent protection on both channels
- Undervoltage lock-out on VCC pin
- Dual input voltage mode operation
  - Operates directly from battery 5V to 24V input
  - Operates from 3.3V or 5V system rail
- Excellent dynamic response
  - Combined voltage feed-forward and current mode control
- Power-good signal for each channel
- 300kHz switching frequency
  - 180° channel-to-channel phase shift operation
- Pb-free available (RoHS compliant)

Ordering Information

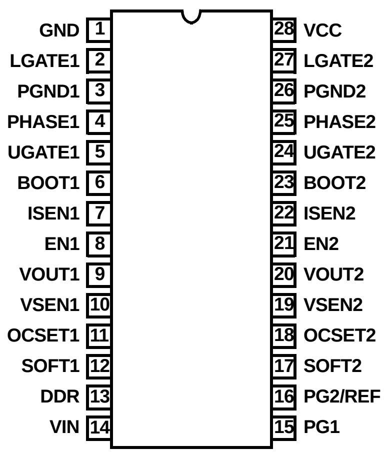
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6227CA*	ISL 6227CA	-10 to +100	28 Ld QSOP	M28.15
ISL6227CAZ* (Note)	ISL 6227CAZ	-10 to +100	28 Ld QSOP (Pb-free)	M28.15
ISL6227IA*	ISL 6227IA	-40 to +100	28 Ld QSOP	M28.15
ISL6227IAZ* (Note)	ISL 6227IAZ	-40 to +100	28 Ld QSOP (Pb-free)	M28.15
ISL6227IRZ* (Note)	ISL 6227IRZ	-10 to +100	28 Ld QFN (Pb-free)	L28.5x5
ISL6227HRZ* (Note)	ISL 6227HRZ	-10 to +100	28 Ld QFN (Pb-free)	L28.5x5
ISL6227EVAL2Z	Evaluation Platform			

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

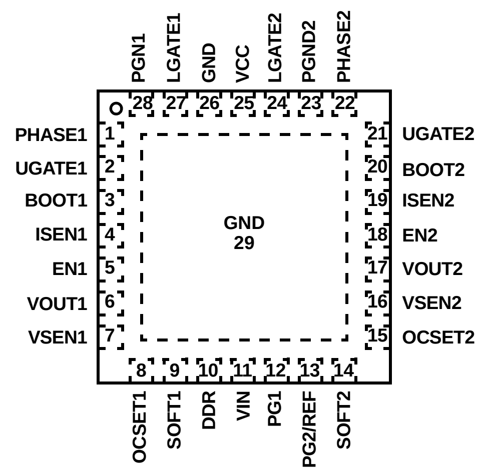
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL6227
(28 LD QSOP)
TOP VIEW



ISL6227
(28 LD QFN)
TOP VIEW



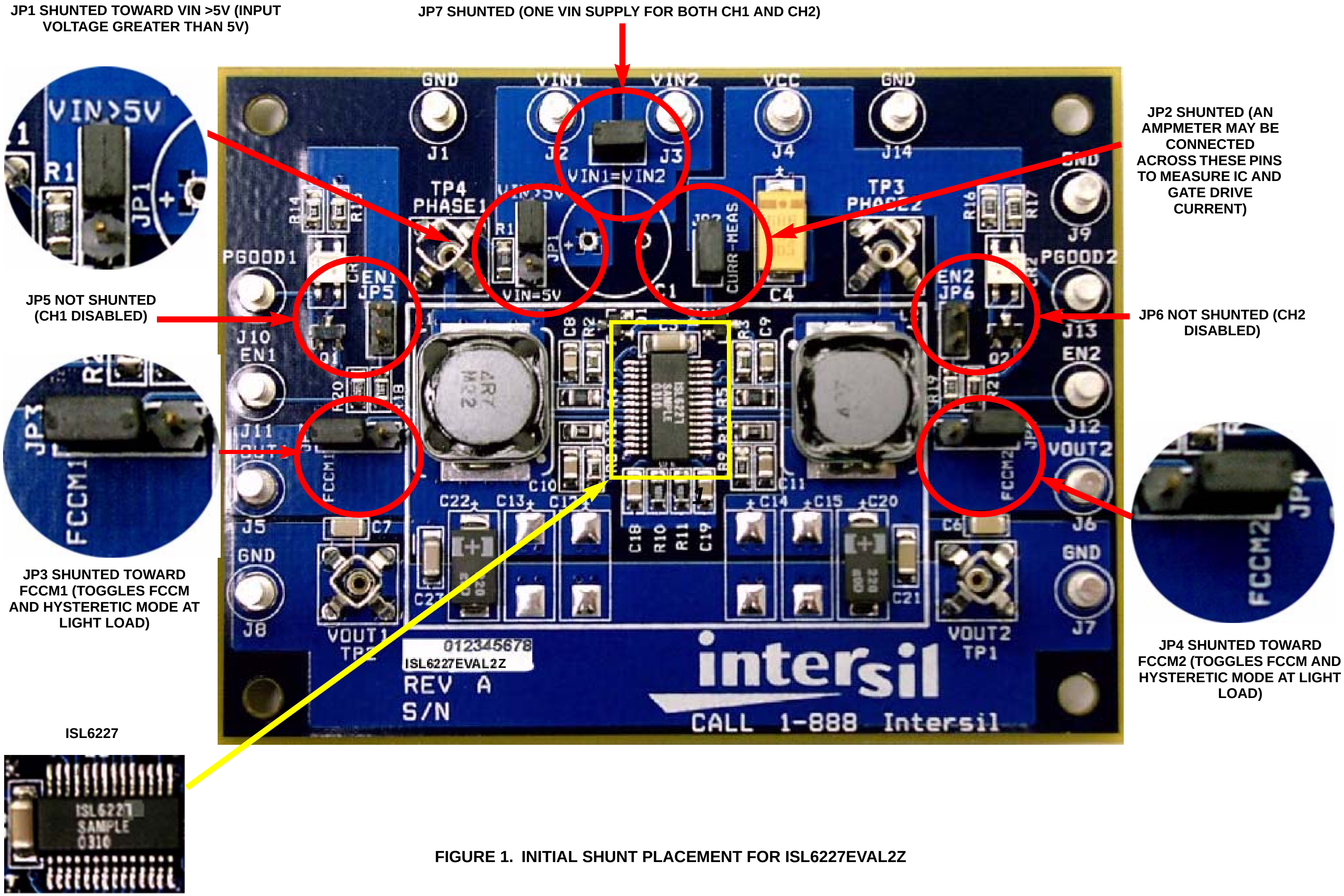


FIGURE 1. INITIAL SHUNT PLACEMENT FOR ISL6227EVAL2Z

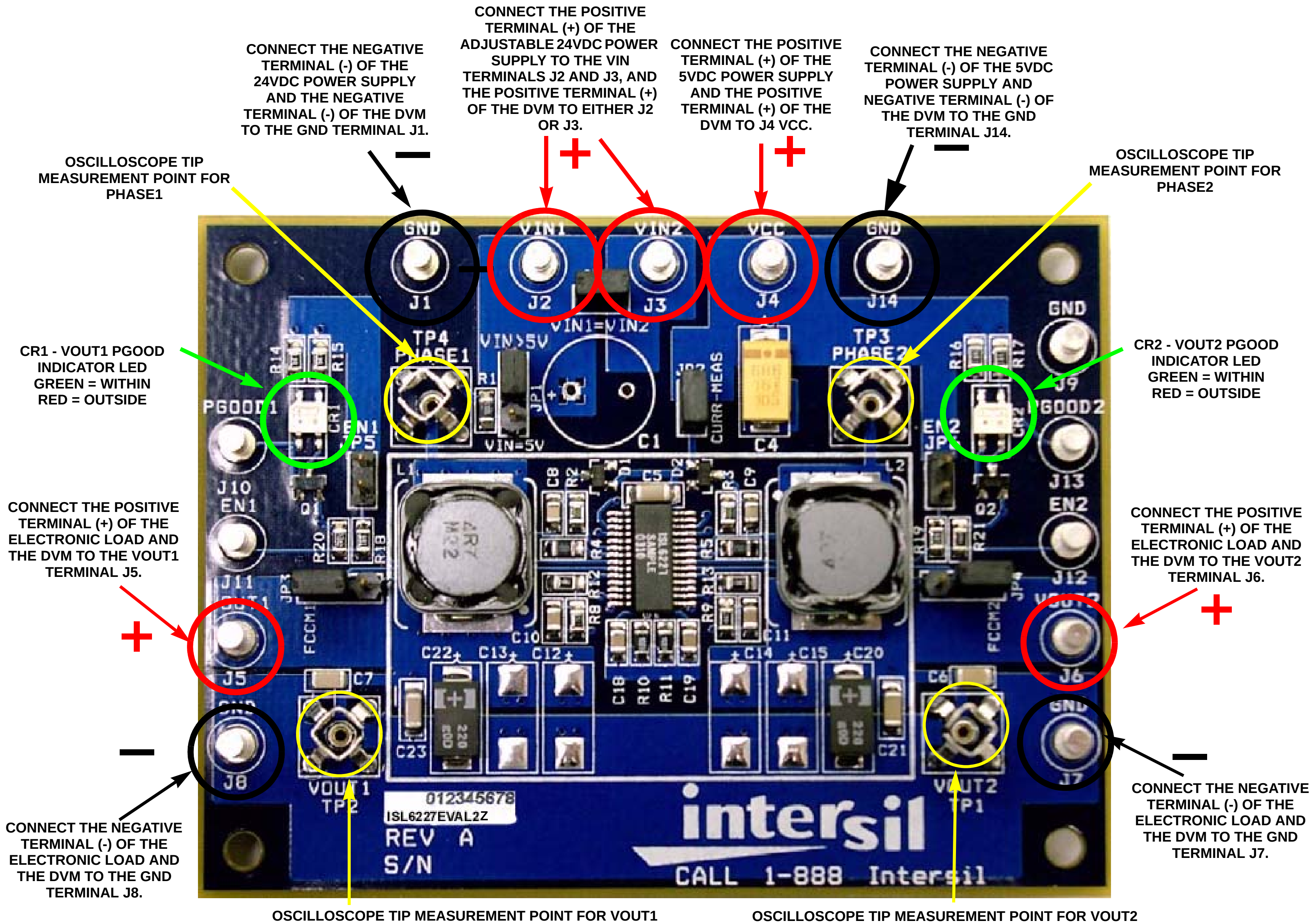


FIGURE 2. WIRING CONNECTIONS FOR ISL6227EVAL2Z

What's Inside

This Evaluation Board Kit contains the following materials:

- the ISL6227EVAL2Z Evaluation Board
- the ISL6227EVAL2Z Evaluation Board Setup Procedure

What is Needed

The following items will be needed to perform a complete evaluation:

- 4 channel oscilloscope with probes
- 2 electronic loads
- 2 laboratory power supplies
- Precision digital multi-meters
- Digital pulse generator

TABLE 1. JUMPER SETTINGS

JUMPER	POSITION	FUNCTION
JP1	*VIN >5V	*Input Voltage greater than 5V
	VIN = 5V	Input Voltage 3.3V to 5.0 Volt operation
JP2	*Shunted	*An AmpMeter may be connected across these pins to measure IC and GATE Drive Current only
JP3	*FCCM1	*Channel 1 Fixed Continuous Conduction Mode
	Away from FCCM1	Channel 1 Hysteretic Operation enabled
JP4	*FCCM2	*Channel 2 Fixed Continuous Conduction Mode
	Away from FCCM2	Channel 2 Hysteretic Operation enabled
JP5	Shunted	Channel 1 enabled
	*Removed	*Channel 1 disabled
JP6	Shunted	Channel 2 enabled
	*Removed	*Channel 2 disabled
JP7	*Shunted	*One VIN supply for both CH1 and CH2
	Removed	Separate VIN supplies for CH1 and CH2

NOTE: * = initial setting

TABLE 2. LED CONDITION INDICATORS

LED CONDITION	CONDITION	RESULT
CR1	green	VOUT1 WITHIN PGOOD RANGE
	red	VOUT1 OUTSIDE PGOOD RANGE
CR2	green	VOUT2 WITHIN PGOOD RANGE
	red	VOUT1 OUTSIDE PGOOD RANGE

Quick Setup

- The VIN Power Supply must always be the first supply on and the last supply off.
- The 5V V_{CC} Power Supply must be within 5V ± 5%.
- Make sure the power is off before moving any jumpers, except EN1 and EN2.
- Better connect/disconnect probes without powering circuit
- Make sure the electronic loads are set at 0A condition before the connection.

Step 1: Connect power supply and measurement equipment

1a. Connect VCC power supply

- Set the output voltage of the 5V adjustable power supply to zero volts. Connect the positive terminal (+) of the power supply to the VCC terminal J4. Connect the negative terminal (-) of the 5VDC power supply to the GND terminal J14.

1b. Connect VCC measurement equipment

- Connect the positive terminal (+) of a DVM to the VCC terminal J4. Connect the negative terminal (-) of the DVM to the GND terminal J14.

- **Do not apply power yet**

1c. Connect VIN power supply

- Set the adjustable 24VDC output voltage to zero volts. Connect the positive terminal (+) of the power supply to the VIN terminals J2 and J3. Connect the negative terminal (-) of the 24VDC power supply to the GND terminal J1.

1d. Connect VIN measurement equipment

- Connect the positive terminal (+) of a DVM to one of the VIN terminals J2 or J3. Connect the negative terminal
(-) of the DVM to the GND terminal J1.

- **Do not apply power yet**

Step 2: Connect load and measurement equipment

2a. Connect load for Channel 1 and measurement equipment

- Connect the positive terminal (+) of the electronic load and the DVM to the VOUT1 terminal J5. Connect the negative terminal (-) of the electronic load and the DVM to the GND terminal J8. The electronic load should be at 0A load condition.

2b. Connect load for Channel 2 and measurement equipment

- Connect the positive terminal (+) of the electronic load and the DVM to the VOUT2 terminal J6. Connect the negative terminal (-) of the electronic load and the DVM to the GND terminal J7. The electronic load should be at 0A condition.

Step 3: Set control jumper as illustrated in Table 1 on page 5.

Step 4: Power up the EVAL board

4a. Take the adjustable 24VDC power supply that is connected to the VIN terminals J2 and/or J3 and make sure the output voltage is set to zero volts.

4b. Turn on the 24VDC power supply.

4c. While reading the DVM, increase the output voltage of the 24VDC power supply to 5.0 VDC.

4d. Turn on the 5V VCC power supply.

4e. While reading the DVM, increase the output voltage of the 5VDC power supply to 5VDC.

4f. The LED on both channels should be Red.

Step 5: Take initial measurements
(The LED should become red at this point)

5a. Install the EN1 shunt jumper JP5.

5b. This should bring the LED of CR1 to Green

5c. Install the EN2 shunt jumper JP6.

-This would bring the LED of CR2 to Green.

NOTE: Terminals J1 (EN1) and J12 (EN2) may be connected to a pulse generator for controlled on/off operation and may be observed with an oscilloscope. The magnitude of the enable signal must be less than VCC voltage, 5V.

5d. Read the DVM connected to the VOUT1 terminal J5. VOUT1 voltage should be within 2.45V to 2.55V (2.5V ±2%).

5e. Read the DVM connected to the VOUT2 terminal J6. The voltage reading should within 1.764V to 1.836V (1.8V ±2%).

Step 6: Vary operating conditions

6a. The 24V VIN Power Supply may be adjusted between 5VDC to 24 VDC.

-The electronic load can be adjusted between 0A to 5A to check the output regulation.

6b. If Hysteretic operation is desired, move jumper J3 for Channel 1 PWM or JP4 for channel 2 PWM, to the position opposite the silk screen “FCCM”.

Step 7: Power off

7a. Turn off the VCC power supply

7b. Turn off the VIN power supply

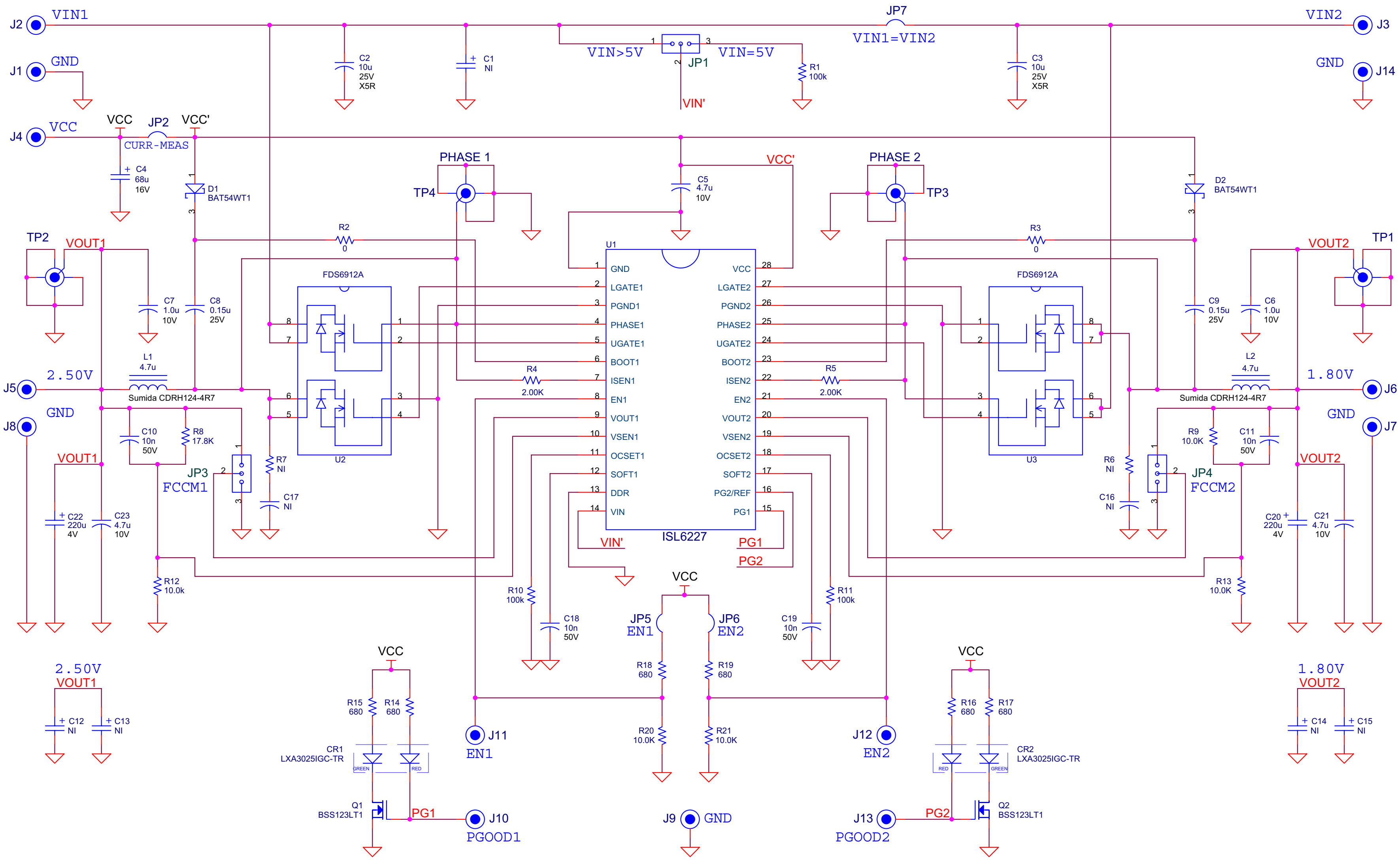


FIGURE 3. ISL6227EVAL2Z SCHEMATIC

intersil

TABLE 3. BILL OF MATERIALS (BOM)

QTY	REFERENCE	DESCRIPTION	VENDOR	PART NO.
1		PWB-PCB, ISL6227EVAL2Z	Intersil	ISL6227EVAL2ZREVBPCB
1	C1	CAP, RADIAL, 220µF, 25V, 20%, ALUM, ELEC	Panasonic	EEU-FC1E221
4	C10, C11, C18, C19	CAPACITOR, SMD, 0805, 0.01µF, 50V, 10%, X7R	Panasonic	ECJ-2VB1H103K
2	C2, C3	CAPACITOR, SMD, 1812, 10µF, 25V, 20%, X5R	Taiyo Yuden	TMK432BJ106MM
2	C20, C22	CAP TANT, LOW ESR, SMD, D2, 220µF, 4V, 20%	Sanyo	4TPC220M
1	C4	CAP TANT, LOW ESR, SMD, D, 68µF, 16V, 10%	Kemet	T494D686K016AS
3	C5, C21, C23	CAPACITOR, SMD,1206, 4.7µF, 10V, 10%, X7R	Venkel	C1206X7R100475KNE
2	C6, C7	CAPACITOR, SMD, 1206, 1µF, 10V, 10%, X7R	Kemet	C1206C105K8RAC
2	C8, C9	CAPACITOR, SMD, 0805, 0.15µF, 25V, 10%, X7R	Panasonic	ECJ-2YB1E154K
2	CR1, CR2	LED, SMD, 3x2.5mm, 4P, RED/GRN,12/20MCD, 2V	Lumex	SSL-LXA3025IGC-TR
2	D1, D2	DIODE-SCHOTTKY, SMD, SOT323, 3P, 30V, 0.2A	ON-Semiconductor	BAT54WT1-T
14	J1-J14	CONN-GEN, TERMINAL POST, TH, 0.09 INSERTION	Keystone	1502-2
3	JP1, JP3, JP4	HEADER, 1x3, BREAKAWAY, 1X36, 2.54mm, ST	Berg/FCI	68000-236-1X3
7	JP1-JP7	JUMPER, 2PIN, SHUNT	Sullens	SPC02SYAN
4	JP2, JP5-JP7	HEADER, 1x2, RETENTIVE, 2.54mm, ST	Berg/FCI	69190-202
2	L1, L2	COIL-PWR INDUCTOR, SMD, 12mm, 4.7µH, 20%, 5.7	Sumida	CDRH124-4R7MC
2	Q1, Q2	TRANSISTOR, N-CHANNEL, 3P, SOT23, 100V, 0.17A	ON-Semiconductor	BSS123LT1-T
3	R1, R10, R11	RESISTOR, SMD, 0805, 100k, 1/10W, 1%, TF	Panasonic	ERJ-6ENF1003V
6	R14-R19	RESISTOR, SMD, 0805, 680Ω, 1/10W, 5%, TF	Panasonic	ERJ-6GEYJ681V
2	R2, R3	RESISTOR, SMD, 0805, 0Ω, 1/10W, TF	Panasonic	ERJ-6GEY0R00V
2	R4, R5	RESISTOR, SMD, 0805, 2k, 1/10W, 1%, TF	Panasonic	ERJ-6ENF2001V
1	R8	RESISTOR, SMD, 0805, 17.8k, 1/10W, 1%, TF	Panasonic	ERJ-6ENF1782V
5	R9, R12, R13, R20, R21	RESISTOR, SMD, 0805, 10k, 1/10W, 1%, TF	Panasonic	ERJ-6ENF1002V
4	TP1-TP4	TEST POINT, SCOPE PROBE, 0.135" DIA	Tektronix	131-4353-00
1	U1	IC, DUAL SWITCHER, 30V, 28PIN, QSOP, DDR OPTION	Intersil	ISL6227CA, ISL6227CAZ
2	U2, U3	MOSFET, DUAL, N-CHANNEL, Logic, 8P, SOIC, 30V, 6A	Fairchild	FDS6912A

ISL6227EVAL2Z Layout

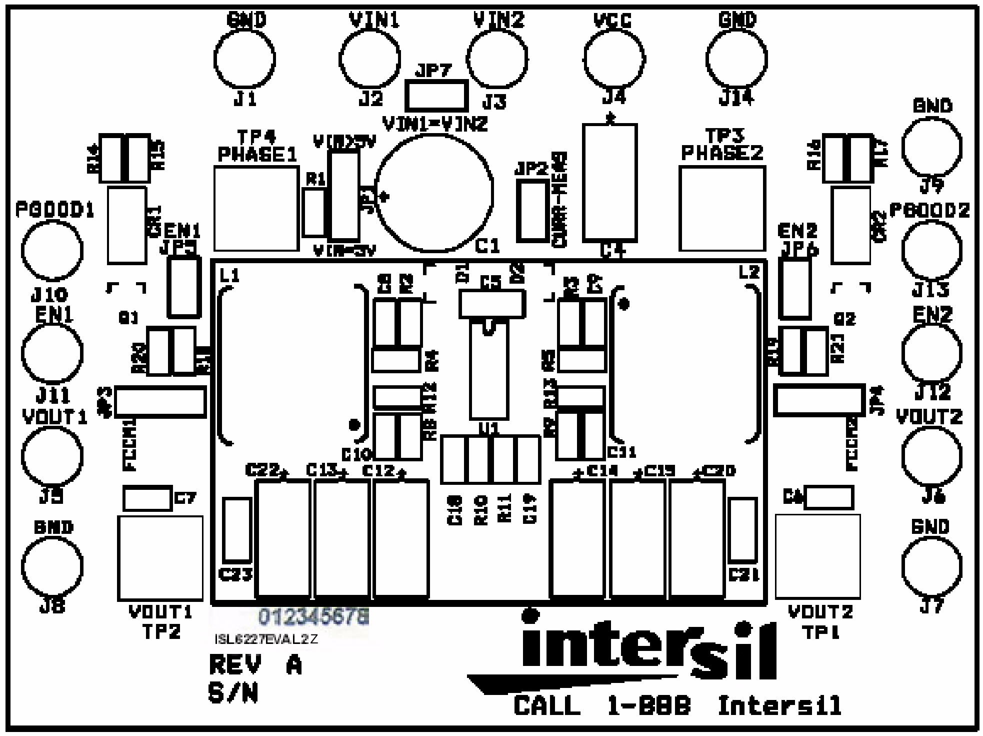


FIGURE 4. TOP SILK SCREEN

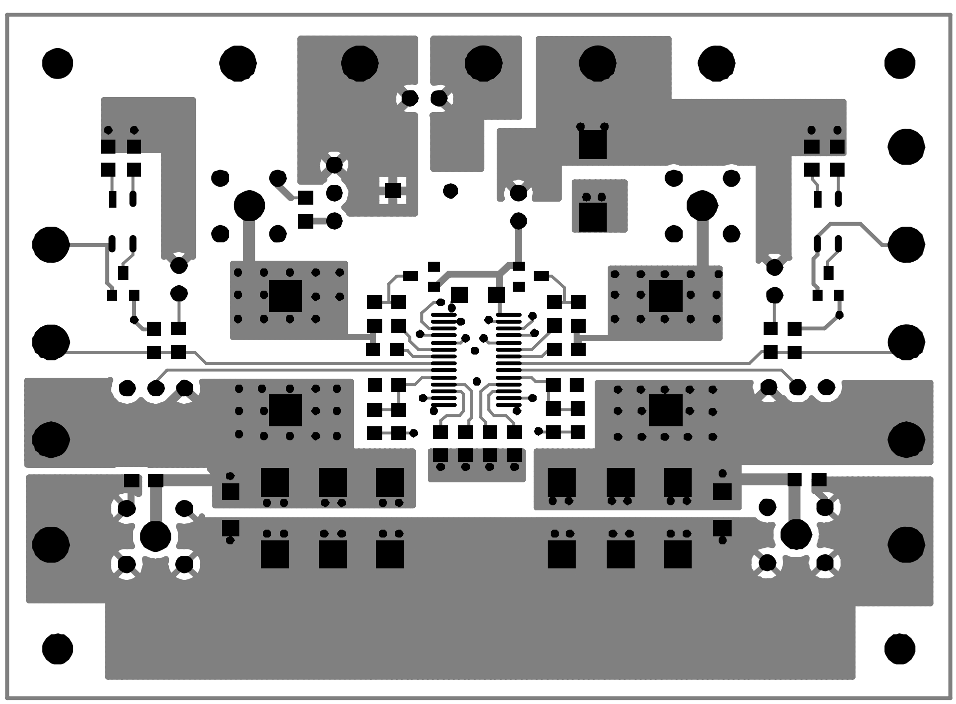


FIGURE 5. TOP LAYER

ISL6227EVAL2Z Layout (Continued)

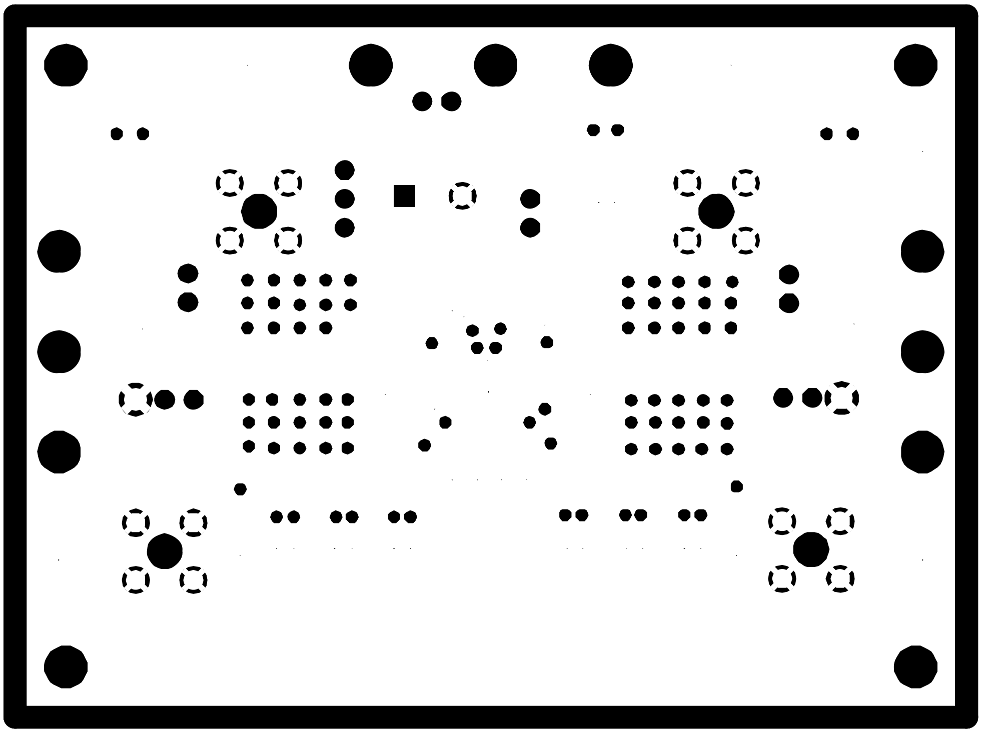


FIGURE 6. GND - INTERNAL 1

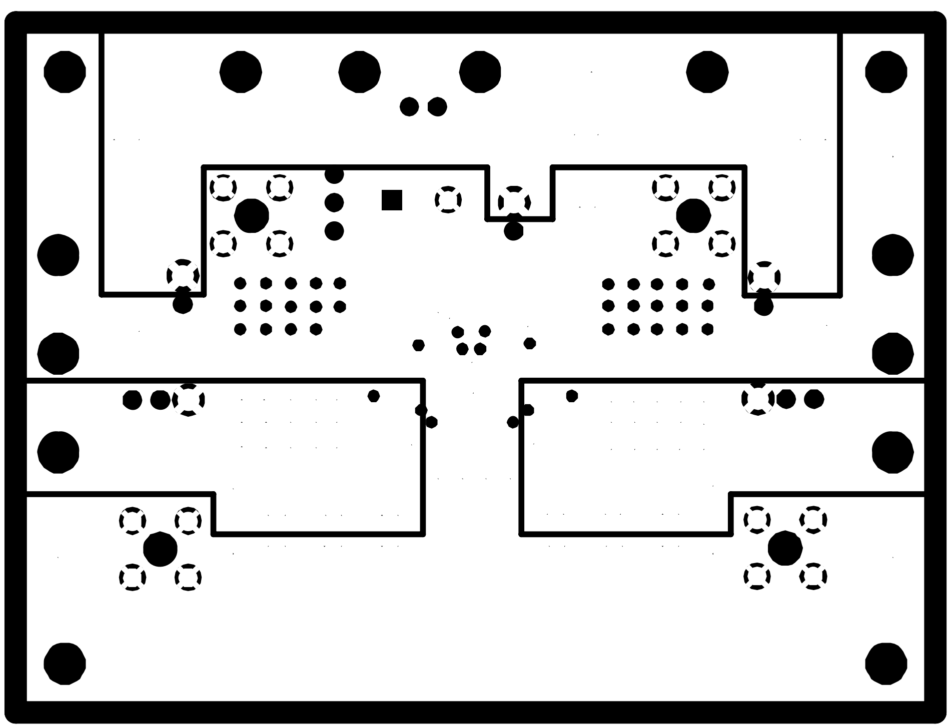


FIGURE 7. POWER - INTERNAL 2

ISL6227EVAL2Z Layout (Continued)

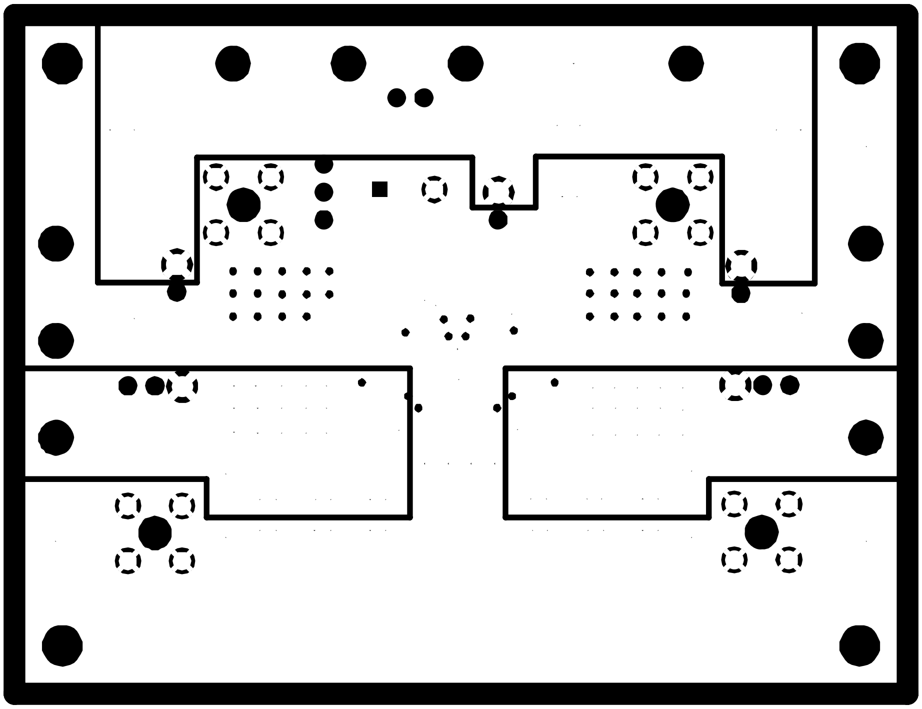


FIGURE 8. POWER - INTERNAL 3

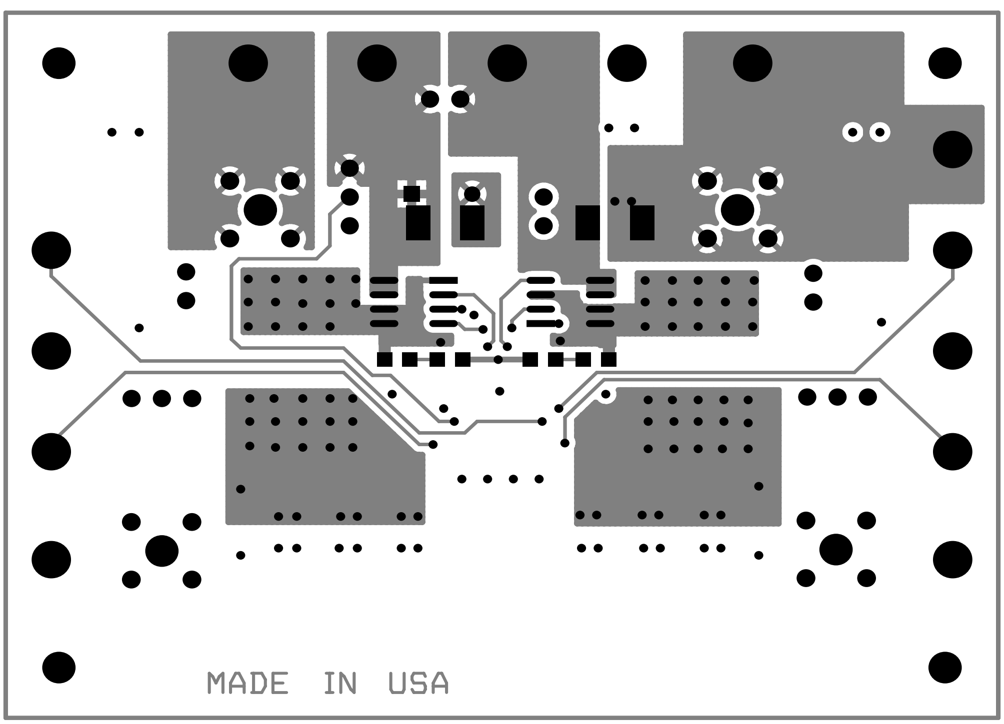


FIGURE 9. BOTTOM LAYER

ISL6227EVAL2Z Layout (Continued)

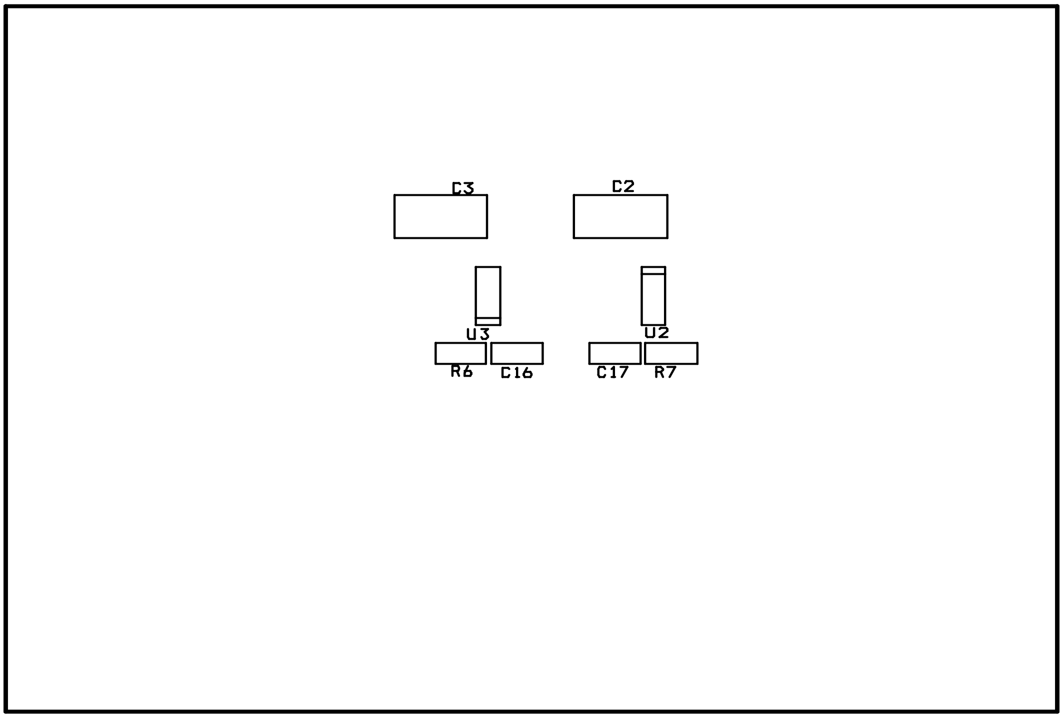


FIGURE 10. SILK SCREEN BOTTOM