Features

❑ Microcontroller: MLX16-FX RISC CPU

16bit RISC CPU with 20MIPS and Power-Saving-Modes
Co-processor for fast multiplication and division
Flash and NVRAM memory with ECC
In-circuit debug and emulation support

❑ Supported Bus Interfaces:

LIN interface with integrated LIN transceiver supporting LIN 2.x, certified LIN protocol software provided by Melexis
In-Module programming (Flash and NVRAM) via pin LIN using a special Melexis fast protocol
PWM interface

❑ Motor Controller

Patented algorithms for sensor-less 3-phase sine and trapezoidal motor control
Phase voltage integration filter for BEMF voltage sensing at lowest speeds
Position dependent phase inductance sensing via shunt current measurements at stand still and low to medium speeds
Support of Star and Delta based motor configurations without the need for center star point
Support of 3-phase switched reluctance motor control

❑ Voltage Regulator

Direct powered from 12V board net with low voltage detection
Operating voltage VS = 5V to 18V
Internal voltage regulator with possibility to use external regulator transistor
Very low standby current, < 50µA in sleep mode, wake-up possible via LIN or local sources

❑ Pre-Driver

Pre-driver (~27Ω Rdson) for 3 N-FET half bridges with programmable Inter-Lock-Delay and slope control for optimal EMC and thermal performance during N-FET switching
Monitoring of Drain-Source voltages of the N-FETs

❑ Periphery

Full duplex SPI, Master/Slave, double-buffered, programmable speed, DMA access.
Full duplex UART
4 independent 16 bit timer modules with capture and compare and additional software timer
3 programmable 12 bit PWM units with programmable frequencies
10 bit ADC converter (2µs conversion time) and DMA access
On-chip temperature sensor with ±10K accuracy
System-clock-independent fully integrated watchdog
40MHz clock from internal RC oscillator with PLL
Optional crystal oscillator
Load dump and brown out interrupt function
Integrated shunt current amplifier with programmable gain

Applications

The MLX81205/07 are designed to control BLDC motors via external FET transistors for applications like oil pumps, water pumps, fuel pumps, blowers, compressors, and positioning actuators.

Table of Contents

1. Family Overview and Ordering Information

	MLX81205	MLX81207
Flash Memory [kByte]	32	32
RAM [kByte]	4	4
NVRAM [Byte] [1]	4x128	4x128
Package	QFN32	QFN48 TQFP48
Support of active high side reverse polarity protection	No	Yes
Current shunt measurement possibility	High side	High side
SPI	No	Yes
UART	Yes	Yes
Number of general purpose IO pins	3	6
Support of sensor based BLDC motor control	No	Yes
Bonded pins in package	32	37
Pin compatibility		

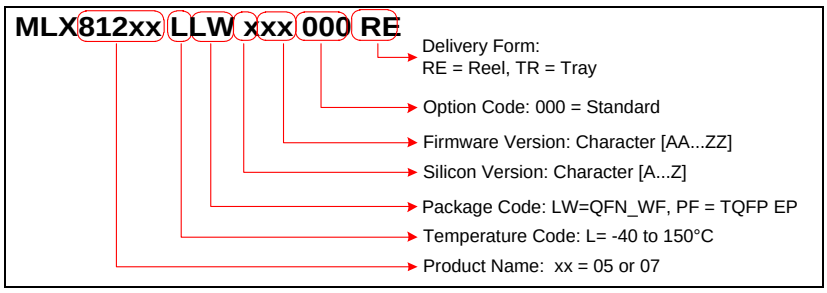
Table 1 – Family Overview

Order Code	Temperature Range	Package	Delivery	Remark
MLX81205 LLW-BAD-000-RE	-40 - 150 °C	QFN32_WF 5x5	Reel	QFN with wettable flanks
MLX81207 LLW-BAD-000-RE	-40 - 150 °C	QFN48_WF 7x7	Reel	QFN with wettable flanks
MLX81207 LPF-BAD-000-TR	-40 - 150 °C	TQFP EP 48 7x7	Tray	
MLX81207 LPF-BAD-000-RE	-40 - 150 °C	TQFP EP 48 7x7	Reel	

Table 2 – Ordering Information

[1] One page of 128 byte is only writable in test mode and reserved for Melexis calibration and test data

Legend:


MLX812xx LLW xxx 000 RE
Delivery Form:
RE = Reel, TR = Tray
Option Code: 000 = Standard
Firmware Version: Character [AA...ZZ]
Silicon Version: Character [A...Z]
Package Code: LW=QFN_WF, PF = TQFP EP
Temperature Code: L= -40 to 150°C
Product Name: xx = 05 or 07

2. Functional Diagram

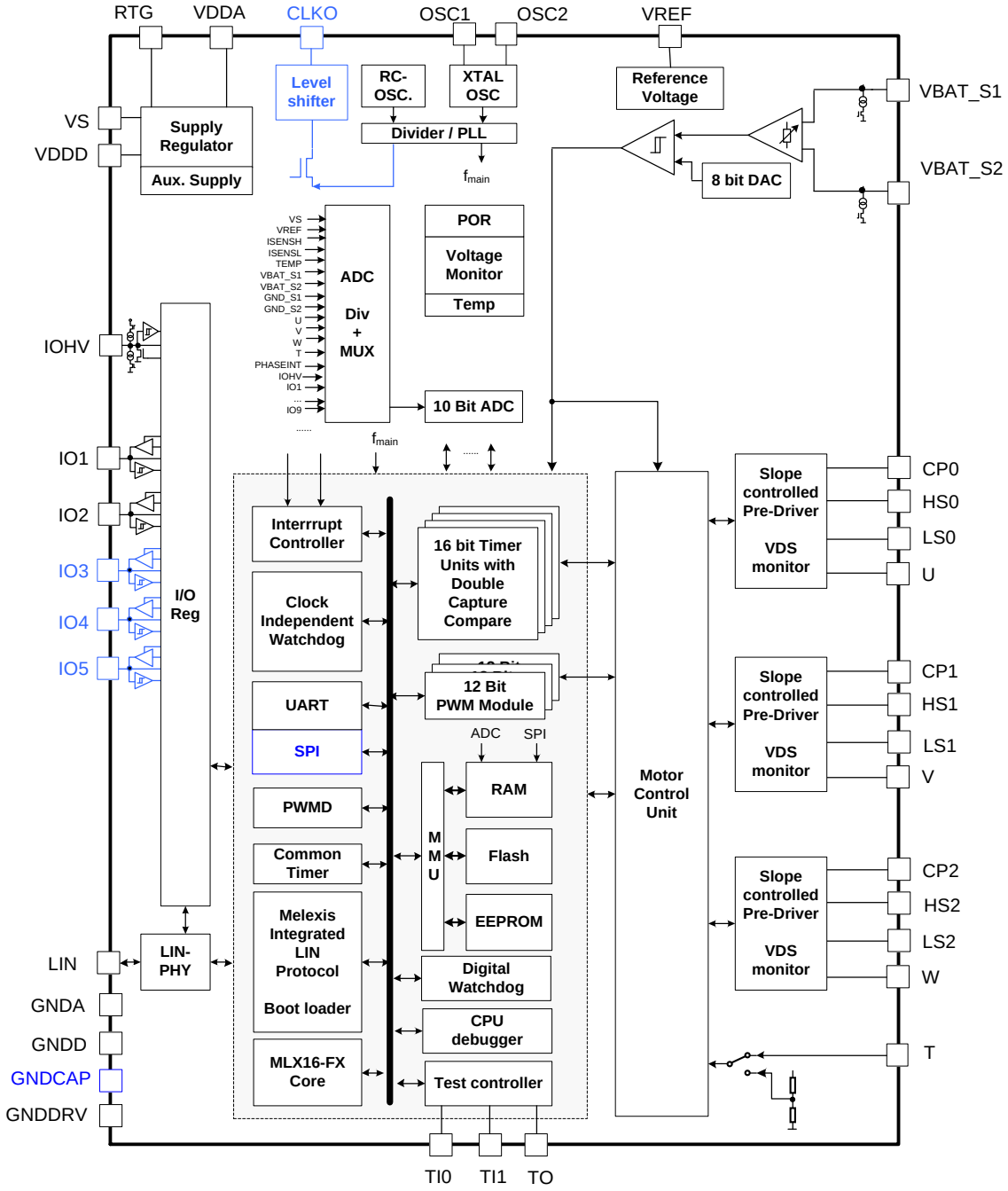


Figure 1 – Block Diagram

Colour legend:
Black: common for MLX81205 and MLX81207
Blue: additional pins or functionality for MLX81207

3. Pin Description

Name	Type	Function	MLX81205	MLX81207
VS	P	Battery Supply	X	X
RTG	O	3.3V External MOS Gate Control	X	X
VDDA	P	3.3V Supply	X	X
VDDD	P	1.8V Regulator output	X	X
GNDD	GND	Digital ground	X	X
GNDCAP	GND	Digital ground		X
GNDDRV	GND	Driver ground	X	X
GNDA	GND	Analogue ground	X	X
LIN	HVIO	Connection to LIN bus or PWM interface	X	X
IOHV	HVIO	General purpose IO pin	X	X
TI0	I	Test input, debug interface	X	X
TI1	I	Test input, debug interface	X	X
TO	O	Test output, debug interface	X	X
OSC1	I	Quartz interface input	X	X
OSC2	O	Quartz interface output	X	X
IO1	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO2	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO3	LVIO	General purpose IO pin (Low voltage 3.3V)		X
IO4	LVIO	General purpose IO pin (Low voltage 3.3V)		X
IO5	LVIO	General purpose IO pin (Low voltage 3.3V)		X
CLKO	HVO	Switch able 250kHz clock output to VREF level		X
T	HVI	Reference input to BEMF sensing blocks	X	X
VREF	P	Clamped 8V or 12V ref. voltage for bootstrap	X	X
CP2	HVIO	High side bootstrap capacitor driver 2	X	X
HS2	HVIO	N-FET high side gate driver 2	X	X
W	HVI	Phase W input to HS2 buffer and BEMF sensing blocks	X	X
LS2	HVO	N-FET low side gate driver 2	X	X
CP1	HVIO	High side bootstrap capacitor driver 1	X	X
HS1	HVIO	N-FET high side gate driver 1	X	X
V	HVI	Phase V input to HS1 buffer and BEMF sensing blocks	X	X
LS1	HVO	N-FET low side gate driver 1	X	X
CP0	HVIO	High side bootstrap capacitor driver 0	X	X
HS0	HVIO	N-FET high side gate driver 0	X	X
U	HVI	Phase U input to HS0 buffer and BEMF sensing blocks	X	X
LS0	HVO	N-FET low side gate driver 0	X	X
VBAT_S1	HVI	VS high side input for current sensing	X	X
VBAT_S2	HVI	VS low side input for current sensing	X	X
		Pin count	**32**	**37**

Table 3 – Pin Description MLX81205 / MLX81207

4. Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the MLX81205/07 is only specified within the limits shown in Table 4.

4.1 Operating Conditions

Parameter	Symbol	min	max	Unit
IC supply voltage	VS	5.0	18	V
Operating ambient temperature	Tamb	-40	+125 (+150) 2	°C

Table 4 – Operating Conditions

4.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	min	max	Unit
IC supply voltage on pins VS, VBAT_S1, VBAT_S2	VS	T = 2 min	-0.3	28	V
		T < 500 ms 3		45	
	VS.tr1	ISO 7637-2 pulse 1 4 VS=13.5V, TA=(23 ± 5)°C	-100		V
	VS.tr2	ISO 7637-2 pulse 2 4 VS=13.5V, TA=(23 ± 5)°C		+75	V
	VS.tr3	ISO 7637-2 pulses 3A, 3B 4 VS=13.5V, TA=(23 ± 5)°C	-150	+100	V
	VS.tr5	ISO 7637-2 pulses 5b 4 VS=13.5V, TA=(23 ± 5)°C	+65	+87	V
LIN Bus	VLIN	T<500ms	-25	40	V
	VLIN.tr1	ISO 7637-2 pulse 1 5 VS=13.5V, TA=(23 ± 5)°C	-100		
	VLIN.tr2	ISO 7637-2 pulse 2 5 VS=13.5V, TA=(23 ± 5)°C		+75	
	VLIN.tr3	ISO 7637-2 pulses 3A, 3B 6 VS=13.5V, TA=(23 ± 5)°C	-150	+100	
Maximum reverse current into any pin 7			-10	+10	mA
Maximum sum of reverse currents into all pins 7				+10	mA
DC voltage on LVIO pins, OSC<2:1>			-0.3	VDDA+0.3	V
DC voltage on pins HV I/O			-0.3	VS+0.3	V

2 With temperature applications at TA>125°C a reduction of chip internal power dissipation by using an external supply transistor is mandatory. The extended temperature range is only allowed for a limited period of time, a mission profile has to be agreed by Melexis as a mandatory part of the Part Submission Warrant (PSW)

3 Only allowed, if FET drivers are disabled, i.e. the high-side driver must not be stressed with V(CP) > 45V

4 ISO 7637 test pulses are applied to VS via a reverse polarity diode and >22µF blocking capacitor

5 ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF

6 ISO 7637 test pulses are applied to LIN via a coupling capacitance of 100pF

7 Excluding pins HS0, HS1, HS2, U, V, W, LS0, LS1, LS2.

Parameter	Symbol	Condition	min	max	Unit
DC voltage on drivers supply pin VREF			-0.3	18	V
DC voltage on pin CLKO			-0.3	VREF+0.3	V
DC voltage on drivers control pins LS<2:0>			-0.5 8	VREF+0.3	V
DC voltage on drivers pins CP<2:0>		Voltage on pins CP<2:0> must not exceed 45V.	-0.3	V<U,V,W> + 13	V
DC voltage on drivers pins HS<2:0>		Voltage on pins HS<2:0> must not exceed 45V	-0.5 9 10	VS + VREF	V
DC voltage on phases related pins U,V,W		Voltage on pins U,V,W must not exceed 36V	-0.5 9 10	VS+1.5	V
DC voltage on phases related pin T		Voltage on pin T must not exceed 36V	-0.3	VS+1.5	V
Positive dynamic disturbance on pin VBAT_S1 11	Vpdd	Spdd > 2 V/µs		4.5	V
ESD capability of pin LIN to GND	ESDBUSHB	Human body model 12	-6	+6	kV
ESD capability of pin VS to GND	ESDVSHB	Human body model 12	-4	+4	kV
ESD capability of any other pins	ESDHB	Human body model 12	-2	+2	kV
ESD capability ay any pin	ESDCDM	Charge Device Model 13	-500	+500	V
Maximum latch–up free current at any pin	ILATCH		-250	+250	mA
Junction temperature 2	Tvj			+155	°C
Storage temperature	Tstg		-55	+150	°C
Rthjc QFN32 14	Rthjc		10		K/W
Rthjc QFN48 14			5		
Rthjc TQFP48 14			5.5		

Table 5 – Absolute Maximum Ratings

8 During short transient pulses smaller than 1us and while the LS driver is fully connecting the LS pin to GND (i.e. LSI N DRV[3:0]=0xF), the voltage on any LS<2:0> pin is allowed: -1V ≤ LS<2:0> ≤ -0.5: if the current flowing out of any LS<2:0> pin does not exceed 75mA. The sum of all currents flowing out of the LS pins during these conditions must not exceed 150mA

9 During short transient pulses smaller than 1us, the voltage on any HS<2:0> pin and any U,V or W pin is allowed: -1V ≤ HS<2:0>, U,V,W ≤ -0.5: if the current flowing out of any pin HS<2:0>, U,V,W does not exceed 50mA

10 During short transient pulses smaller than 1us, the sum of all currents flowing out of pins HS<2:0> and U,V,W with -1V < HS<2:0>, U,V,W <-0.5 must not exceed 75mA

11 There might be ripple on the VBAT_S1 pin due to parasitic elements in the supply line. Positive voltage peaks with a slew rate larger than Spdd should be limited to Vpdd (see Datasheet). This only applies if the high side current sensor is switched on

12 Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor conform to AEC-Q100-002 or ESDA/JEDEC JDS-001

13 ESD CDM Test confirm to AEC-Q100-011 or JEDEC22-C101

14 Simulated value for low conductance board (JEDEC)

5. Application Examples [15]

The following sections show typical application examples

5.1 Sensor-less BLDC Motor Control on the LIN bus or via PWM-Interface

The below application example with MLX81205 realizes a sensor-less control of a BLDC motor via three external power N-FET half bridges, with only a few external components. The high side N-FET driver is built with a bootstrap output stage. Reverse polarity protection of the bridge is realized with an external power N-FET. An external temperature sensor is connected to the 10 bit ADC via pin IO1. The integrated window watchdog is monitoring application integrity. The communication interface can be either LIN or PWM interface. Pins LIN and IOHV can be used as wake-up sources and furthermore pin LIN will be also used to program the Flash memory.

[15] All application examples are principal schematics only. Details need to be worked out for each application separately, depending on application requirements

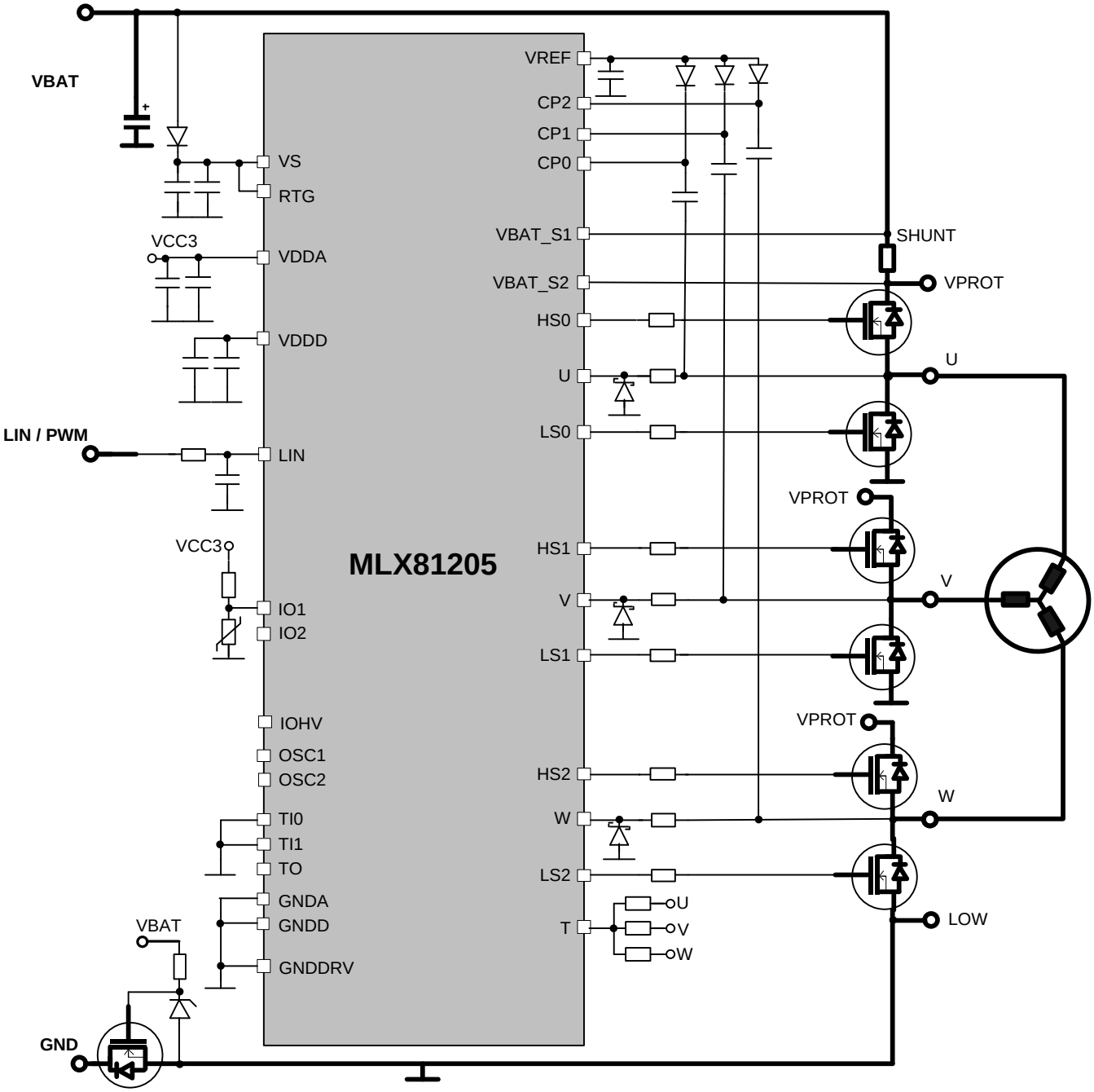


Figure 2 – Sensor-less BLDC Motor Control with MLX81205

The motor currents are measured by a shunt resistor in battery path. In case current exceeds the programmed threshold, the bridge can be switched off automatically without software interaction and in addition a software interrupt can be generated. The motor current can also be measured by the 10 bit ADC.
The patented Melexis TruSense technology combines two methods to determine the rotor position:

- The measurement of the induced BEMF voltage at medium and high speeds
- The measurement of position depending on coil inductance variations at stand-still and low speeds

As a result TruSense allows operation of the motor in the widest dynamic speed range. The motor can be driven with block, trapezoidal or sine-wave currents. The motor start-up can be made independent of the load conditions according to the application requirements. In this example application the motor star point is not available. It is modelled with external resistors from the motor phases and connected to T input. Alternatively an artificial IC internal reference point can be chosen as shown in the block diagram of the MLX81205/07.

5.2 Sensor-less BLDC Motor Control with LIN bus or via PWM Interface with reverse polarity protection in the battery path

In the following sample application MLX81207 has been selected in order to benefit from the external high side reverse polarity protection possibility. All other remarks from the previous application example remain valid.

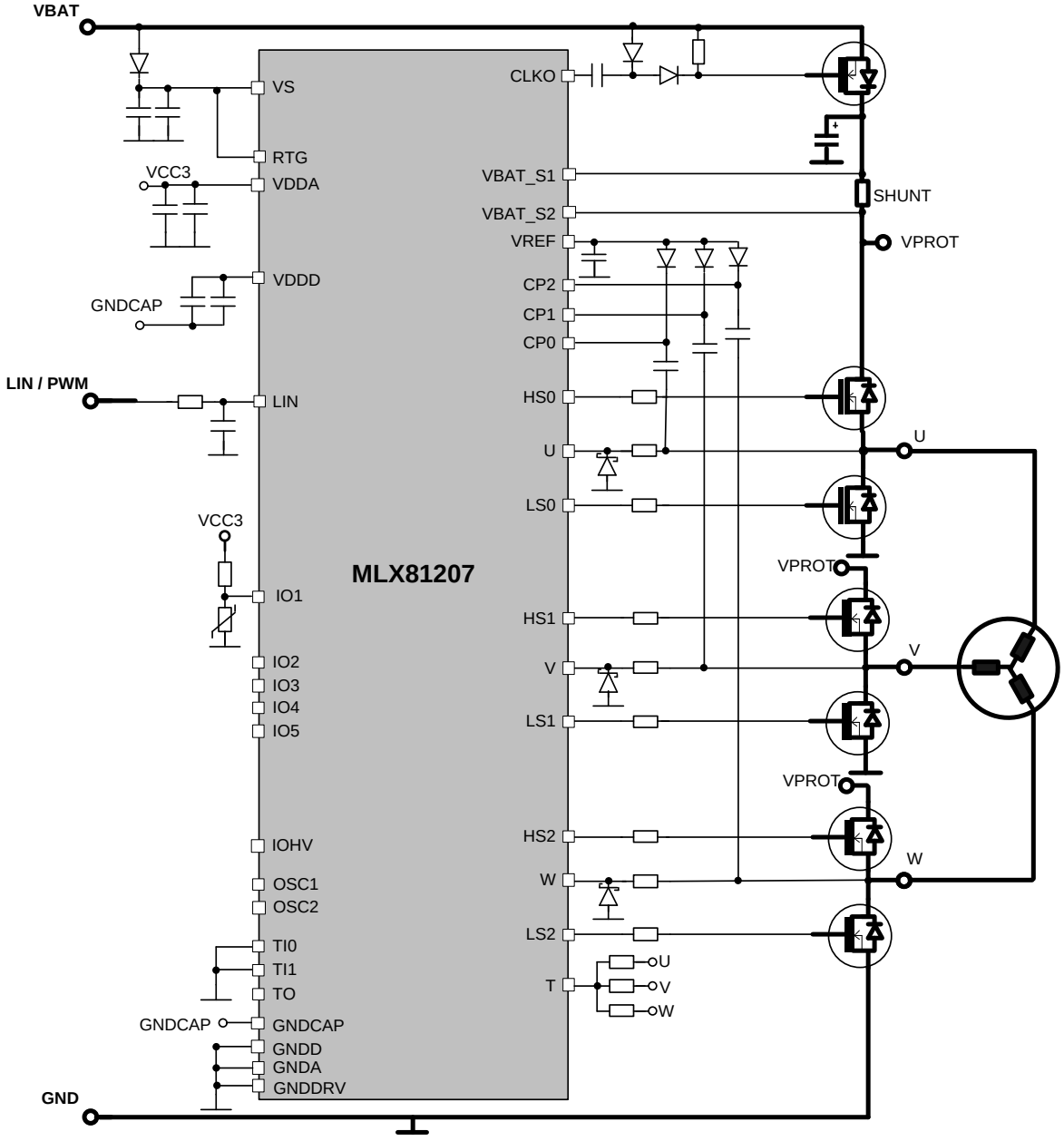


Figure 3 – Typical Sensor-less BLDC Motor Control Application Example with MLX81207

5.3 Sensor based BLDC Motor Control

In sample application below, the chip MLX81207 is driving a BLDC motor with 3 Hall sensors. An external P-FET is used to generate the 3.3V supply with a higher current capability in order to keep the power dissipation outside of the MLX81207 IC.

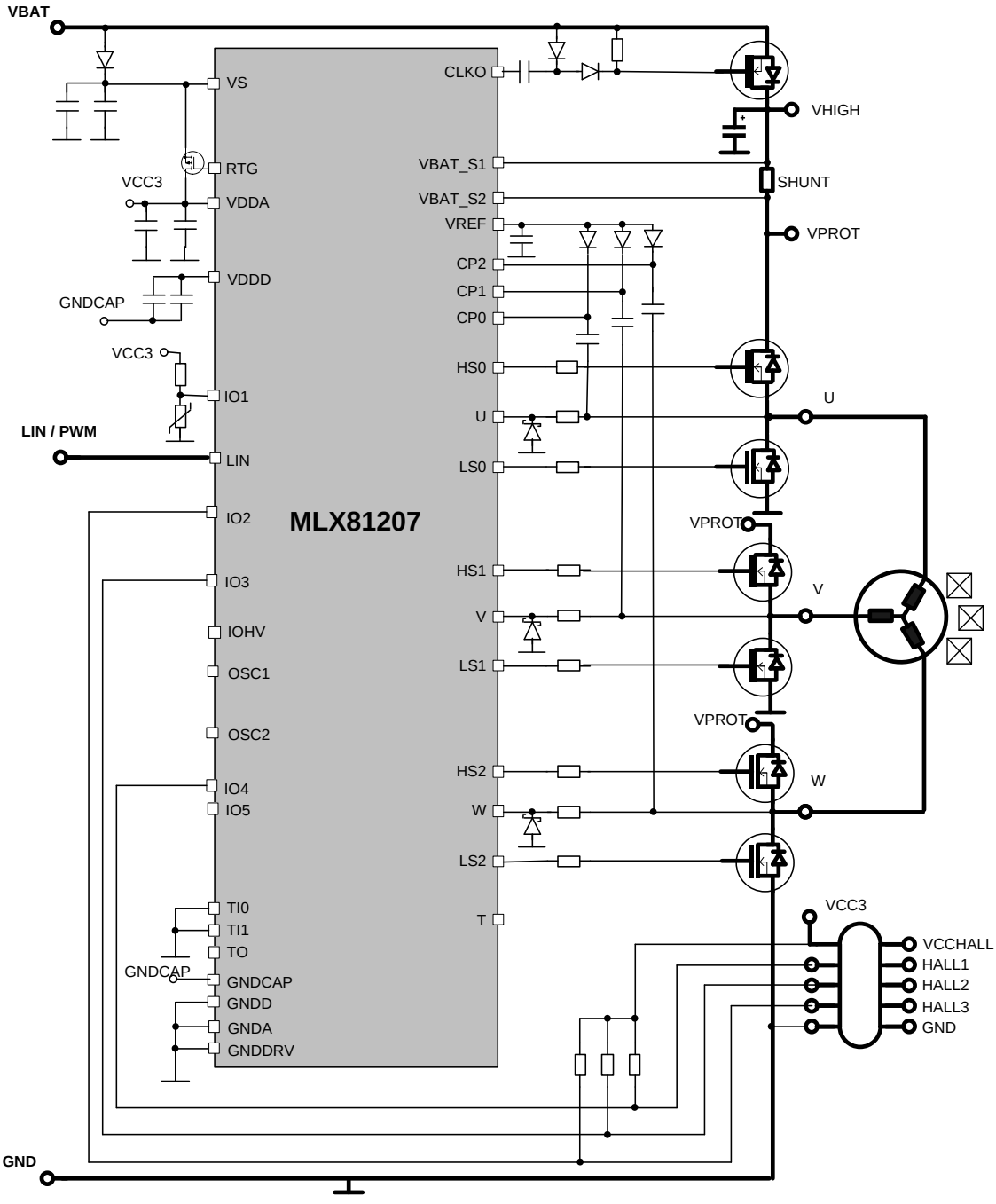


Figure 4 – Typical Sensor based BLDC Motor Control Application Example with MLX81207

6. Mechanical Specification [16]

6.1 QFN packages

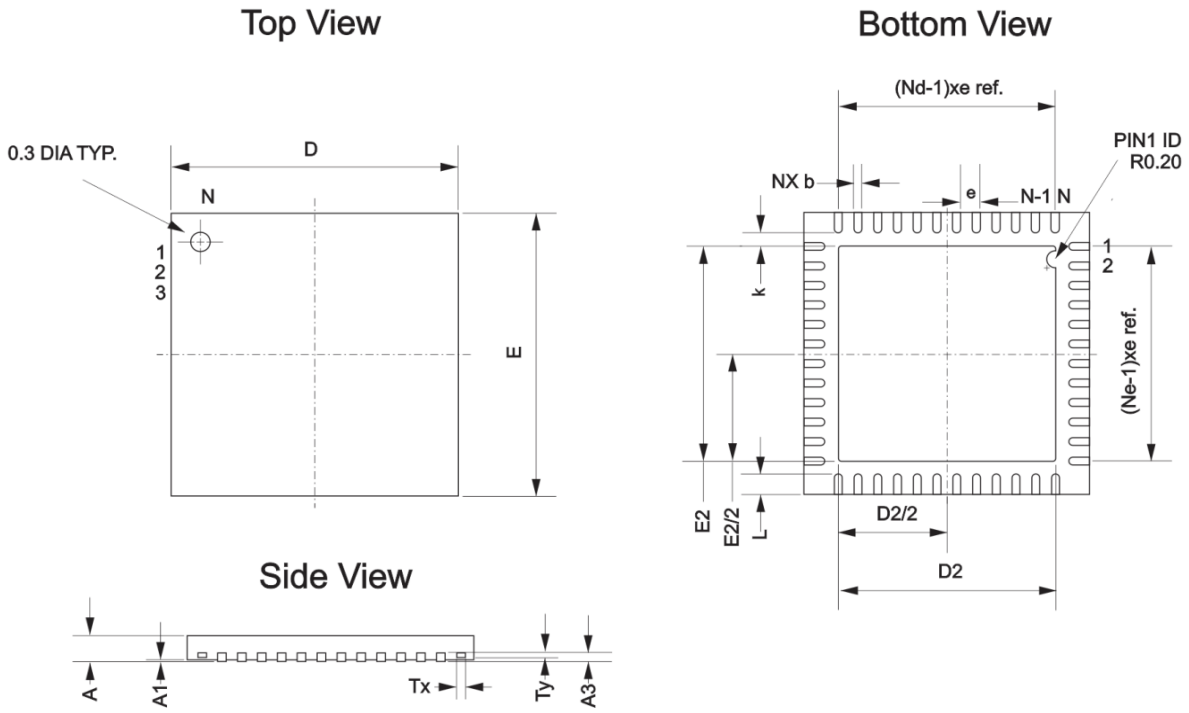


Figure 5 - QFN Package Drawing

6.1.1. QFN32_WF 5x5 (32 leads)

Symbol [17]	A	A1	A3	b	D	D2	E	E2	e	L	Tx	Ty	N [18]	Nd [19]	Ne 19
Min	0.80	0.00		0.18		3.50		3.50		0.35					
Nom	0.90	0.02	0.20	0.25	5.00	3.60	5.00	3.60	0.50	0.40	0.16	0.10	32	8	8
Max	1.00	0.05		0.30		3.70		3.70		0.45					

Table 6 – QFN32_WF 5x5 Package Dimensions

[16] Dimensions and tolerances conform to ASME Y14.5M-1994
[17] Dimensions in millimetres, angles in degrees
[18] N is the total number of terminals
[19] ND and NE refer to number of terminals on each D and E side respectively

6.1.2. QFN48_WF 7x7 (48 leads)

Symbol 17	A	A1	A3	b	D	D2	E	E2	e	L	Tx	Ty	N 18	Nd 19	Ne 19
Min	0.80	0		0.18		5.00		5.00		0.40					
Nom	0.90	0.02	0.20	0.25	7.00	5.10	7.00	5.10	0.50	0.50	0.165	0.100	48	12	12
Max	1.00	0.05		0.30		5.20		5.20		0.60					

Table 7 – QFN48_WF 7x7 Package Dimensions

6.2 TQFP package (48 leads)

	A	A1	A2	b	b1	D	D1	D2	E	E1	E2	e	L	N	ccc	ddd
Min	-	0.05	0.95	0.17	0.17								0.45		-	-
Nom	-	-	1.00	0.22	0.20	9.00	7.00	5.00	9.00	7.00	5.00	0.50	0.60	48	-	-
Max	1.20	0.15	1.05	0.27	0.23								0.75		0.08	0.08

Notes:
1. All Dimensioning and Tolerances conform to ASME Y14.5M-1994,
Δ2. Datum Plane [-|-|-] located at Mould Parting Line and coincident with Lead, where Lead exists, plastic body at bottom of parting line.
Δ3. Datum [A-B] and [-D-] to be determined at centreline between leads where leads exist, plastic body at datum plane [-|-|-]
Δ4. To be determined at seating plane [-C-]
Δ5. Dimensions D1 and E1 do not include Mould protrusion. Dimensions D1 and E1 do not include mould protrusion. Allowable mould protrusion is 0.254 mm on D1 and E1 dimensions.
6. 'N' is the total number of terminals
Δ7. These dimensions to be determined at datum plane [-|-|-]
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
Δ9. Dimension b does not include dam bar protrusion, allowable dam bar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition, dam bar cannot be located on the lower radius of the foot.
10. Controlling dimension millimetre.
11. maximum allowable die thickness to be assembled in this package family is 0.38mm
12. This outline conforms to JEDEC publication 95 Registration MS-026, Variation ABA, ABC & ABD.
Δ13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
Δ14. Dimension D2 and E2 represent the size of the exposed pad. The actual dimensions are specified in bonding diagram, and are independent from die size.
15. Exposed pad shall be coplanar with bottom of package within 0.05.

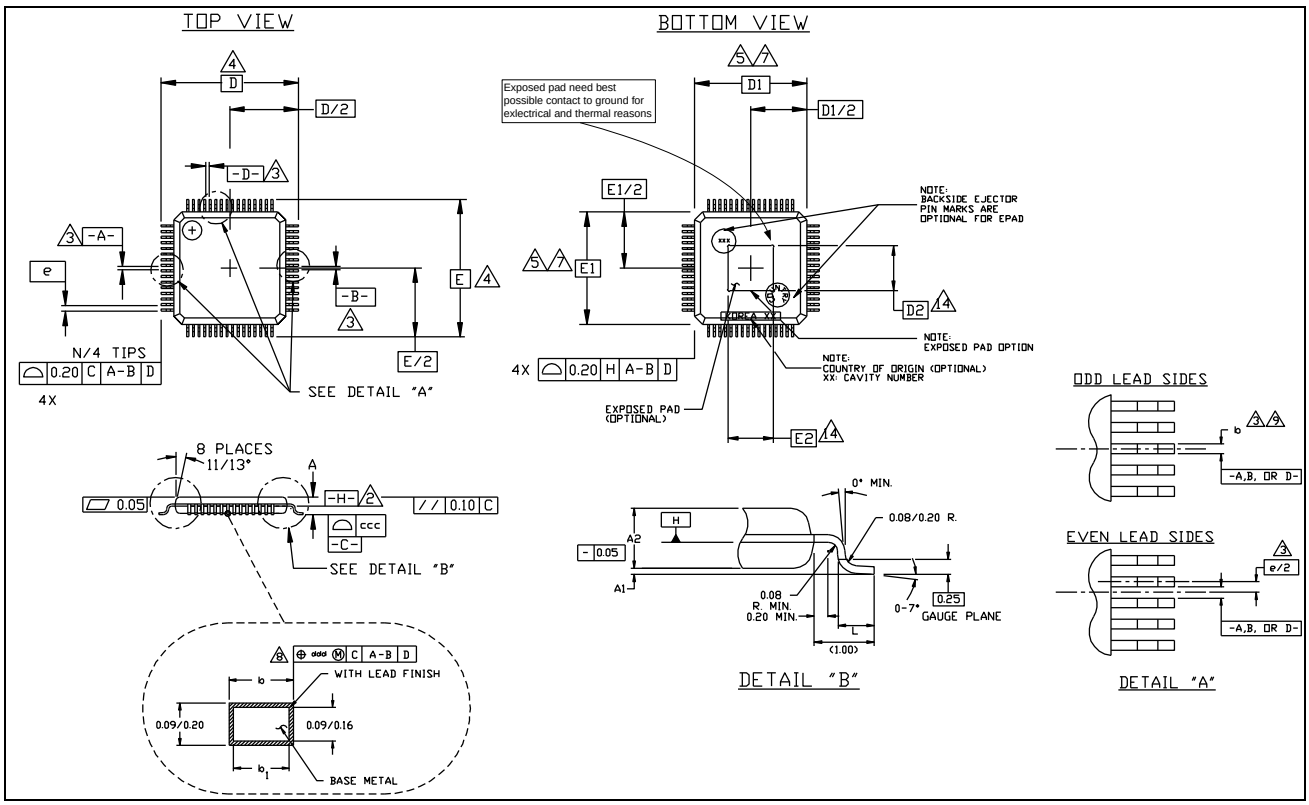


Figure 6 – TQFP 7x7 Drawing

6.3 Marking MLX81205/07

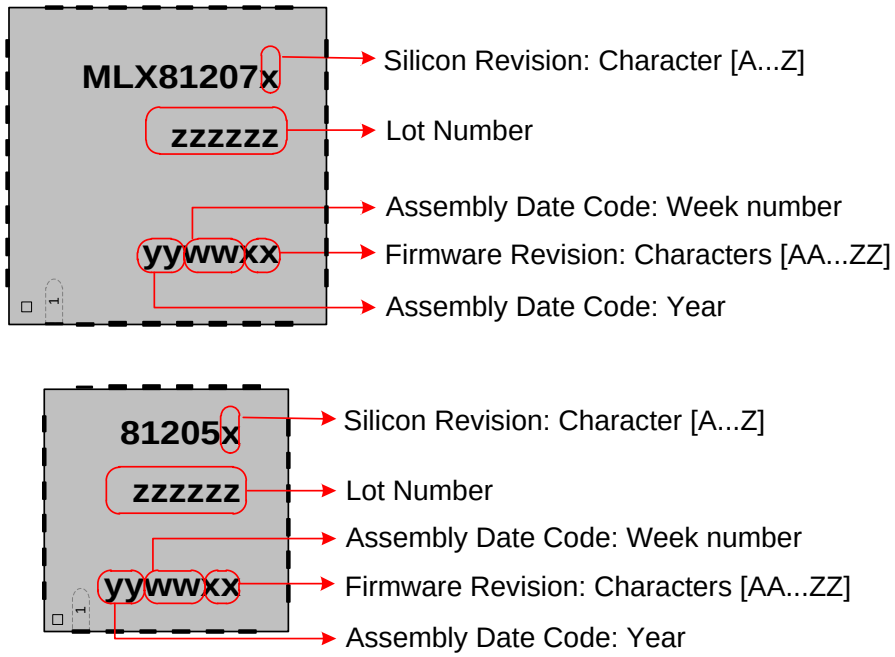


Figure 7 – Marking Code

The exposed pad is connected to IC substrate via conductive glue and must be connected to PCB ground.

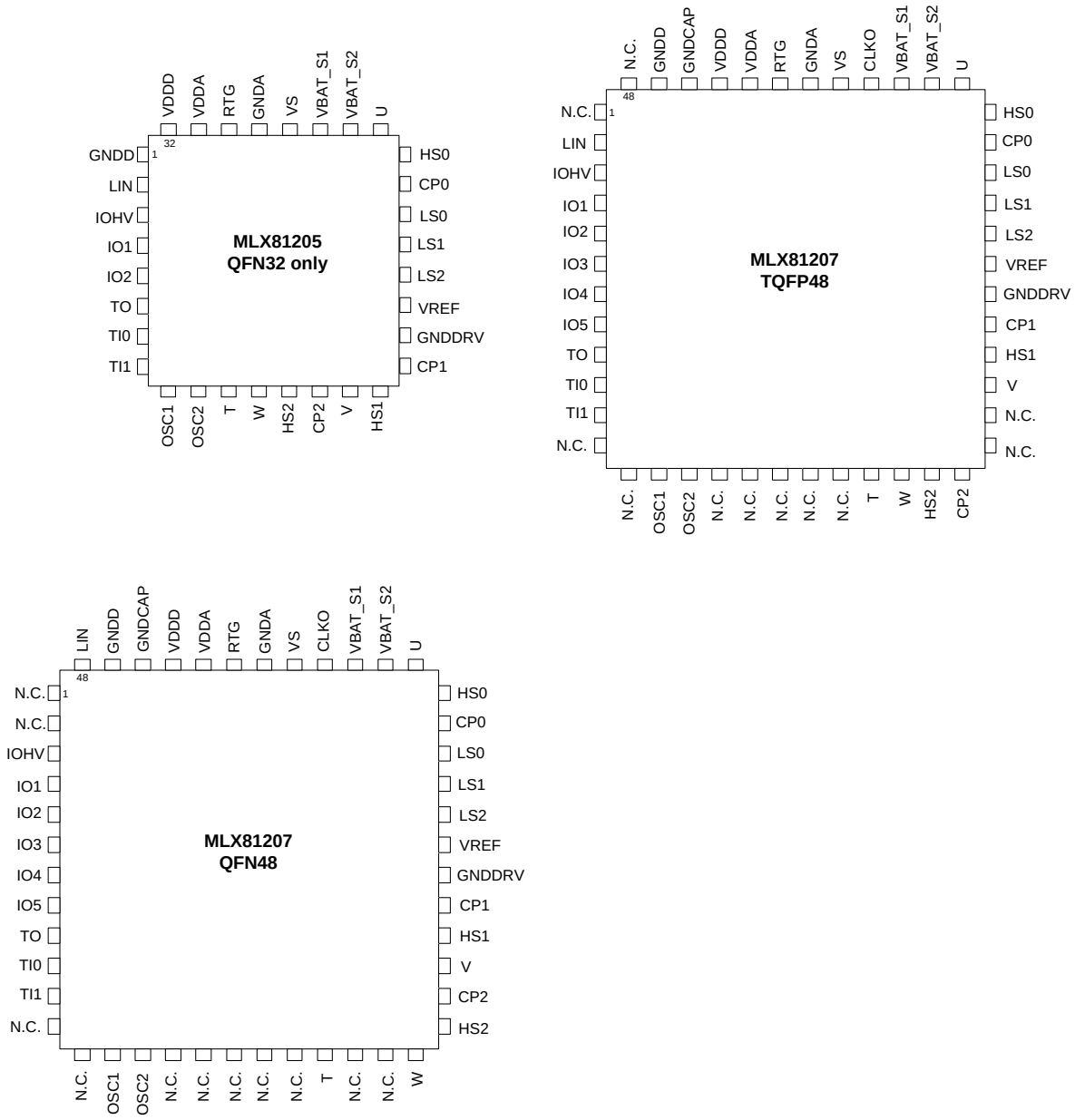


Figure 8 – MLX81205/07 Pins

7. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solder ability and moisture sensitivity level according to following test methods:

Reflow Soldering SMDs (Surface Mount Devices)

IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices
(Classification reflow profiles according to table 5-2)
EIA/JEDEC JESD22-A113
Preconditioning of Non-hermetic Surface Mount Devices Prior to Reliability Testing
(Reflow profiles according to table 2)

Wave Soldering SMDs (Surface Mount Devices) and THDs (Through Hole Devices)

EN60749-20
Resistance of plastic- encapsulated SMDs to combined effect of moisture and soldering heat
EIA/JEDEC JESD22-B106 and EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THDs (Through Hole Devices)

EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Solderability SMDs (Surface Mount Devices) and THDs (Through Hole Devices)

EIA/JEDEC JESD22-B102 and EN60749-21

Solderability
For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMDs is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

8. Disclaimer

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