MCP433X/435X

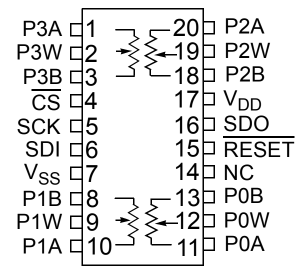
7/8-Bit Quad SPI Digital POT with Volatile Memory

Features

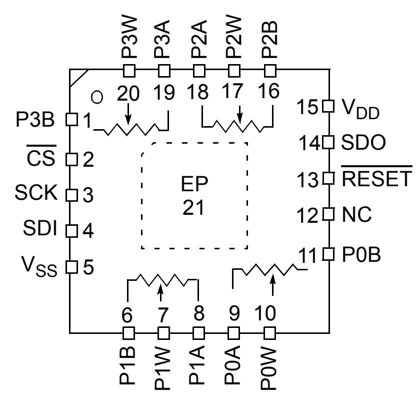
- Quad Resistor Network
- Potentiometer or Rheostat Configuration Options
- Resistor Network Resolution:
  - 7-bit: 128 Resistors (129 Taps)
  - 8-bit: 256 Resistors (257 Taps)
- R_{AB} Resistances Options of:
  - 5 kΩ
  - 10 kΩ
  - 50 kΩ
  - 100 kΩ
- Zero Scale to Full Scale Wiper Operation
- Low Wiper Resistance: 75 Ω (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- SPI Serial Interface (10 MHz, Modes 0,0 and 1,1):
  - High-Speed Read/Writes to wiper registers
- Resistor Network Terminal Disconnect Feature via Terminal Control (TCON) Register
- Reset Input Pin
- Brown-out Reset Protection (1.5V typical)
- Serial Interface Inactive Current (2.5 µA typical)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Supports Split Rail Applications
- Internal Weak Pull-up on all Digital Inputs
- Wide Operating Voltage:
  - 2.7V to 5.5V – Device Characteristics Specified
  - 1.8V to 5.5V – Device Operation
- Wide Bandwidth (-3 dB) Operation:
  - 2 MHz (typical) for 5.0 kΩ device
- Extended Temperature Range (-40°C to +125°C)

Package Types (Top View)

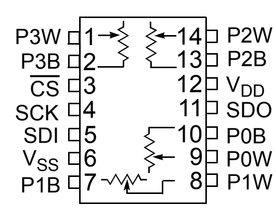
MCP43X1 Quad Potentiometers
TSSOP



MCP43X1 Quad Potentiometers
4x4 QFN*

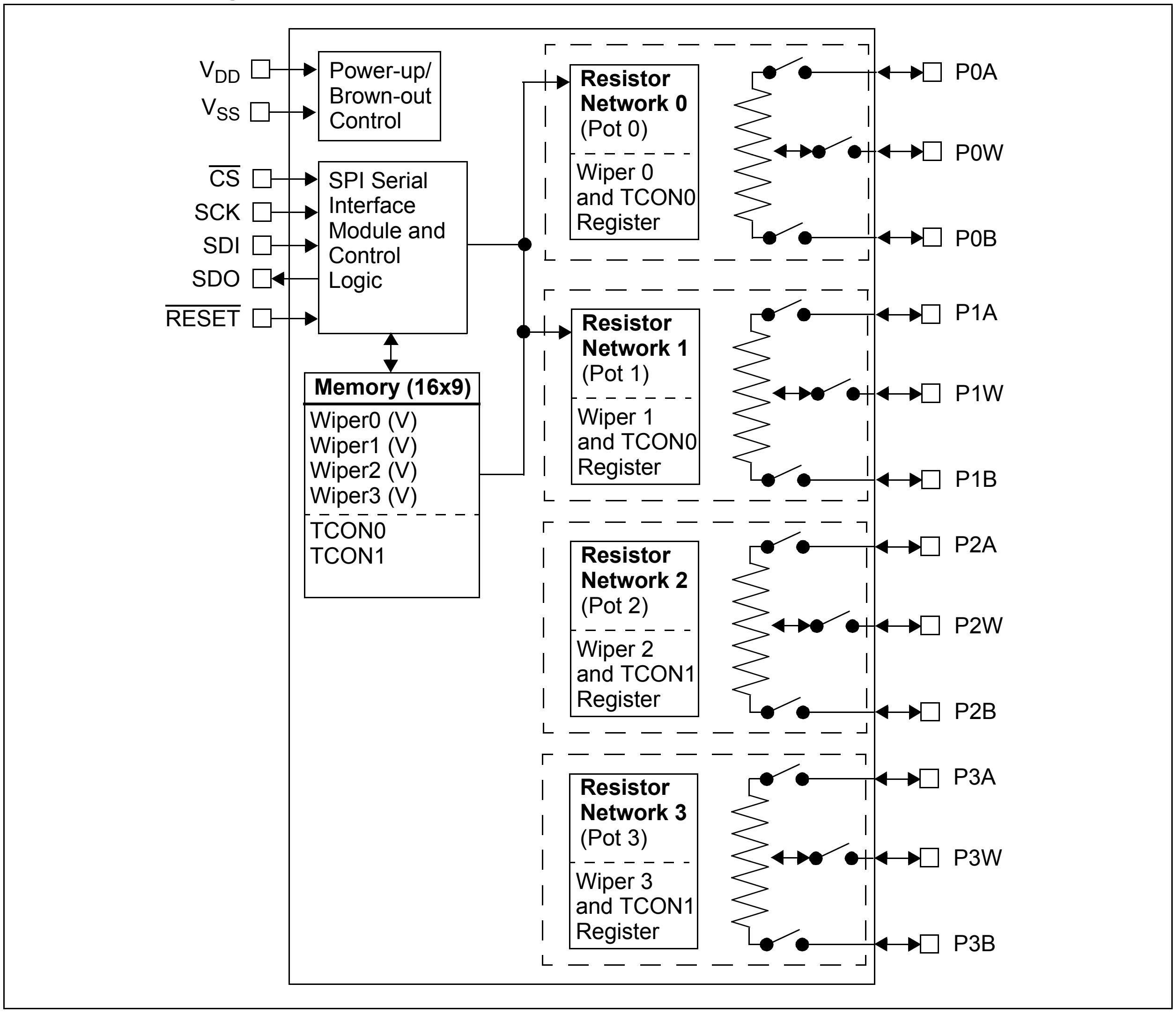


MCP43X2 Quad Rheostat
TSSOP



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	Memory Type	WiperLock Technology	POR Wiper Setting	Resistance (typical) R_{AB} Options (kΩ)	Resistance (typical) Wiper - R_W (Ω)	# of Taps	V_{DD} Operating Range [2]
MCP4331	4	Potentiometer [1]	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4332	4	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4341	4	Potentiometer [1]	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4342	4	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4351	4	Potentiometer [1]	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4352	4	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4361	4	Potentiometer [1]	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4362	4	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +7.0V
Voltage on $\overline{CS}$, SCK, SDI, SDI/SDO, and $\overline{RESET}$ with respect to V_{SS} .... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, PxB and SDO) with respect to V_{SS} .... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ ON HV pins) ....±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ....±20 mA
Maximum output current sunk by any Output pin ....25 mA
Maximum output current sourced by any Output pin ....25 mA
Maximum current out of V_{SS} pin .... 100 mA
Maximum current into V_{DD} pin .... 100 mA
Maximum current into PxA, PxW and PxB pins ±2.5 mA Storage temperature ....-65°C to +150°C
Ambient temperature with power applied ....-40°C to +125°C
Package power dissipation (T_A = +50°C, T_J = +150°C) TSSOP-14 .... 1000 mW
TSSOP-20..1110 mW
QFN-20 (4x4) ....2320 mW
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins ....≥ 4 kV (HBM), ... ≥ 300V (MM)
Maximum Junction Temperature (T_J) .... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $-40°C \le T_A \le +125°C$ (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Supply Voltage	V_{DD}	2.7	—	5.5	V		
		1.8	—	2.7	V	Serial Interface only.	
$\overline{CS}$, SDI, SDO, SCK, $\overline{RESET}$ pin Voltage Range	V_{HV}	V_{SS}	—	12.5V	V	$V_{DD} \ge 4.5V$	The $\overline{CS}$ pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
		V_{SS}	—	V_{DD} + 8.0V	V	$V_{DD} < 4.5V$	
V_{DD} Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}	
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 9**)			V/ms		
Delay after device exits the Reset state ($V_{DD} > V_{BOR}$)	T_{BORD}	—	10	20	µs		
Supply Current **(Note 10)**	I_{DD}	—	—	450	µA	Serial Interface Active, V_{DD} = 5.5V, $\overline{CS} = V_{IL}$, SCK @ 5 MHz, write all 0's to volatile Wiper 0 (address 0h)	
		—	2.5	5	µA	Serial Interface Inactive, $\overline{CS} = V_{IH}$, V_{DD} = 5.5V	
		—	0.55	1	mA	Serial Interface Active, V_{DD} = 5.5V, $\overline{CS} = V_{IHH}$, SCK @ 5 MHz, decrement volatile Wiper 0 (address 0h)	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistance (± 20%)	R_{AB}	4.0	5	6.0	kΩ	-502 devices **(Note 1)**	
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**	
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**	
		80.0	100	120.0	kΩ	-104 devices **(Note 1)**	
Resolution	N	257			Taps	8-bit	No Missing Codes
		129			Taps	7-bit	No Missing Codes
Step Resistance	R_S	—	R_{AB}/ (256)	—	Ω	8-bit	**Note 6**
		—	R_{AB}/ (128)	—	Ω	7-bit	**Note 6**
Nominal Resistance Match	(| R_{ABWC} - R_{ABMEAN} |)/ R_{ABMEAN}	—	0.2	1.50	%	5 kΩ	**MCP43X1** devices only
		—	0.2	1.25	%	10 kΩ	
		—	0.2	1.0	%	50 kΩ	
		—	0.2	1.0	%	100 kΩ	
	(| R_{BWWC} - R_{BWMEAN} |)/ R_{BWMEAN}	—	0.25	1.75	%	5 kΩ	Code = Full Scale
		—	0.25	1.50	%	10 kΩ	
		—	0.25	1.25	%	50 kΩ	
		—	0.25	1.25	%	100 kΩ	
Wiper Resistance (**Note 3, Note 4**)	R_W	—	75	160	Ω	V_{DD} = 5.5 V, I_W = 2.0 mA, code = 00h	
		—	75	300	Ω	V_{DD} = 2.7 V, I_W = 2.0 mA, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (80h or 40h)	
Resistance Tracking	ΔR_{TRACK}	**Section 2.0**			ppm/°C	See **Section 2.0 "Typical Performance Curves"**	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 5, Note 6**
Maximum current through A, W or B	I_W	—	—	2.5	mA	Worst case current through wiper when wiper is either Full Scale or Zero Scale. **(Note 6)**
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP43X1** PxA = PxW = PxB = V_{SS}
		—	100	—	nA	**MCP43X2** PxB = PxW = V_{SS}

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP43X1** only.

4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Full Scale Error (**MCP43X1** only) (8-bit code = 100h, 7-bit code = 80h)	V_{WFSE}	-6.0	-0.1	—	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-4.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-3.5	-0.1	—	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-2.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.8	-0.1	—	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Zero Scale Error (**MCP43X1** only) (8-bit code = 00h, 7-bit code = 00h)	V_{WZSE}	—	+0.1	+6.0	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.5	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+2.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.8	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Potentiometer Integral Non-linearity	INL	-1	±0.5	+1	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP43X1** devices only **(Note 2)**	
		-0.5	±0.25	+0.5	LSb	7-bit		
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP43X1** devices only **(Note 2)**	
		-0.25	±0.125	+0.25	LSb	7-bit		
Bandwidth -3 dB (See Figure 2-92, load = 30 pF)	BW	—	2	—	MHz	5 kΩ	8-bit	Code = 80h
		—	2	—	MHz		7-bit	Code = 40h
		—	1	—	MHz	10 kΩ	8-bit	Code = 80h
		—	1	—	MHz		7-bit	Code = 40h
		—	200	—	kHz	50 kΩ	8-bit	Code = 80h
		—	200	—	kHz		7-bit	Code = 40h
		—	100	—	kHz	100 kΩ	8-bit	Code = 80h
		—	100	—	kHz		7-bit	Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP43X1** only.

4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Integral Non-linearity **MCP43X1** (**Note 4, Note 8**) **MCP43X2** devices only **(Note 4)**	R-INL	-1.5	±0.5	+1.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-8.25	+4.5	+8.25	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 900 µA
		-6.0	+4.5	+6.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-1.5	±0.5	+1.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-5.5	+2.5	+5.5	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 450 µA
		-4.0	+2.5	+4.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-1.5	±0.5	+1.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-2.0	+1	+2.0	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 90 µA
		-1.5	+1	+1.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-1.0	±0.5	+1.0	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-1.5	+0.25	+1.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA
		-0.8	±0.5	+0.8	LSb		7-bit	5.5V, I_W = 45 µA
		-1.125	+0.25	+1.125	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $-40°C \leq T_A \leq +125°C$ (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Differential Non-linearity **MCP43X1** (**Note 4, Note 8**) **MCP43X2** devices only **(Note 4)**	R-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-1.0	+0.5	+1.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 900 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-0.5	±0.25	+0.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-1.0	+0.25	+1.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 450 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-0.5	±0.25	+0.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 90 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-0.5	±0.25	+0.5	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 45 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = Full Scale
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, Code = Full Scale
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = Full Scale
Digital Inputs/Outputs ($\overline{\text{CS}}$, SDI, SDO, SCK, $\overline{\text{WP}}$, $\overline{\text{RESET}}$)						
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	$0.2V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	$0.1V_{DD}$	—	V	
High Voltage Input Entry Voltage	V_{IHH}	8.5	—	12.5 (6)	V	
High Voltage Input Exit Voltage	V_{IHH}	—	—	V_{DD} + 0.8V	V	
High Voltage Limit	V_{MAX}	—	—	12.5 (6)	V	Pin can tolerate V_{MAX} or less.
Output Low Voltage (SDO)	V_{OL}	V_{SS}	—	$0.3V_{DD}$	V	I_{OL} = 5 mA, V_{DD} = 5.5V
		V_{SS}	—	$0.3V_{DD}$	V	I_{OL} = 1 mA, V_{DD} = 1.8V
Output High Voltage (SDO)	V_{OH}	$0.7V_{DD}$	—	V_{DD}	V	I_{OH} = -2.5 mA, V_{DD} = 5.5V
		$0.7V_{DD}$	—	V_{DD}	V	I_{OL} = -1 mA, V_{DD} = 1.8V

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $-40°C \le T_A \le +125°C$ (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Weak Pull-up Current	I_{PU}	—	—	1.75	mA	Internal V_{DD} pull-up, V_{IHH} pull-down, V_{DD} = 5.5V, $V_{\overline{CS}}$ = 12.5V
		—	170	—	µA	$\overline{CS}$ pin, V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V
$\overline{CS}$ Pull-up/ Pull-down Resistance	R_{CS}	—	16	—	kΩ	V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V
$\overline{RESET}$ Pull-up Resistance	R_{RESET}	—	16	—	kΩ	V_{DD} = 5.5V, $V_{\overline{RESET}}$ = 0V
Input Leakage Current	I_{IL}	-1	—	1	µA	$V_{IN} = V_{DD}$ (all pins) and $V_{IN} = V_{SS}$ (all pins except $\overline{RESET}$)
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz
RAM (Wiper, TCON) Value						
Value Range	N	0h	—	1FFh	hex	8-bit device
		0h	—	1FFh	hex	7-bit device
TCON POR/BOR Setting			1FF		hex	All terminals connected
Wiper POR/BOR Setting	N		080h		hex	8-bit
			040h		hex	7-bit
Power Requirements						
Power Supply Sensitivity (**MCP43X1**)	PSS	—	0.0015	0.0035	%/%	8-bit; V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 80h
		—	0.0015	0.0035	%/%	7-bit; V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP43X1** only.
4: **MCP43X2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
8: The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network.

1.1 SPI Mode Timing Waveforms and Requirements

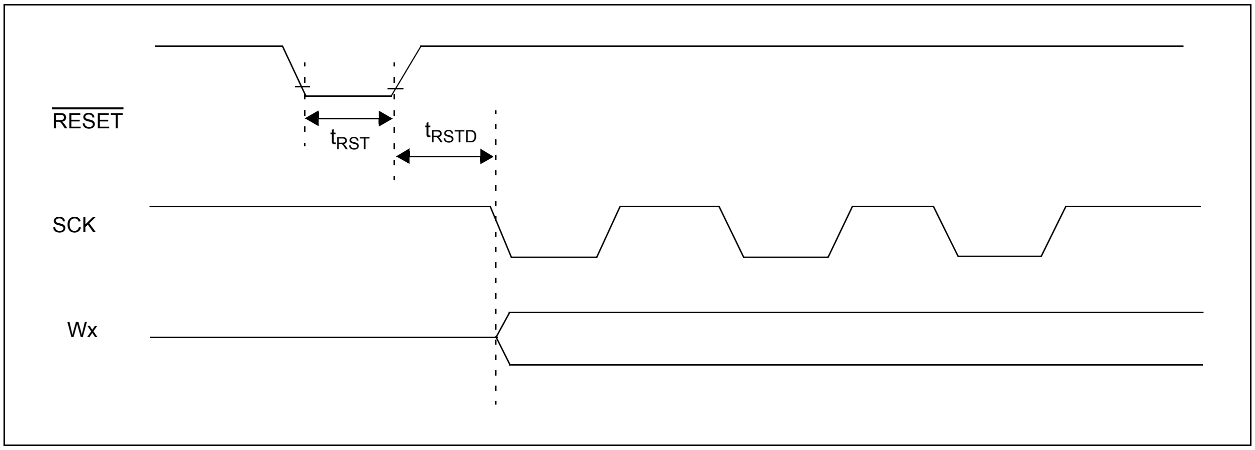


FIGURE 1-1: Reset Waveforms.

TABLE 1-1: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
$\overline{\text{RESET}}$ pulse width	t_{RST}	50	—	—	ns	
$\overline{\text{RESET}}$ rising edge normal mode (Wiper driving and SPI interface operational)	t_{RSTD}	—	—	20	ns	

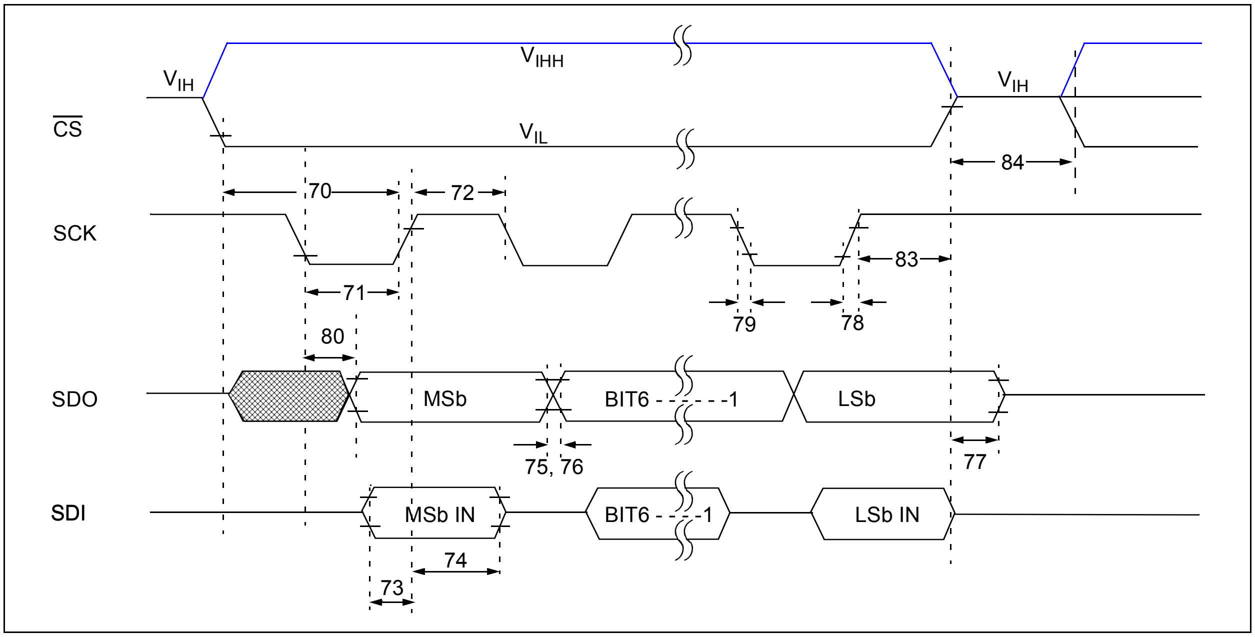


FIGURE 1-2: *SPI Timing Waveform (Mode = 11).*

TABLE 1-2: SPI REQUIREMENTS (MODE = 11)

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ input	TcsA2scH	60	—	ns	
71	SCK input high time	TscH	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK input low time	TscL	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	70	ns	V_{DD} = 2.7V to 5.5V
				170	ns	V_{DD} = 1.8V to 2.7V
83	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	TscH2csI	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		ms	V_{DD} = 1.8V to 2.7V
84	Hold time of $\overline{CS}$ Inactive (V_{IH}) to $\overline{CS}$ Active (V_{IL} or V_{IHH})	TcsA2csI	50	—	ns	

Note 1: This specification by design.

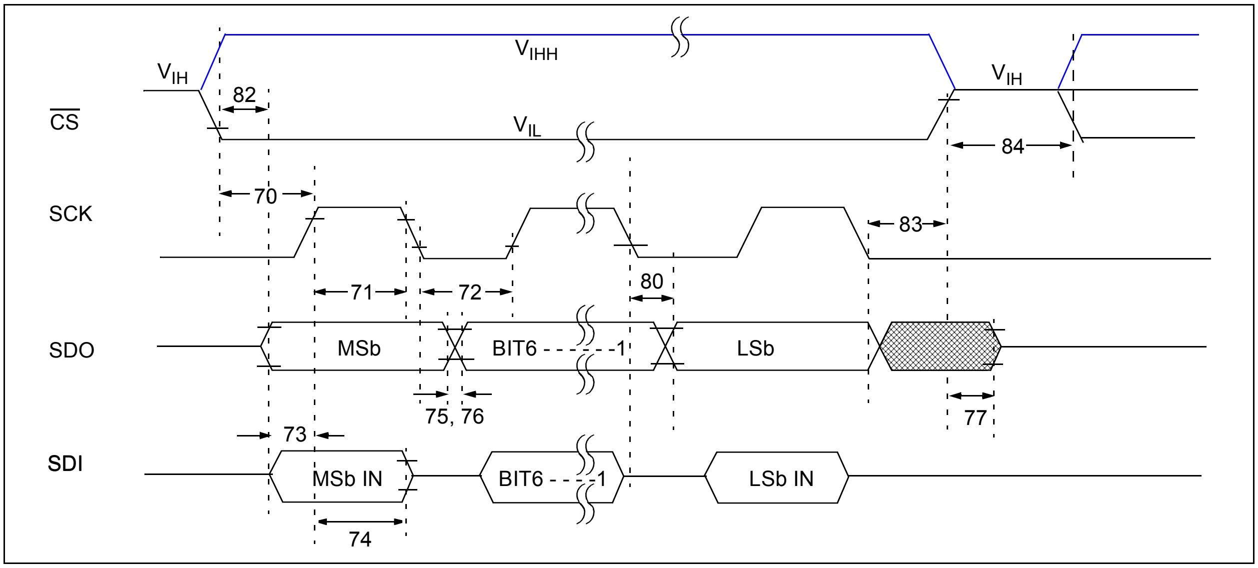


FIGURE 1-3: *SPI Timing Waveform (Mode = 00).*

TABLE 1-3: SPI REQUIREMENTS (MODE = 00)

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ input	TcsA2scH	60	—	ns	
71	SCK input high time	TscH	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK input low time	TscL	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	70	ns	V_{DD} = 2.7V to 5.5V
				170	ns	V_{DD} = 1.8V to 2.7V
82	SDO data output valid after $\overline{CS}$ Active (V_{IL} or V_{IHH})	TssL2doV	—	85	ns	
83	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	TscH2csI	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		ms	V_{DD} = 1.8V to 2.7V
84	Hold time of $\overline{CS}$ Inactive (V_{IH}) to $\overline{CS}$ Active (V_{IL} or V_{IHH})	TcsA2csI	50	—	ns	

Note 1: This specification by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 20L-QFN	θ_{JA}	—	43	—	°C/W	
Thermal Resistance, 20L-TSSOP	θ_{JA}	—	90	—	°C/W	

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

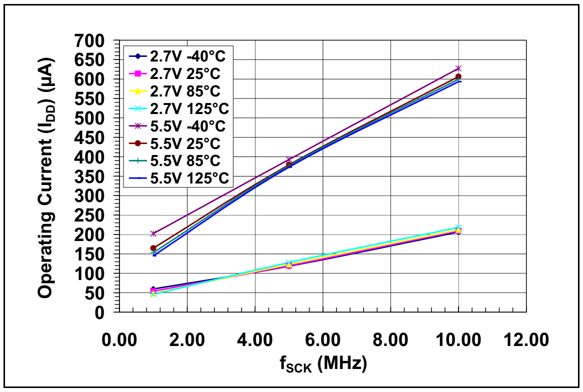


FIGURE 2-1: *Device Current (I_{DD}) vs. SPI Frequency (f_{SCK}) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

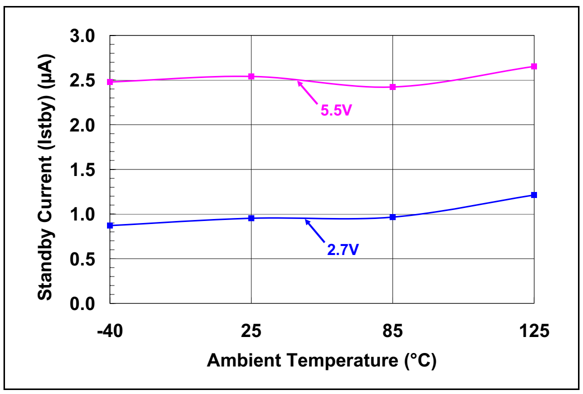


FIGURE 2-2: *Device Current (I_{SHDN}) and V_{DD}. ($\overline{CS}$ = V_{DD}) vs. Ambient Temperature.*

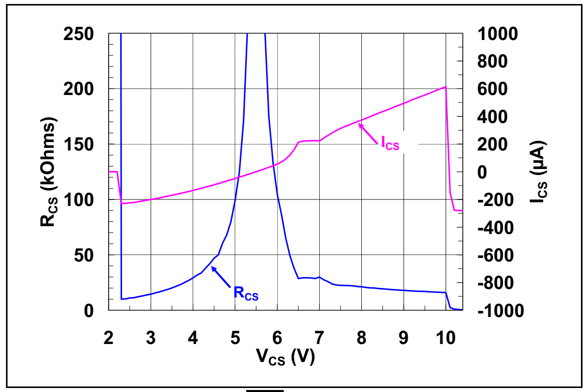


FIGURE 2-3: *$\overline{CS}$ Pull-up/Pull-down Resistance ($R_{\overline{CS}}$) and Current ($I_{\overline{CS}}$) vs. $\overline{CS}$ Input Voltage ($V_{\overline{CS}}$) (V_{DD} = 5.5V).*

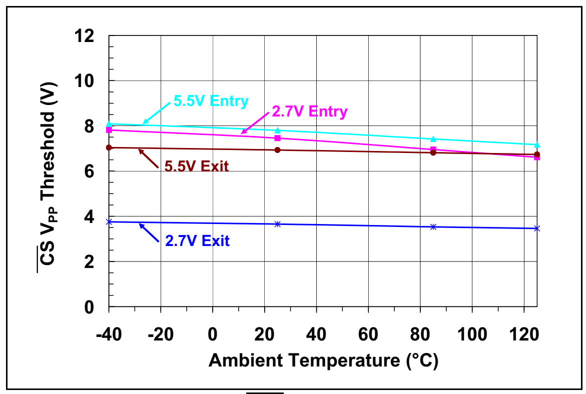


FIGURE 2-4: *$\overline{CS}$ High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

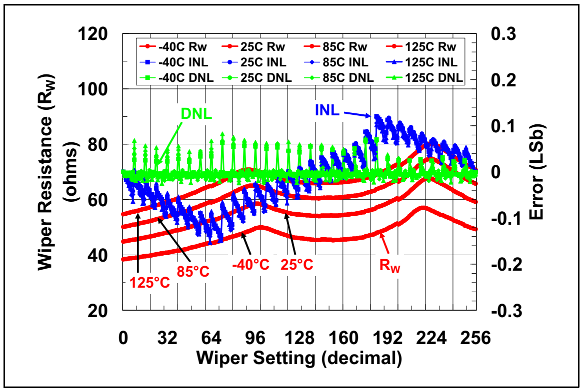


FIGURE 2-5: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

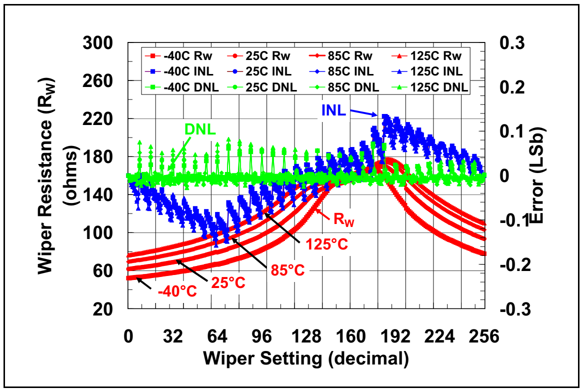
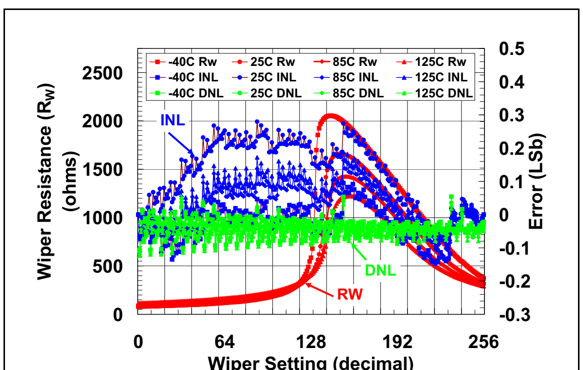


FIGURE 2-6: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-7: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

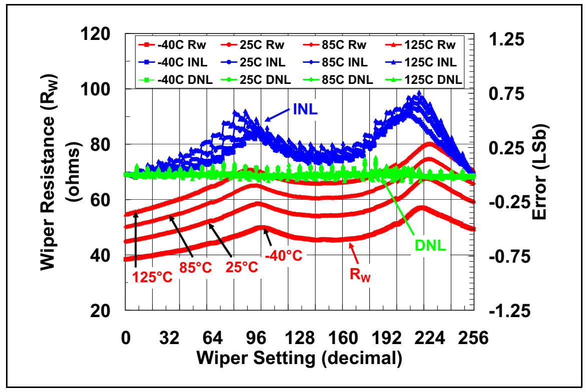


FIGURE 2-8: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 900 µA).

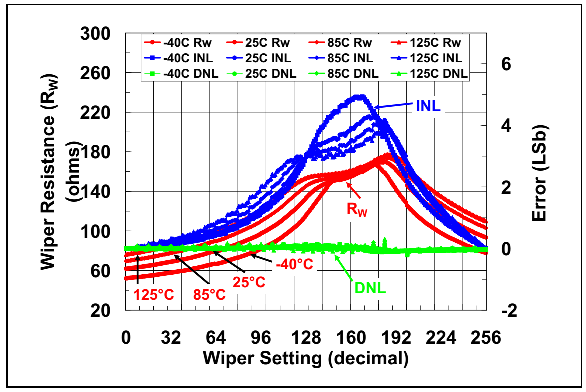
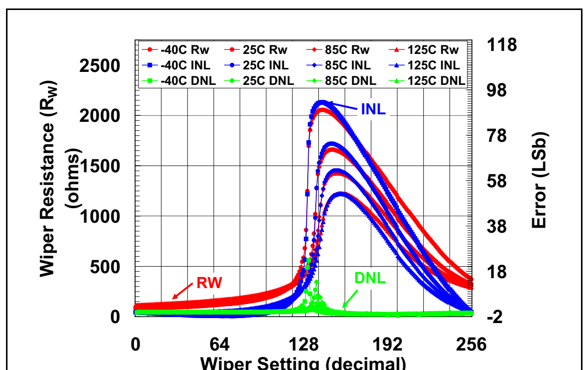


FIGURE 2-9: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 480 µA).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-10: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 260 µA).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

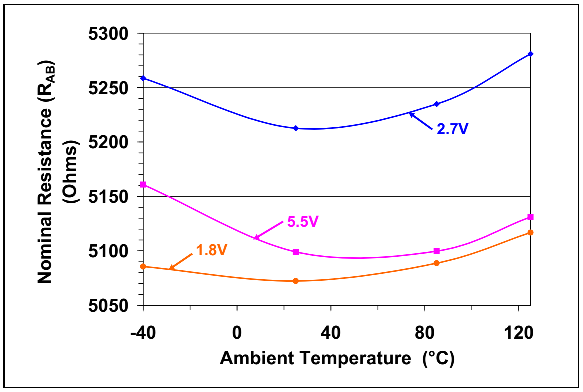


FIGURE 2-11: *5 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

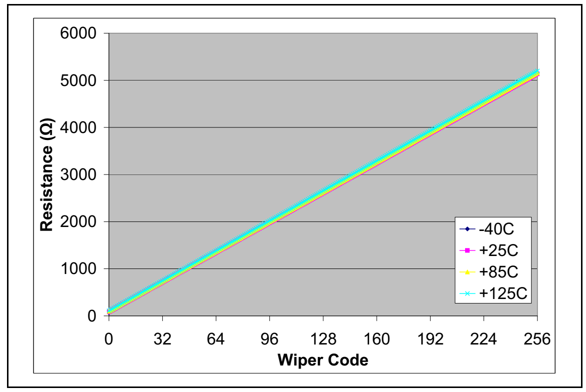


FIGURE 2-12: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 190 µA).*

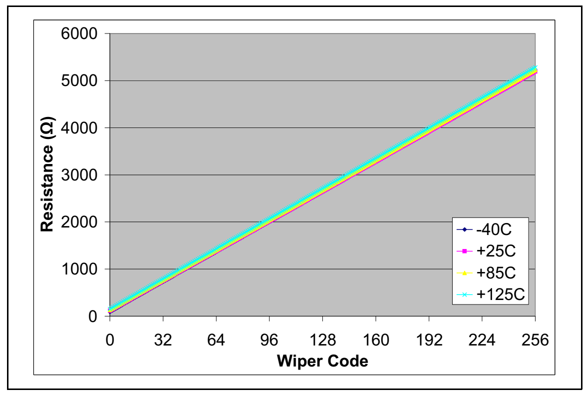
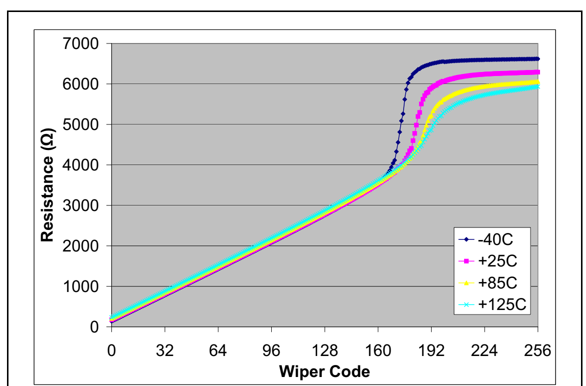


FIGURE 2-13: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 190 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-14: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 190 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

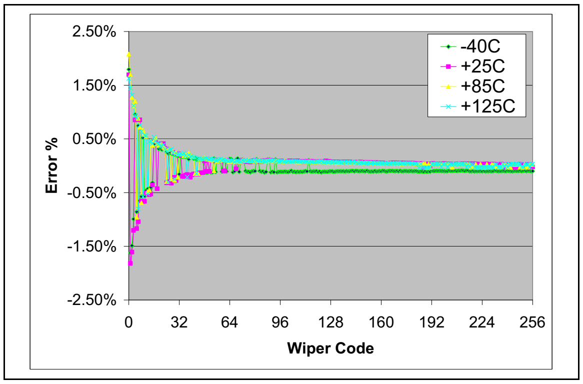


FIGURE 2-15: 5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 5.5V, I_W = 190 µA).

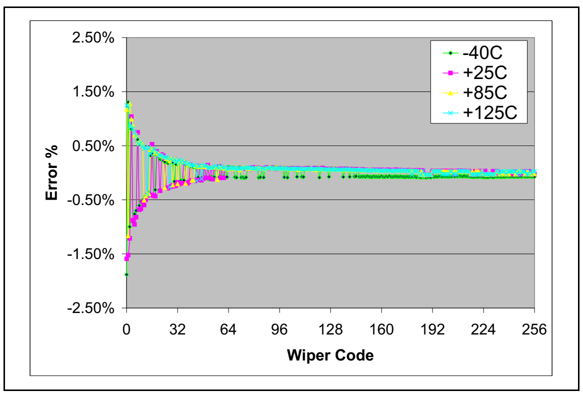
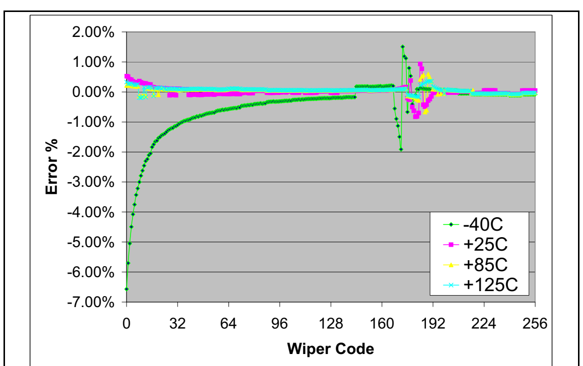


FIGURE 2-16: 5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 3.0V, I_W = 190 µA).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-17: 5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 1.8V, I_W = 190 µA).

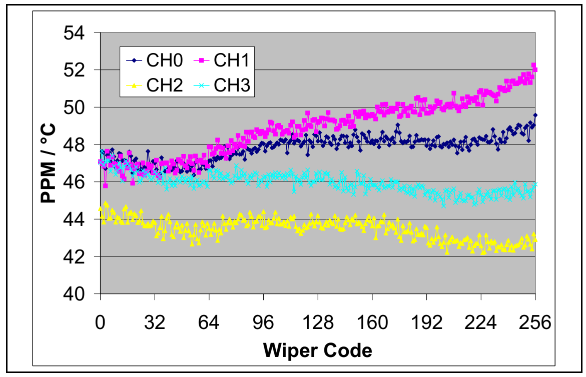


*FIGURE 2-18: 5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, I_W = 190 µA).*

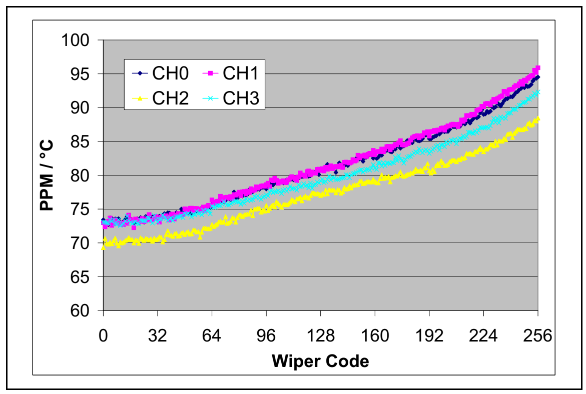
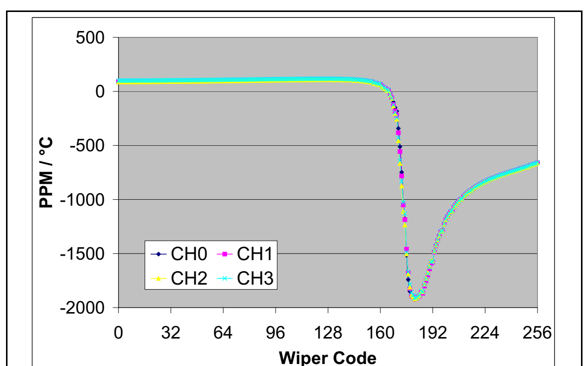


*FIGURE 2-19: 5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, I_W = 190 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

*FIGURE 2-20: 5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 1.8V, I_W = 190 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

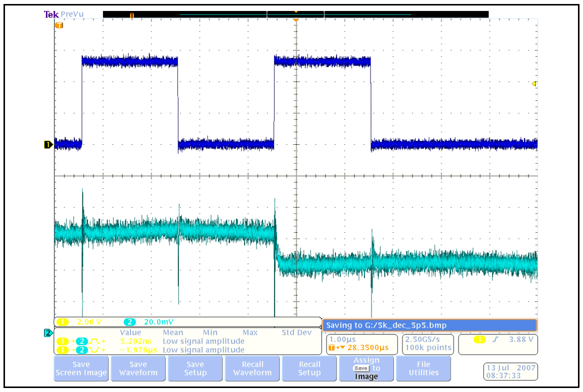


FIGURE 2-21: 5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).

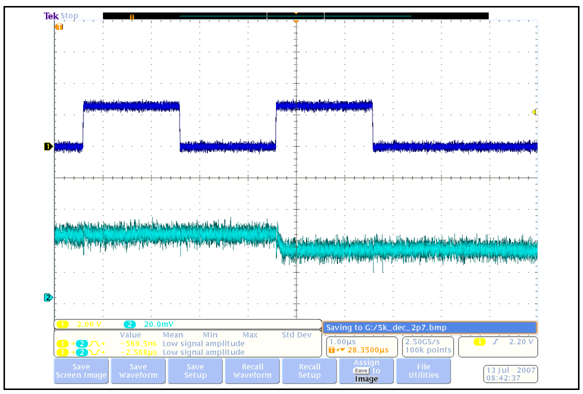


FIGURE 2-22: 5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).

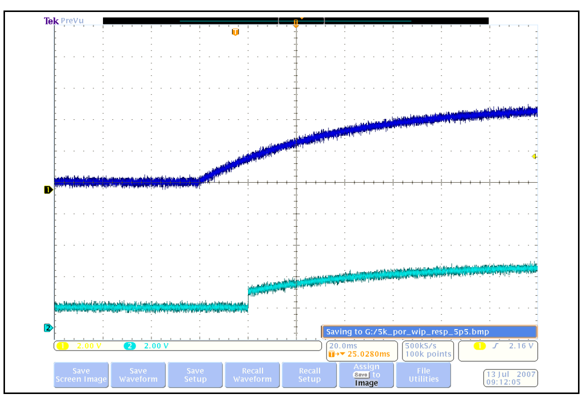


FIGURE 2-23: 5 kΩ – Power-Up Wiper Response Time (20 ms/Div).

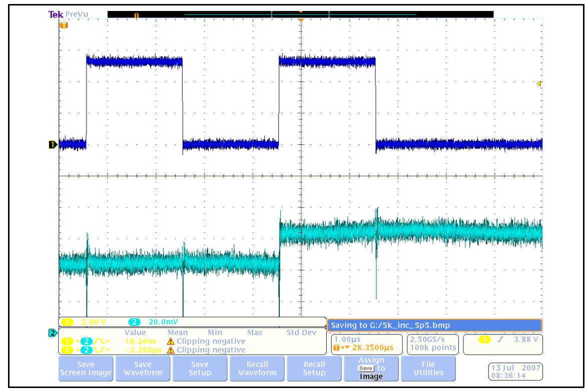


FIGURE 2-24: 5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).

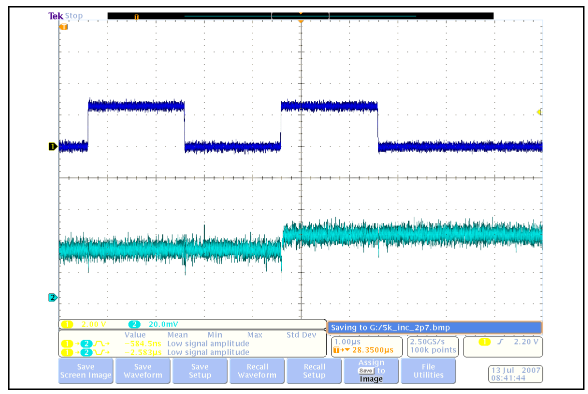


FIGURE 2-25: 5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

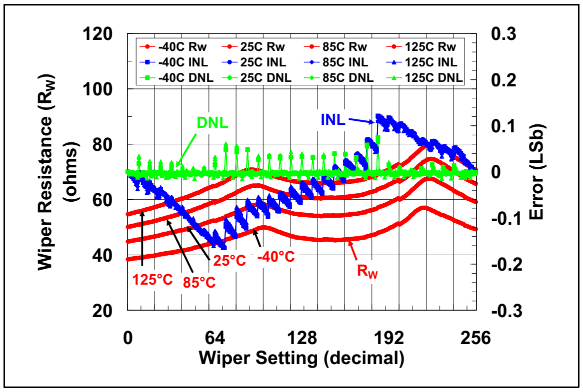


FIGURE 2-26: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

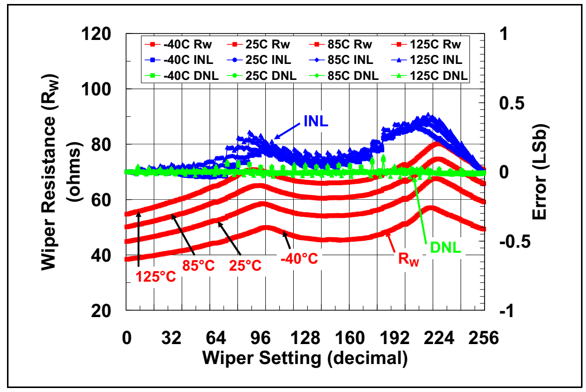


FIGURE 2-29: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 450 µA).

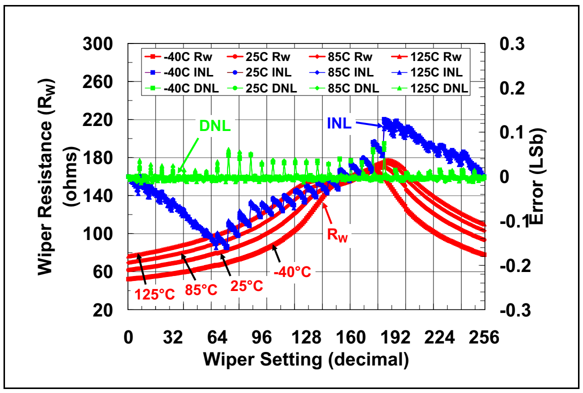


FIGURE 2-27: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).

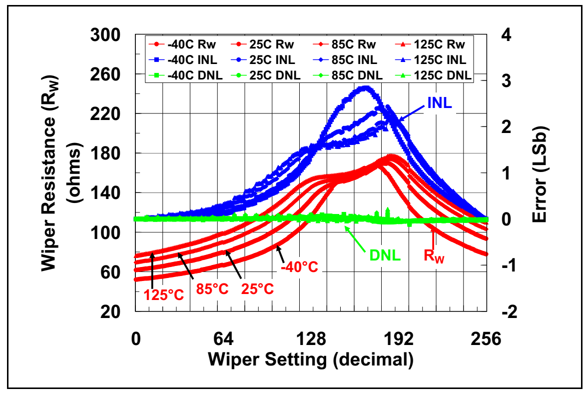
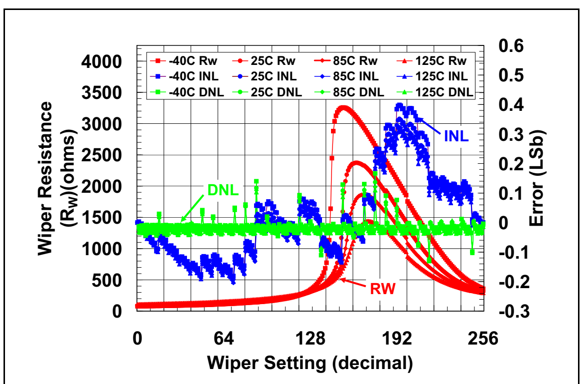
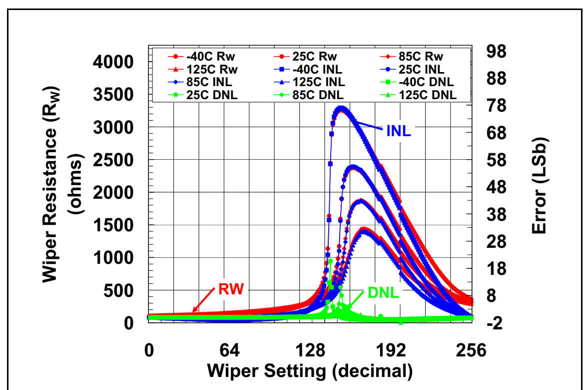


FIGURE 2-30: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 240 µA).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-28: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-31: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 125 µA).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

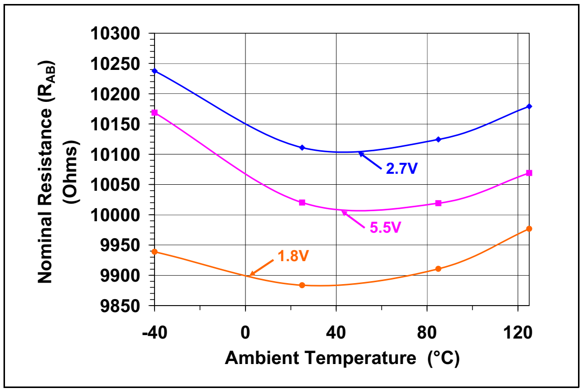


FIGURE 2-32: *10 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

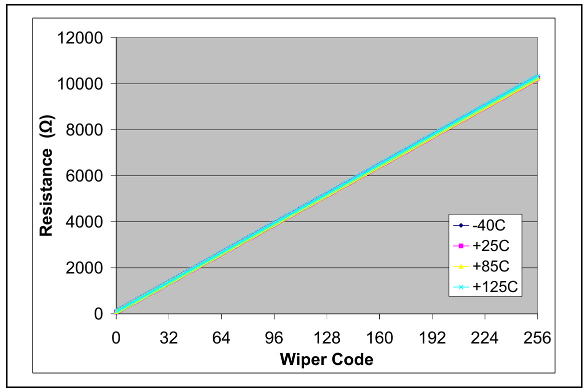


FIGURE 2-33: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 150 µA).*

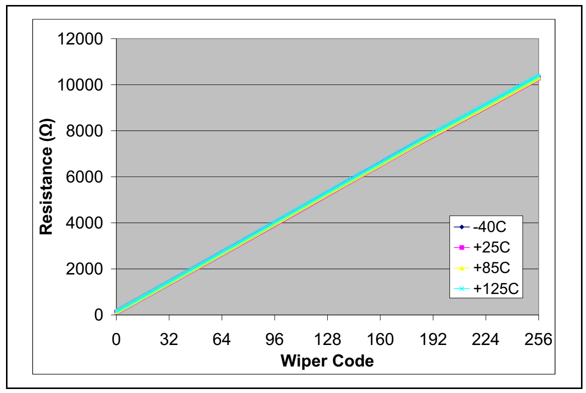
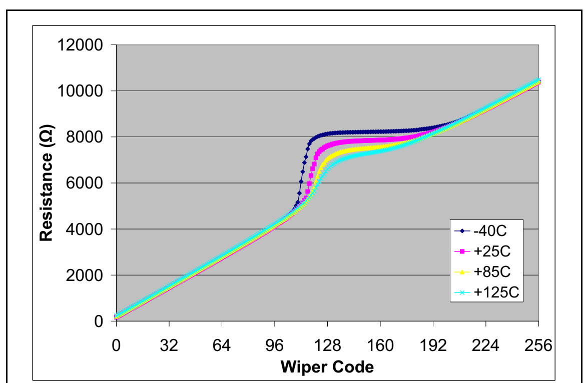


FIGURE 2-34: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 150 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-35: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 150 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

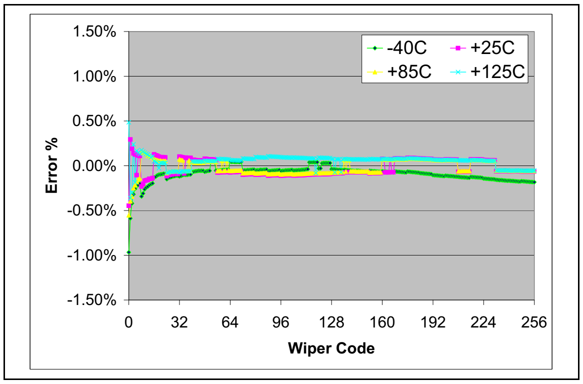


FIGURE 2-36: *10 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 5.5V, I_W = 150 µA).*

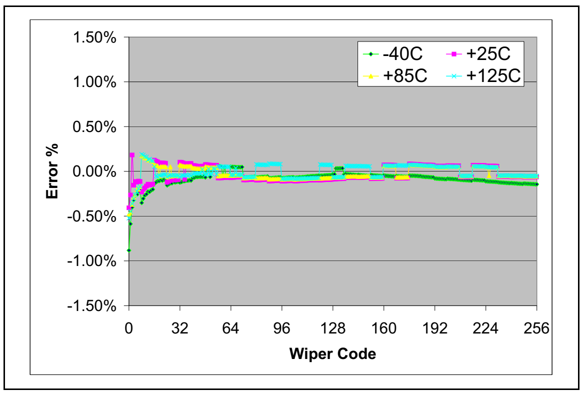
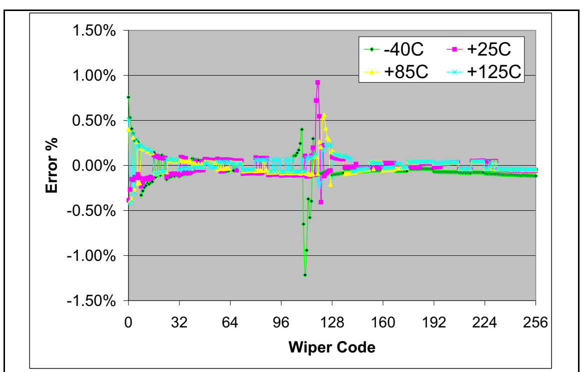


FIGURE 2-37: *10 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 3.0V, I_W = 150 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-38: *10 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 1.8V, I_W = 150 µA).*

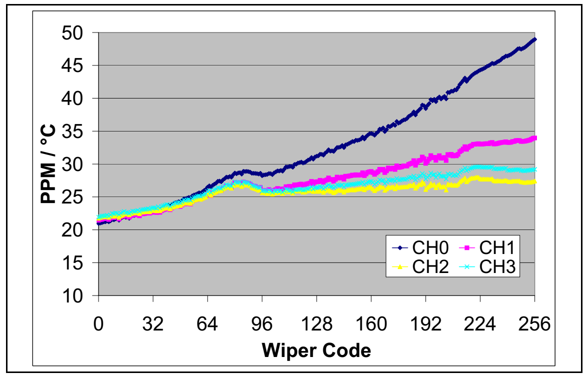


FIGURE 2-39: *10 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, I_W = 150 µA).*

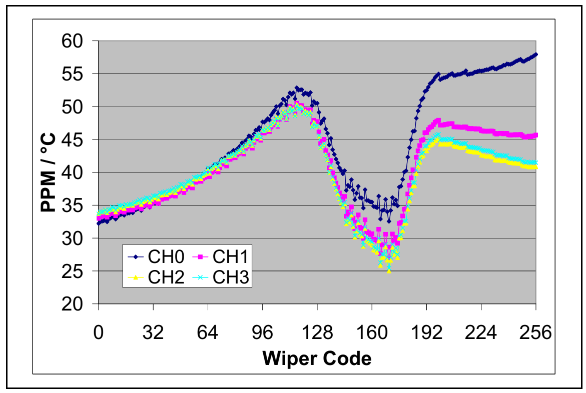
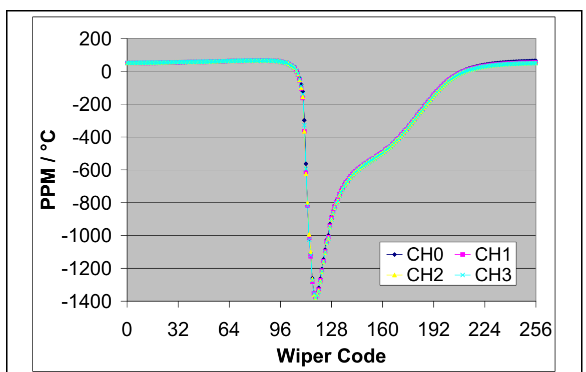


FIGURE 2-40: *10 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, I_W = 150 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-41: *10 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 1.8V, I_W = 150 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

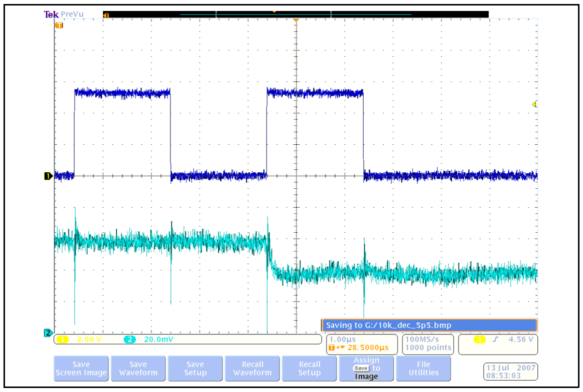


FIGURE 2-42: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

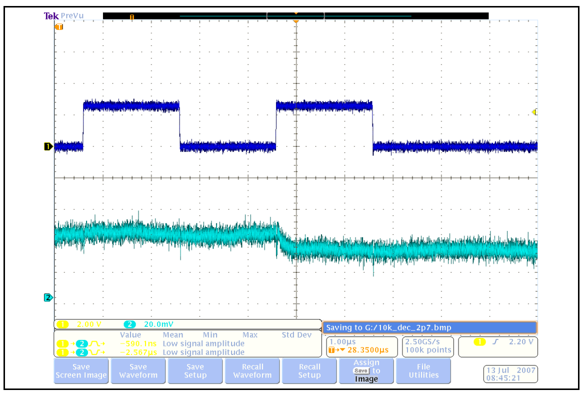


FIGURE 2-43: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

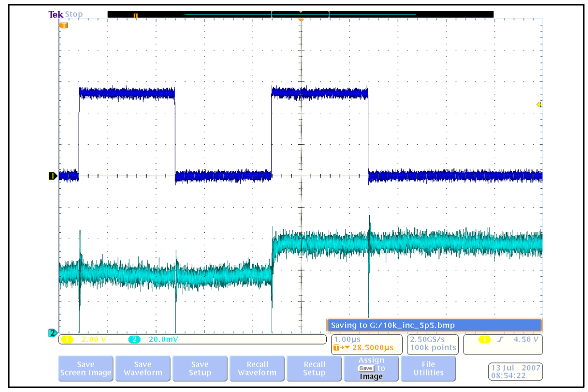


FIGURE 2-44: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

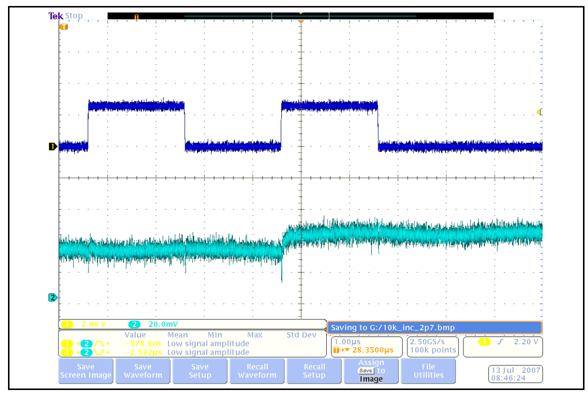


FIGURE 2-45: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

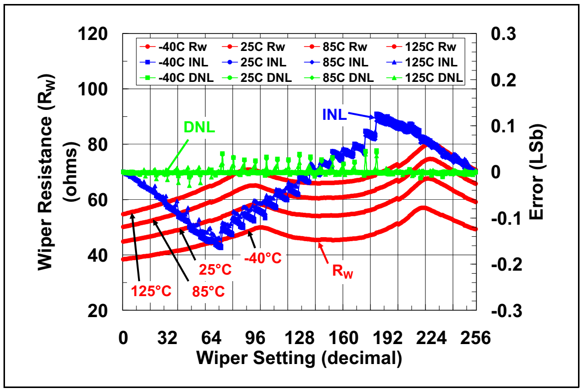


FIGURE 2-46: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

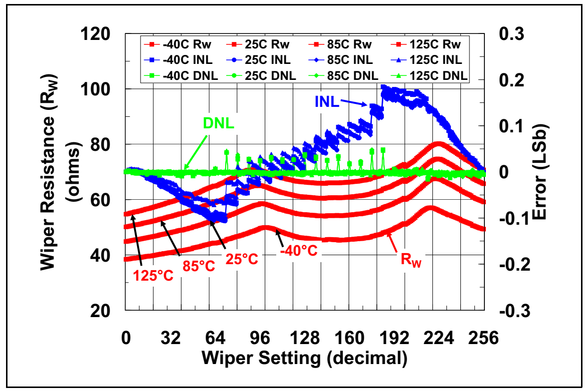


FIGURE 2-49: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 90 µA).*

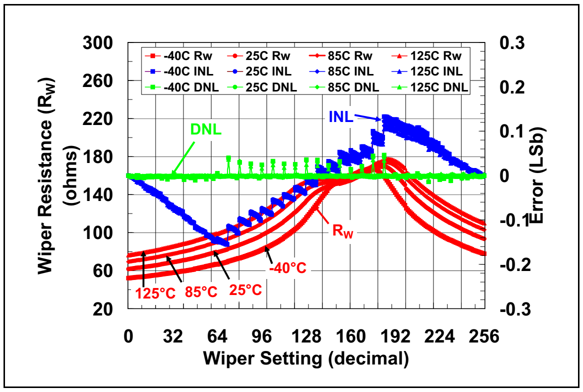


FIGURE 2-47: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

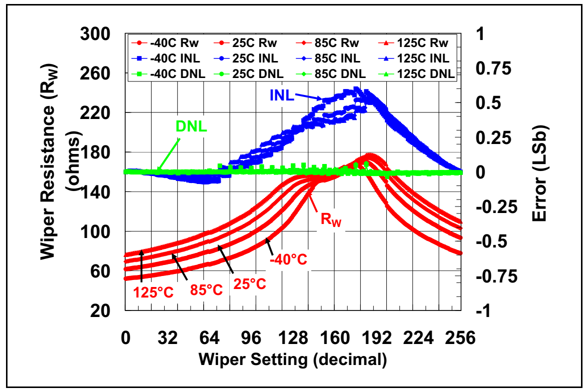
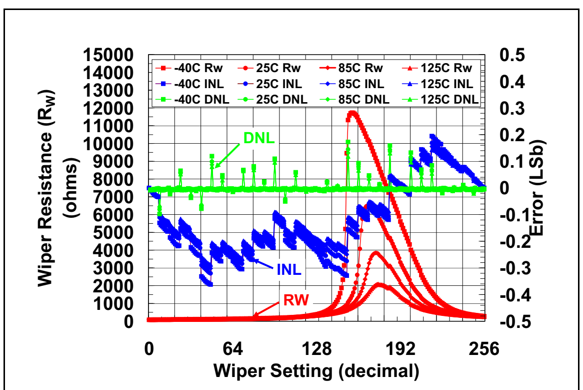
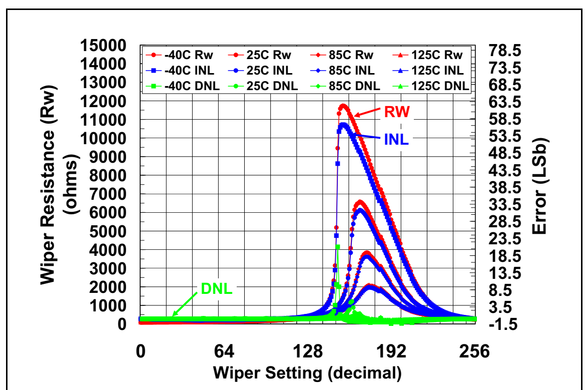


FIGURE 2-50: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 48 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-48: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-51: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 25 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

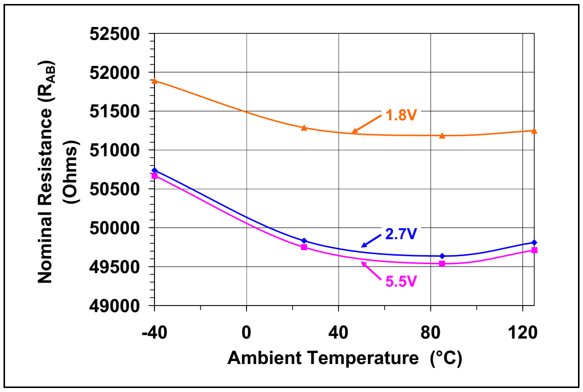


FIGURE 2-52: *50 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

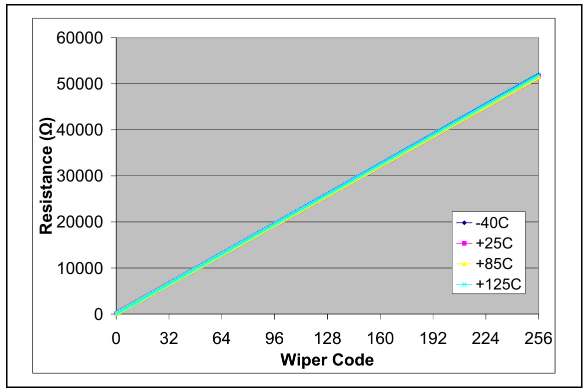


FIGURE 2-53: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 90 µA).*

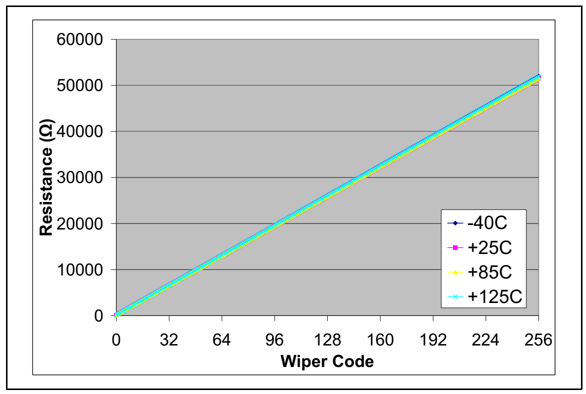
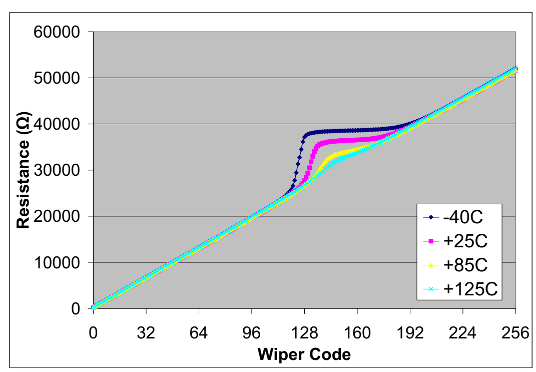


FIGURE 2-54: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 48 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-55: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 30 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

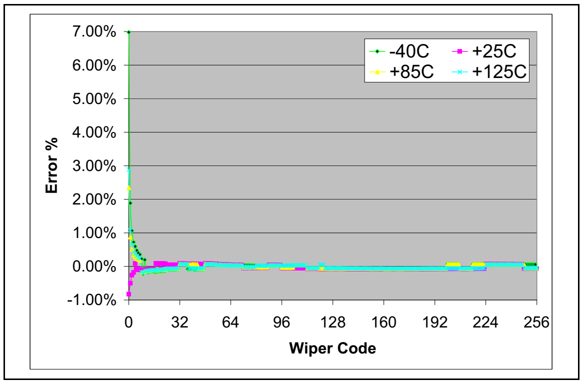


FIGURE 2-56: *50 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 5.5V, I_W = 90 µA).*

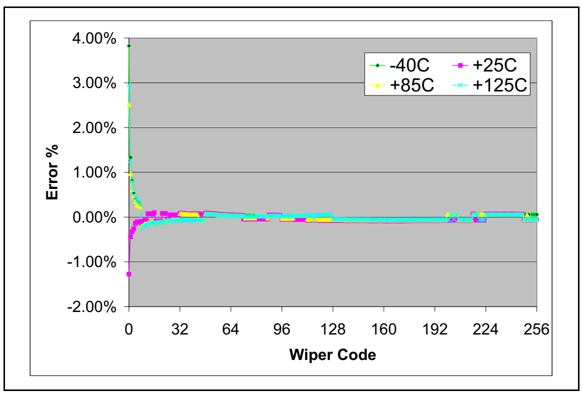
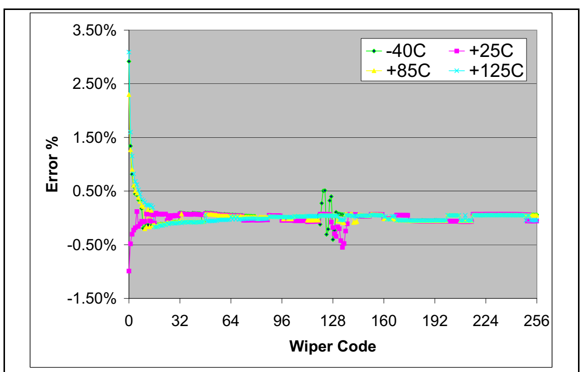


FIGURE 2-57: *50 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 3.0V, I_W = 48 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-58: *50 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 1.8V, I_W = 30 µA).*

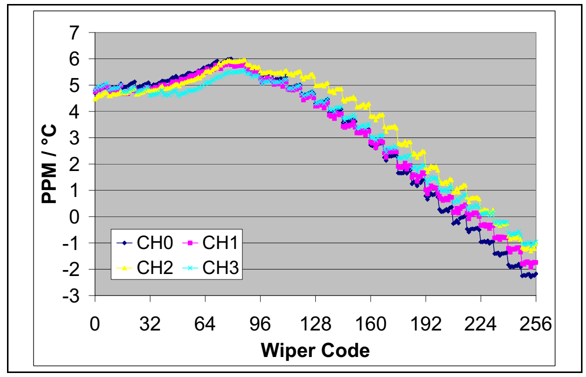


FIGURE 2-59: *50 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, I_W = 90 µA).*

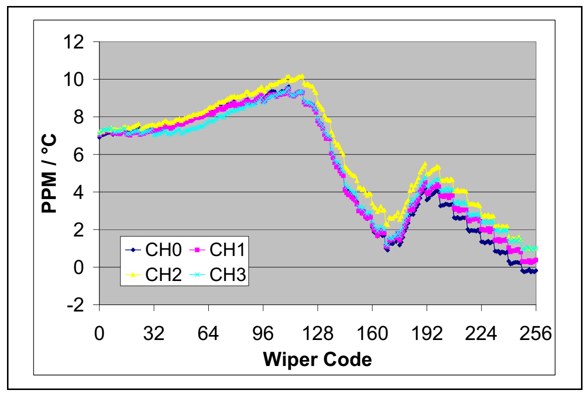
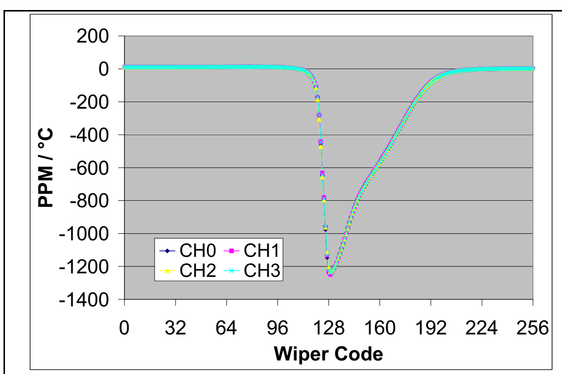


FIGURE 2-60: *50 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, I_W = 48 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-61: *50 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 1.8V, I_W = 30 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

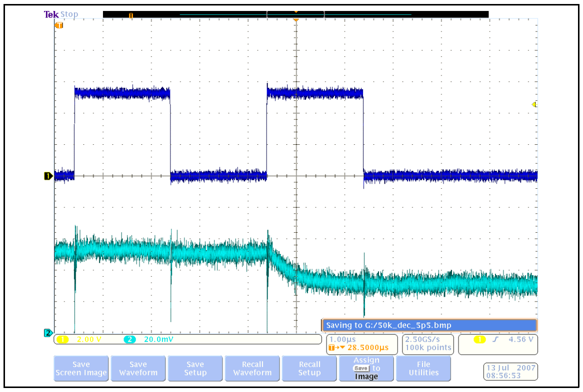


FIGURE 2-62: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

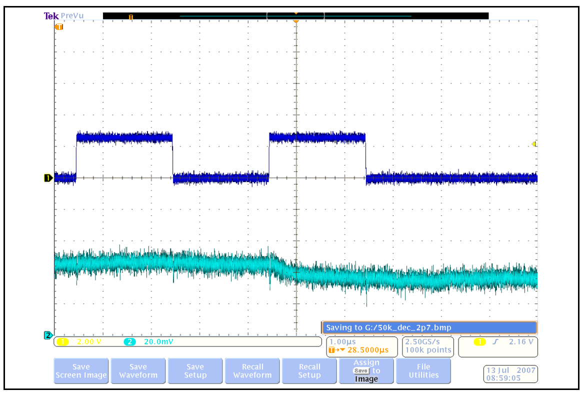


FIGURE 2-63: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

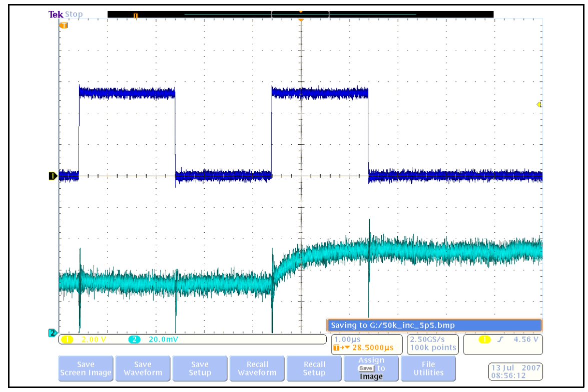


FIGURE 2-64: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

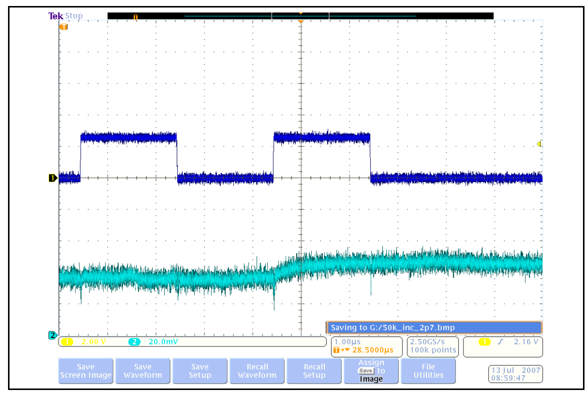


FIGURE 2-65: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

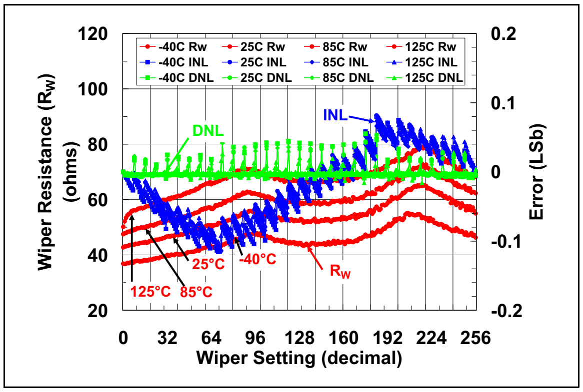


FIGURE 2-66: 100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

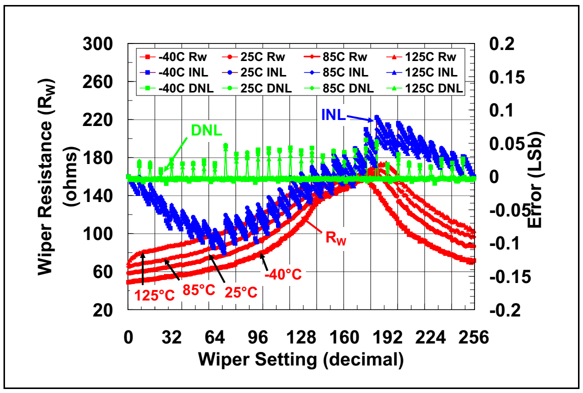
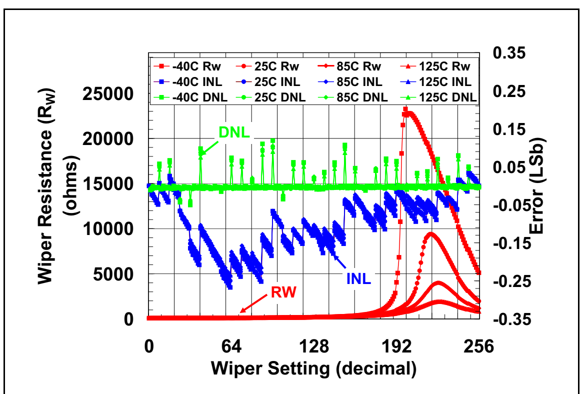


FIGURE 2-67: 100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-68: 100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

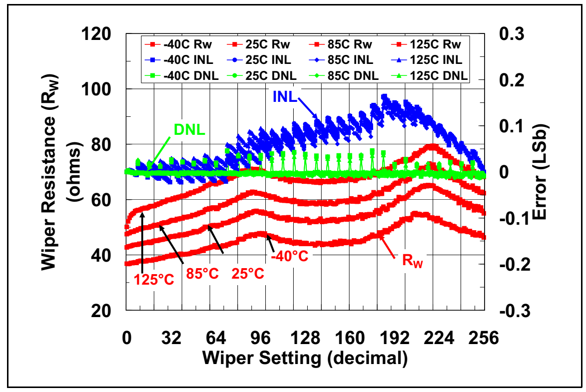


FIGURE 2-69: 100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 45 µA).

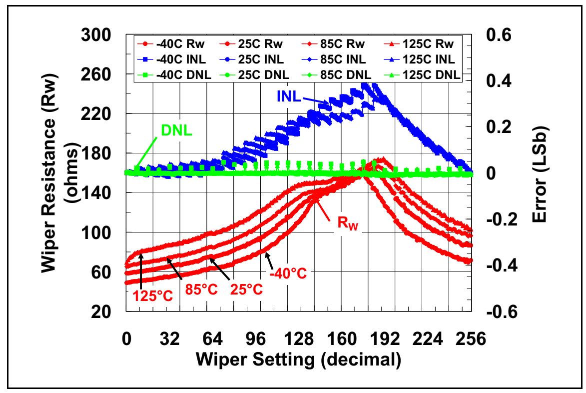
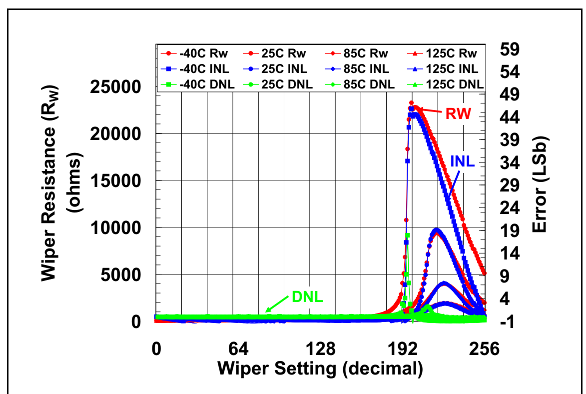


FIGURE 2-70: 100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 24 µA).



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-71: 100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 10 µA).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

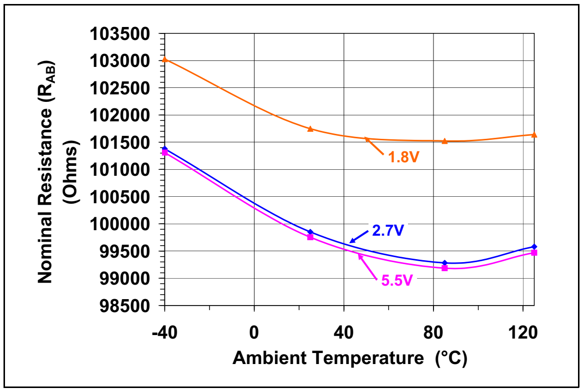


FIGURE 2-72: *100 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

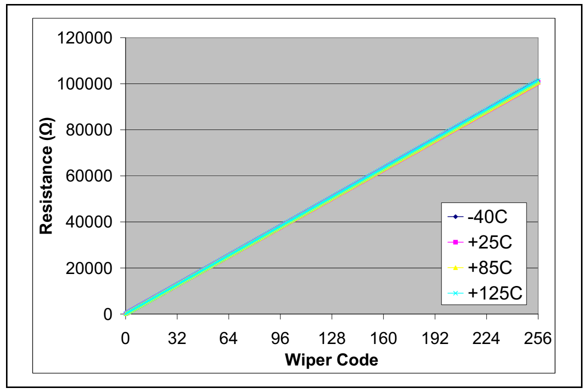


FIGURE 2-73: *100 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 45 µA).*

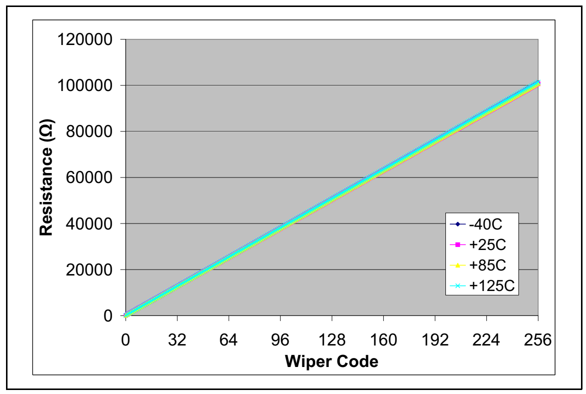
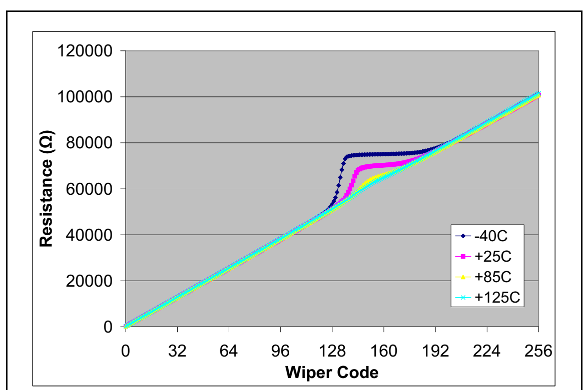


FIGURE 2-74: *100 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 24 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-75: *100 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 15 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

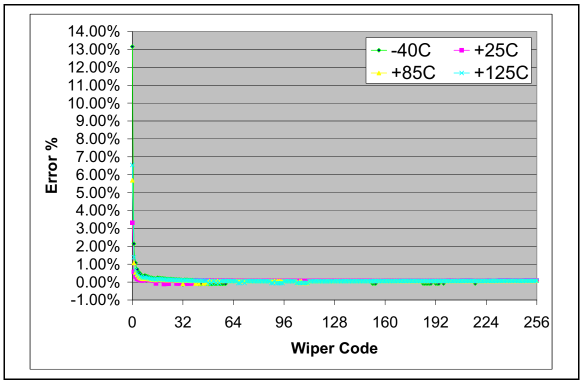


FIGURE 2-76: *100 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 5.5V, I_W = 45 µA).*

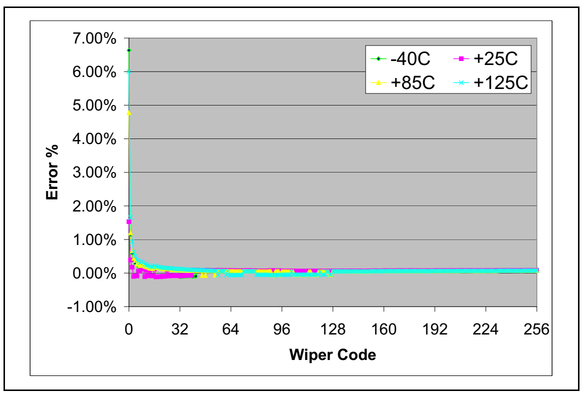
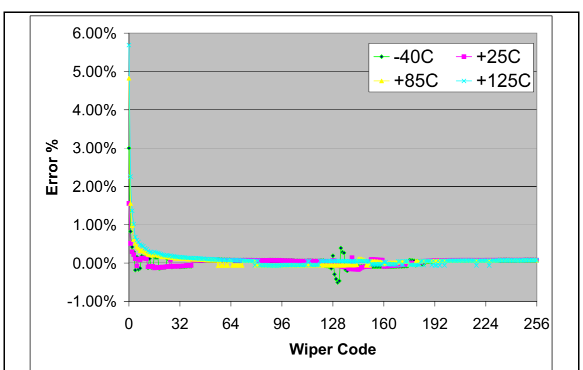


FIGURE 2-77: *100 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 3.0V, I_W = 24 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-78: *100 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 1.8V, I_W = 15 µA).*

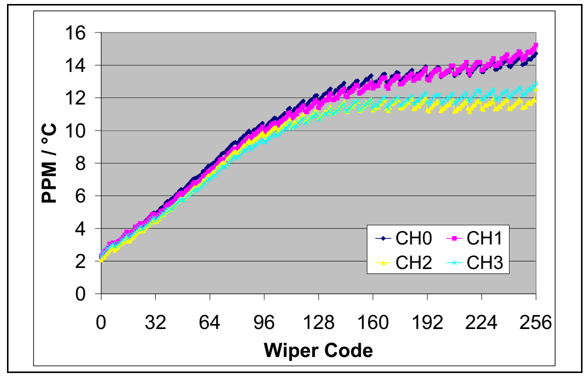


FIGURE 2-79: *100 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, I_W = 45 µA).*

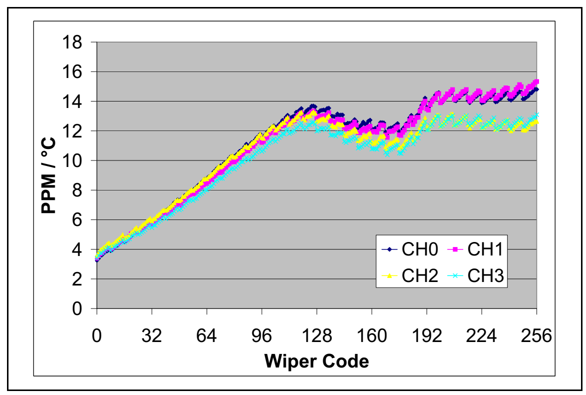
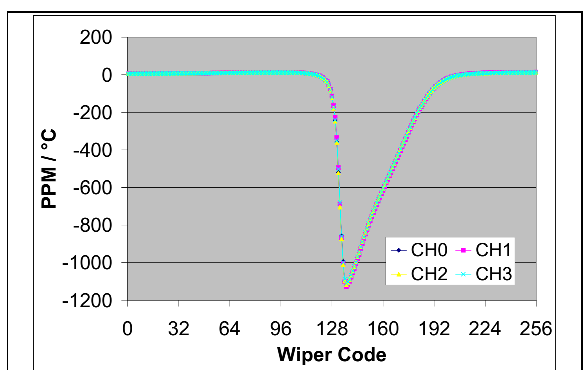


FIGURE 2-80: *100 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, I_W = 24 µA).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-81: *100 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 1.8V, I_W = 15 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

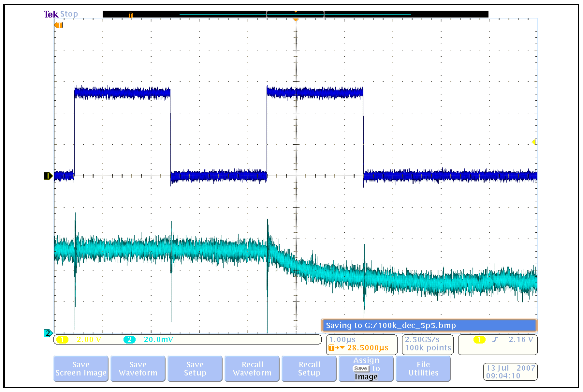


FIGURE 2-82: 100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).

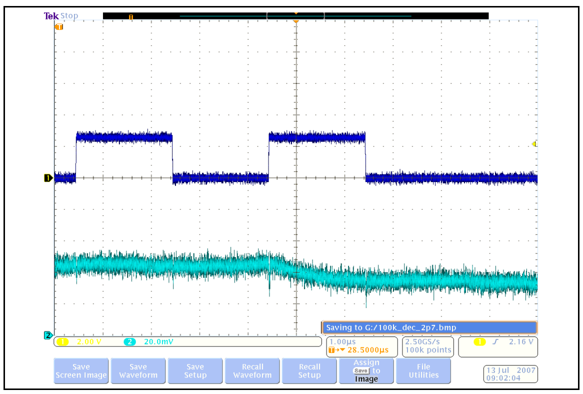


FIGURE 2-83: 100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).

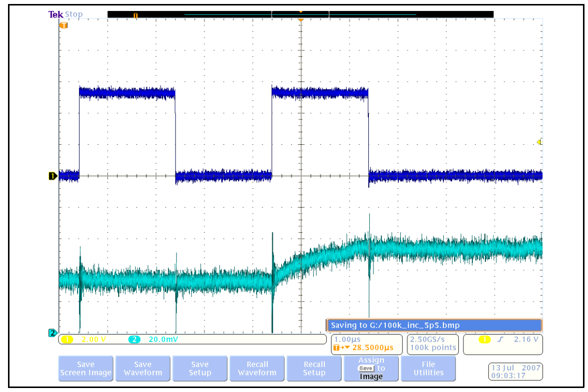


FIGURE 2-84: 100 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).

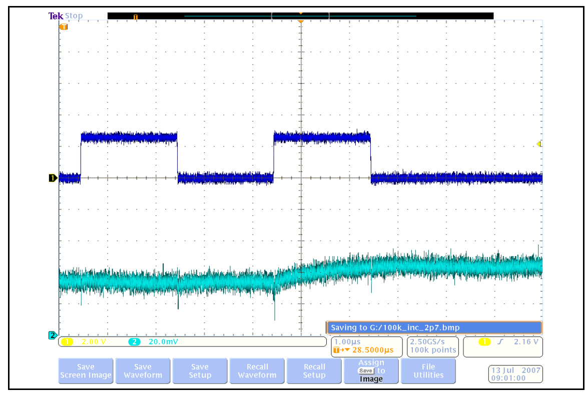


FIGURE 2-85: 100 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

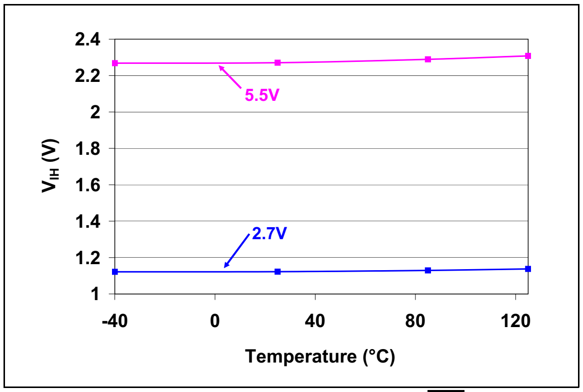


FIGURE 2-86: *V_{IH} (SDI, SCK, $\overline{CS}$, and $\overline{RESET}$) vs. V_{DD} and Temperature.*

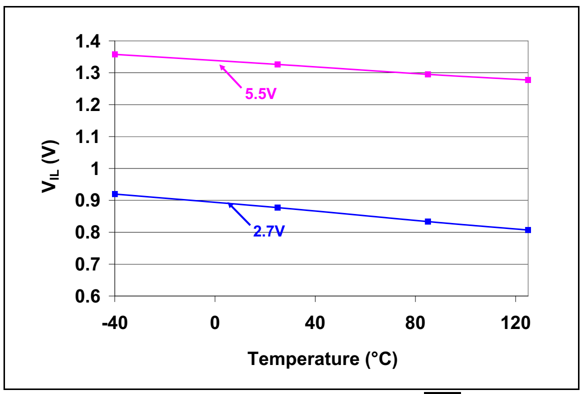


FIGURE 2-87: *V_{IL} (SDI, SCK, $\overline{CS}$, and $\overline{RESET}$) vs. V_{DD} and Temperature.*

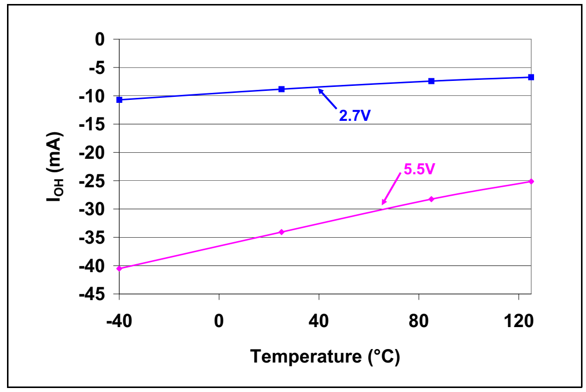


FIGURE 2-88: *I_{OH} (SDO) vs. V_{DD} and Temperature.*

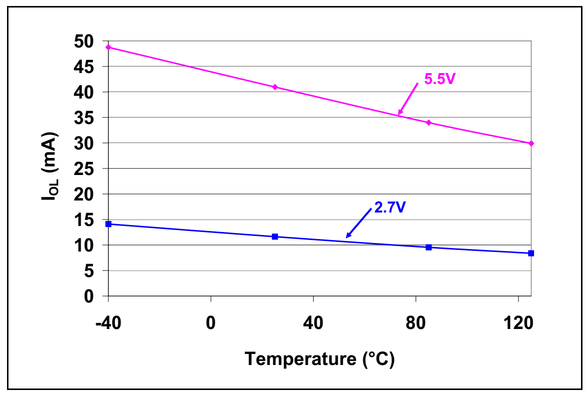


FIGURE 2-89: *I_{OL} (SDO) vs. V_{DD} and Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

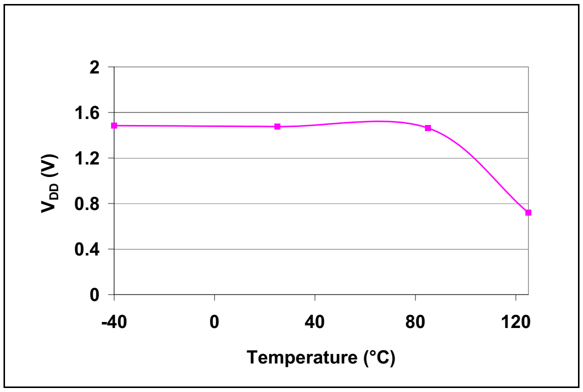


FIGURE 2-90: *POR/BOR Trip point vs. V_{DD} and Temperature.*

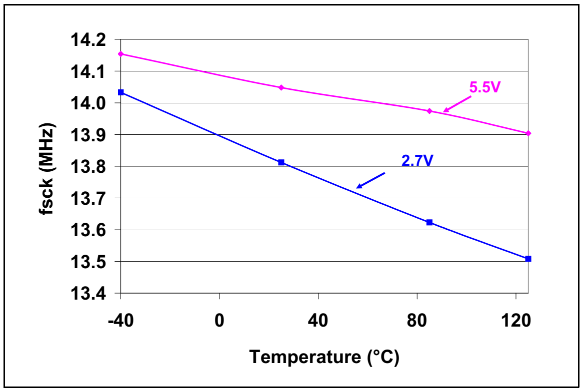


FIGURE 2-91: *SCK Input Frequency vs. Voltage and Temperature.*

2.1 Test Circuits

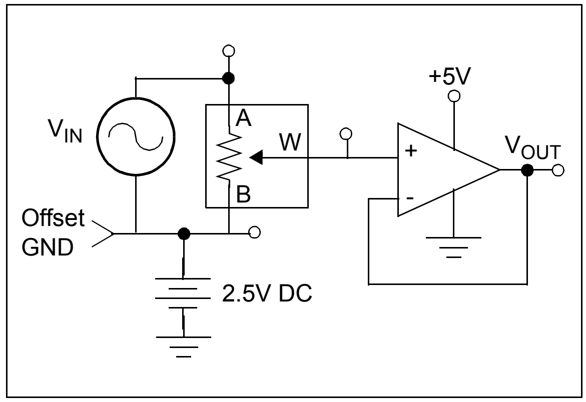


FIGURE 2-92: *-3 db Gain vs. Frequency Measurement.*

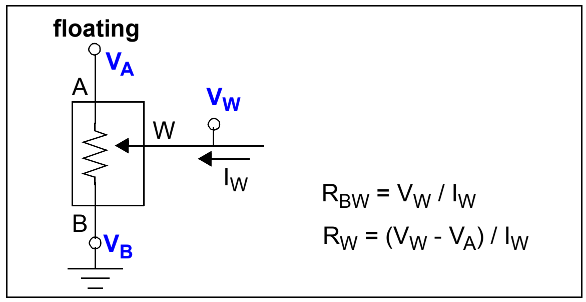


FIGURE 2-93: *R_{BW} and R_W Measurement.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1. Additional descriptions of the device pins follows.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP433X/435X

Pin						Weak Pull-up/ down (Note 1)	Standard Function
TSSOP		QFN	Symbol	I/O	Buffer Type		
14L	20L	20L					
—	1	19	P3A	A	Analog	No	Potentiometer 3 Terminal A
1	2	20	P3W	A	Analog	No	Potentiometer 3 Wiper Terminal
2	3	1	P3B	A	Analog	No	Potentiometer 3 Terminal B
3	4	2	$\overline{CS}$	I	HV w/ST	“smart”	SPI Chip Select Input
4	5	3	SCK	I	HV w/ST	“smart”	SPI Clock Input
5	6	4	SDI	I	HV w/ST	“smart”	SPI Serial Data Input
6	7	5	V_{SS}	—	P	—	Ground
7	8	6	P1B	A	Analog	No	Potentiometer 1 Terminal B
8	9	7	P1W	A	Analog	No	Potentiometer 1 Wiper Terminal
—	10	8	P1A	A	Analog	No	Potentiometer 1 Terminal A
—	11	9	P0A	A	Analog	No	Potentiometer 0 Terminal A
9	12	10	P0W	A	Analog	No	Potentiometer 0 Wiper Terminal
10	13	11	P0B	A	Analog	No	Potentiometer 0 Terminal B
—	14	12	NC	I	I	—	No Connect
—	15	13	$\overline{RESET}$	I	HV w/ST	Yes	Hardware Reset Pin
11	16	14	SDO	O	O	No	SPI Serial Data Output
12	17	15	V_{DD}	—	P	—	Positive Power Supply Input
13	18	16	P2B	A	Analog	No	Potentiometer 2 Terminal B
14	19	17	P2W	A	Analog	No	Potentiometer 2 Wiper Terminal
—	20	18	P2A	A	Analog	No	Potentiometer 2 Terminal A
—	—	21	EP	—	—	—	Exposed Pad. **(Note 2)**

Legend: HV w/ST = High Voltage tolerant input (with Schmitt trigger input)
A = Analog pins (Potentiometer terminals) I = digital input (high Z)
O = digital output I/O = Input / Output
P = Power

Note 1: The pin’s “smart” pull-up shuts off while the pin is forced low. This is done to reduce the standby and shutdown current.

2: The QFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device’s V_{SS} pin.

3.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is the serial interface’s chip select input. Forcing the $\overline{CS}$ pin to V_{IL} enables the serial commands. Forcing the $\overline{CS}$ pin to V_{IHH} enables the high-voltage serial commands.

3.2 Serial Clock (SCK)

The SCK pin is the serial interface's Serial Clock pin. This pin is connected to the host controllers SCK pin. The MCP43XX is an SPI slave device, so it’s SCK pin is an input only pin.

3.3 Serial Data In (SDI)

The SDI pin is the serial interfaces Serial Data In pin. This pin is connected to the host controllers SDO pin.

3.4 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer’s terminal B.

The potentiometer’s terminal B is the fixed connection to the zero scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between V_{SS} and V_{DD}.

MCP43XX devices have four terminal B pins, one for each resistor network.

3.6 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer’s terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between V_{SS} and V_{DD}.

MCP43XX devices have four terminal W pins, one for each resistor network.

3.7 Potentiometer Terminal A

The terminal A pin is available on the MCP43X1 devices, and is connected to the internal potentiometer’s terminal A.

The potentiometer’s terminal A is the fixed connection to the full scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x100 for 8-bit devices or 0x80 for 7-bit devices.

The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between V_{SS} and V_{DD}.

The terminal A pin is not available on the MCP43X2 devices, and the internally terminal A signal is floating.

MCP43X1 devices have four terminal A pins, one for each resistor network.

3.8 Not Connected (NC)

The NC pin is not used.

3.9 Reset ($\overline{RESET}$)

The $\overline{RESET}$ pin is used to force the device into the POR/BOR state.

3.10 Serial Data Out (SDO)

The SDO pin is the serial interfaces Serial Data Out pin. This pin is connected to the host controllers SDI pin.

This pin allows the host controller to read the digital potentiometers registers, or monitor the state of the command error bit.

3.11 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device’s positive power supply input. The input power supply is relative to V_{SS}.

While the devices V_{DD} is less than V_{min} (2.7V), the electrical performance of the device may not meet the data sheet specifications.

3.12 Exposed Pad (EP)

This pad is conductively connected to the device's substrate. This pad should be tied to the same potential as the V_{SS} pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.

4.0 FUNCTIONAL OVERVIEW

This data sheet covers a family of four volatile Digital Potentiometer and Rheostat devices that will be referred to as MCP43XX. The MCP43X1 devices are the Potentiometer configuration, while the MCP43X2 devices are the Rheostat configuration.

As the **Device Block Diagram** shows, there are four main functional blocks. These are:

- **POR/BOR and Reset Operation**
- **Memory Map**
- **Resistor Network**
- **Serial Interface (SPI)**

The POR/BOR operation and the Memory Map are discussed in this section and the Resistor Network and SPI operation are described in their own sections. The **Device Commands** are discussed in **Section 7.0**.

4.1 POR/BOR and Reset Operation

The Power-on Reset is the case where the device is having power applied to it from V_{SS}. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The devices RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the analog electrical performance may not meet the data sheet specifications. In this region, the device is capable of incrementing, decrementing, reading and writing to its volatile memory, if the proper serial command is executed.

When $V_{DD} < V_{POR}/V_{BOR}$ or the $\overline{\text{RESET}}$ pin is Low, the pin weak pull-ups are enabled.

4.1.1 POWER-ON RESET

When the device powers up, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage. Once the V_{DD} voltage crosses the V_{POR}/V_{BOR} voltage, the following happens:

- Volatile wiper register is loaded with the default value
- The TCON registers are loaded with their default value
- The device is capable of digital operation

4.1.2 BROWN-OUT RESET

When the device powers down, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage.

Once the V_{DD} voltage decreases below the V_{POR}/V_{BOR} voltage the following happens:

- Serial Interface is disabled

If the V_{DD} voltage decreases below the V_{RAM} voltage, the following happens:

- Volatile wiper registers may become corrupted
- TCON registers may become corrupted

As the voltage recovers above the V_{POR}/V_{BOR} voltage, the operation is the same as Power-on Reset (see **Section 4.1.1 "Power-on Reset"**).

Serial commands not completed due to a brown-out condition may cause the memory location to become corrupted.

4.1.3 $\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin can be used to force the device into the POR/BOR state of the device. When the $\overline{\text{RESET}}$ pin is forced Low, the device is forced into the Reset state. This means that the TCON registers are forced to their default values and the volatile wiper registers are loaded with the default value. Also the SPI interface is disabled.

This feature allows a hardware method for all registers to be updated to the default value at the same time.

4.1.4 INTERACTION OF $\overline{\text{RESET}}$ PIN AND BOR/POR CIRCUITRY

Figure 4-1 shows how the $\overline{\text{RESET}}$ pin signal and the POR/BOR signal interact to control the hardware Reset state of the device.

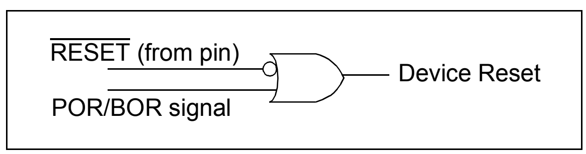


FIGURE 4-1: *POR/BOR Signal and $\overline{\text{RESET}}$ Pin Interaction.*

4.2 Memory Map

The device memory supports 16 locations that are 9-bits wide (16x9 bits). This memory space contains only volatile locations (see Table 4-2).

4.2.1 VOLATILE MEMORY (RAM)

There are six volatile memory locations. These are:

- Volatile Wiper 0
- Volatile Wiper 1
- Volatile Wiper 2
- Volatile Wiper 3
- Terminal Control (TCON0) Register 0
- Terminal Control (TCON)1 Register 1

The volatile memory starts functioning at the RAM retention voltage (V_{RAM}). The POR/BOR Wiper code is shown in Table 4-1.

TABLE 4-1: STANDARD SETTINGS

Resistance Code	Typical R_{AB} Value	Default POR Wiper Setting	Wiper Code 8-bit	Wiper Code 7-bit
-502	5.0 kΩ	Mid scale	80h	40h
-103	10.0 kΩ	Mid scale	80h	40h
-503	50.0 kΩ	Mid scale	80h	40h
-104	100.0 kΩ	Mid scale	80h	40h

TABLE 4-2: MEMORY MAP AND THE SUPPORTED COMMANDS

Address	Function	Memory Type	Allowed Commands	Disallowed Commands (1)	Factory Initialization	
00h	Volatile Wiper 0	RAM	Read, Write, Increment, Decrement	—	7-bit	040h
					8-bit	080h
01h	Volatile Wiper 1	RAM	Read, Write, Increment, Decrement	—	7-bit	040h
					8-bit	080h
02h	Reserved	—	None	All	—	
03h	Reserved	—	None	All	—	
04h	Volatile TCON0 Register	RAM	Read, Write	Increment, Decrement	1FFh	
05h	Reserved	—	None	All	—	
06h	Volatile Wiper 2	RAM	Read, Write, Increment, Decrement	—	7-bit	040h
					8-bit	080h
07h	Volatile Wiper 3	RAM	Read, Write, Increment, Decrement	—	7-bit	040h
					8-bit	080h
08h	Reserved	—	None	All	—	
09h	Reserved	—	None	All	—	
0Ah	Volatile TCON1 Register	RAM	Read, Write	Increment, Decrement	1FFh	
0Bh-0Fh	Reserved	—	None	All	—	

Note 1: This command on this address will generate an error condition. To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level and then back to the active state (V_{IL} or V_{IHH}).

4.2.1.1 Terminal Control (TCON) Registers

There are two Terminal Control (TCON) Registers. These are called TCON0 and TCON1. Each register contains 8 control bits. Four bits for each Wiper. Register 4-1 describes each bit of the TCON0 register, while Register 4-2 describes each bit of the TCON1 register.

The state of each resistor network terminal connection is individually controlled. That is, each terminal connection (A, B and W) can be individually connected/disconnected from the resistor network. This allows the system to minimize the currents through the digital potentiometer.

The value that is written to the specified TCON register will appear on the appropriate resistor network terminals when the serial command has completed.

On a POR/BOR these registers are loaded with 1FFh (9-bits), for all terminals connected. The host controller needs to detect the POR/BOR event and then update the volatile TCON register values.

REGISTER 4-1: TCON0 BITS (1)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
D8	R1HW	R1A	R1W	R1B	R0HW	R0A	R0W	R0B
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 8 **D8:** Reserved. Forced to “1”

bit 7 **R1HW:** Resistor 1 Hardware Configuration Control bit
This bit forces Resistor 1 into the “shutdown” configuration of the Hardware pin
1 = Resistor 1 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 1 is forced to the hardware pin “shutdown” configuration

bit 6 **R1A:** Resistor 1 Terminal A (P1A pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Terminal A to the Resistor 1 Network
1 = P1A pin is connected to the Resistor 1 Network
0 = P1A pin is disconnected from the Resistor 1 Network

bit 5 **R1W:** Resistor 1 Wiper (P1W pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Wiper to the Resistor 1 Network
1 = P1W pin is connected to the Resistor 1 Network
0 = P1W pin is disconnected from the Resistor 1 Network

bit 4 **R1B:** Resistor 1 Terminal B (P1B pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Terminal B to the Resistor 1 Network
1 = P1B pin is connected to the Resistor 1 Network
0 = P1B pin is disconnected from the Resistor 1 Network

bit 3 **R0HW:** Resistor 0 Hardware Configuration Control bit
This bit forces Resistor 0 into the “shutdown” configuration of the Hardware pin
1 = Resistor 0 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 0 is forced to the hardware pin “shutdown” configuration

bit 2 **R0A:** Resistor 0 Terminal A (P0A pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal A to the Resistor 0 Network
1 = P0A pin is connected to the Resistor 0 Network
0 = P0A pin is disconnected from the Resistor 0 Network

bit 1 **R0W:** Resistor 0 Wiper (P0W pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Wiper to the Resistor 0 Network
1 = P0W pin is connected to the Resistor 0 Network
0 = P0W pin is disconnected from the Resistor 0 Network

bit 0 **R0B:** Resistor 0 Terminal B (P0B pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal B to the Resistor 0 Network
1 = P0B pin is connected to the Resistor 0 Network
0 = P0B pin is disconnected from the Resistor 0 Network

Note 1: These bits do not affect the wiper register values.

REGISTER 4-2: TCON1 BITS (1)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
D8	R3HW	R3A	R3W	R3B	R2HW	R2A	R2W	R2B
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 8 **D8:** Reserved. Forced to “1”

bit 7 **R3HW:** Resistor 3 Hardware Configuration Control bit
This bit forces Resistor 3 into the “shutdown” configuration of the Hardware pin
1 = Resistor 3 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 3 is forced to the hardware pin “shutdown” configuration

bit 6 **R3A:** Resistor 3 Terminal A (P3A pin) Connect Control bit
This bit connects/disconnects the Resistor 3 Terminal A to the Resistor 3 Network
1 = P3A pin is connected to the Resistor 3 Network
0 = P3A pin is disconnected from the Resistor 3 Network

bit 5 **R3W:** Resistor 3 Wiper (P3W pin) Connect Control bit
This bit connects/disconnects the Resistor 3 Wiper to the Resistor 3 Network
1 = P3W pin is connected to the Resistor 3 Network
0 = P3W pin is disconnected from the Resistor 3 Network

bit 4 **R3B:** Resistor 3 Terminal B (P3B pin) Connect Control bit
This bit connects/disconnects the Resistor 3 Terminal B to the Resistor 3 Network
1 = P3B pin is connected to the Resistor 3 Network
0 = P3B pin is disconnected from the Resistor 3 Network

bit 3 **R2HW:** Resistor 2 Hardware Configuration Control bit
This bit forces Resistor 2 into the “shutdown” configuration of the Hardware pin
1 = Resistor 2 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 2 is forced to the hardware pin “shutdown” configuration

bit 2 **R2A:** Resistor 2 Terminal A (P0A pin) Connect Control bit
This bit connects/disconnects the Resistor 2 Terminal A to the Resistor 2 Network
1 = P2A pin is connected to the Resistor 2 Network
0 = P2A pin is disconnected from the Resistor 2 Network

bit 1 **R2W:** Resistor 2 Wiper (P0W pin) Connect Control bit
This bit connects/disconnects the Resistor 2 Wiper to the Resistor 2 Network
1 = P2W pin is connected to the Resistor 2 Network
0 = P2W pin is disconnected from the Resistor 2 Network

bit 0 **R2B:** Resistor 2 Terminal B (P2B pin) Connect Control bit
This bit connects/disconnects the Resistor 2 Terminal B to the Resistor 2 Network
1 = P2B pin is connected to the Resistor 2 Network
0 = P2B pin is disconnected from the Resistor 2 Network

Note 1: These bits do not affect the wiper register values.

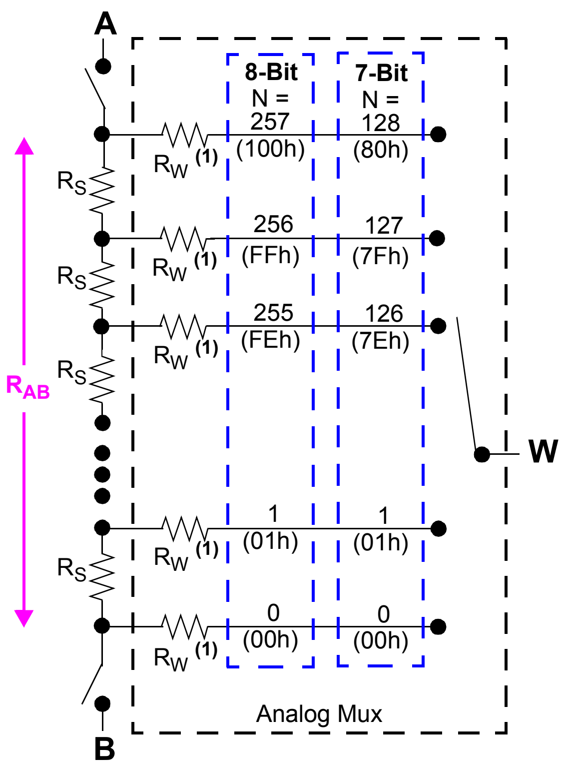
5.0 RESISTOR NETWORK

The Resistor Network has either 7-bit or 8-bit resolution. Each Resistor Network allows zero scale to full scale connections. Figure 5-1 shows a block diagram for the resistive network of a device.

The Resistor Network is made up of several parts. These include:

- Resistor Ladder
- Wiper
- Shutdown (Terminal Connections)

Devices have either four resistor networks. These are referred to as Pot 0, Pot 1, Pot 2 and Pot 3.



Note 1: The wiper resistance is dependent on several factors including, wiper code, device V_{DD}, Terminal voltages (on A, B and W), and temperature.
Also for the same conditions, each tap selection resistance has a small variation. This R_W variation has greater effects on some specifications (such as INL) for the smaller resistance devices (5.0 kΩ) compared to larger resistance devices (100.0 kΩ).

FIGURE 5-1: *Resistor Block Diagram.*

5.1 Resistor Ladder Module

The resistor ladder is a series of equal value resistors (R_S) with a connection point (tap) between the two resistors. The total number of resistors in the series (ladder) determines the R_{AB} resistance (see Figure 5-1). The end points of the resistor ladder are connected to analog switches which are connected to the device terminal A and terminal B pins. The R_{AB} (and R_S) resistance has small variations over voltage and temperature.

For an 8-bit device, there are 256 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 256 resistors thus providing 257 possible settings (including terminal A and terminal B).

For a 7-bit device, there are 128 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 128 resistors thus providing 129 possible settings (including terminal A and terminal B).

Equation 5-1 shows the calculation for the step resistance.

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{AB}}{(256)}$$ 8-bit Device

$$R_S = \frac{R_{AB}}{(128)}$$ 7-bit Device

5.2 Wiper

Each tap point (between the R_S resistors) is a connection point for an analog switch. The opposite side of the analog switch is connected to a common signal which is connected to the Terminal W (Wiper) pin.

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The wiper can connect directly to Terminal B or to Terminal A. A zero scale connection, connects the Terminal W (wiper) to Terminal B (wiper setting of 000h). A full scale connection, connects the Terminal W (wiper) to Terminal A (wiper setting of 100h or 80h). In these configurations the only resistance between the Terminal W and the other Terminal (A or B) is that of the analog switches.

A wiper setting value greater than full scale (wiper setting of 100h for 8-bit device or 80h for 7-bit devices) will also be a full scale setting (Terminal W (wiper) connected to Terminal A). Table 5-1 illustrates the full wiper setting map.

Equation 5-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.

EQUATION 5-2: R_{WB} CALCULATION

$$R_{WB} = \frac{R_{AB}N}{(256)} + R_W$$ 8-bit Device

N = 0 to 256 (decimal)

$$R_{WB} = \frac{R_{AB}N}{(128)} + R_W$$ 7-bit Device

N = 0 to 128 (decimal)

TABLE 5-1: VOLATILE WIPER VALUE VS. WIPER POSITION MAP

Wiper Setting		Properties
7-bit	8-bit	
3FFh-081h	3FFh-101h	Reserved (Full Scale (W = A)), Increment and Decrement commands ignored
080h	100h	Full Scale (W = A), Increment commands ignored
07Fh-041h	0FFh-081h	W = N
040h	080h	W = N (Mid Scale)
03Fh-001h	07Fh-001h	W = N
000h	000h	Zero Scale (W = B) Decrement command ignored

5.3 Shutdown

Shutdown is used to minimize the device's current consumption. The MCP43XX has one method to achieve this:

- **Terminal Control Register (TCON)**

This is different from the MCP42XXX devices in that the Hardware Shutdown pin ($\overline{SHDN}$) has been replaced by a $\overline{RESET}$ pin. The Hardware Shutdown pin function is still available via software commands to the TCON register.

5.3.1 TERMINAL CONTROL REGISTER (TCON)

The Terminal Control (TCON) register is a volatile register used to configure the connection of each resistor network terminal pin (A, B and W) to the Resistor Network. These registers are shown in Register 4-1 and Register 4-2.

The RxHW bit forces the selected resistor network into the same state as the MCP42X1's $\overline{SHDN}$ pin. Alternate low-power configurations may be achieved with the RxA, RxW and RxB bits.

When the RxHW bit is "`0`":

- The P0A, P1A, P2A and P3A terminals are disconnected
- The P0W, P1W, P2W and P3W terminals are simultaneously connect to the P0B, P1B, P2B and P3B terminals, respectively (see Figure 5-2)

Note:	When the RxHW bit forces the resistor network into the hardware $\overline{SHDN}$ state, the state of the TCON0 or TCON1 register's RxA, RxW and RxB bits is overridden (ignored). When the state of the RxHW bit no longer forces the resistor network into the hardware $\overline{SHDN}$ state, the TCON0 or TCON1 register's RxA, RxW and RxB bits return to controlling the terminal connection state. In other words, the RxHW bit does not corrupt the state of the RxA, RxW and RxB bits.

The RxHW bit does NOT corrupt the values in the Volatile Wiper Registers nor the TCON register. When the Shutdown mode is exited (RxHW bit = `1`):

- The device returns to the Wiper setting specified by the Volatile Wiper value
- The TCON register bits return to controlling the terminal connection state

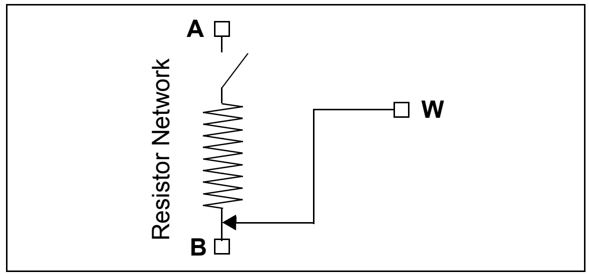


FIGURE 5-2: *Resistor Network Shutdown State (RxHW = `0`).*

NOTES:

6.0 SERIAL INTERFACE (SPI)

The MCP43XX devices support the SPI serial protocol. This SPI operates in the Slave mode (does not generate the serial clock).

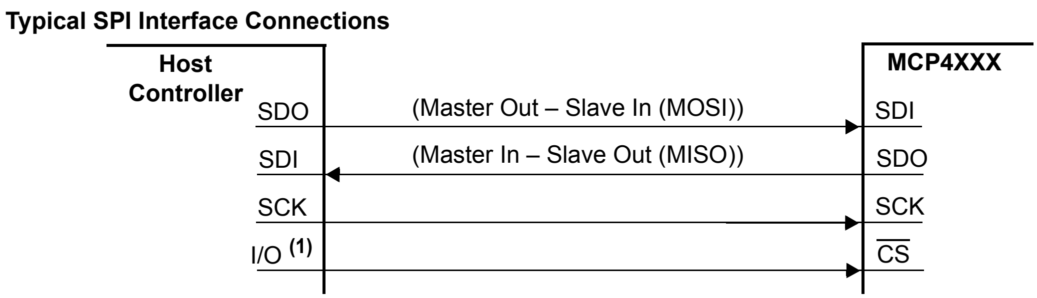
The SPI interface uses up to four pins. These are:

- $\overline{\text{CS}}$ – Chip Select
- SCK – Serial Clock
- SDI – Serial Data In
- SDO – Serial Data Out

Typical SPI Interface is shown in Figure 6-1. In the SPI interface, the Master's Output pin is connected to the Slave's Input pin and the Master's Input pin is connected to the Slave's Output pin.

The MCP4XXX SPI's module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) on the when the $\overline{\text{CS}}$ pin transitions from inactive (V_{IH}) to active (V_{IL} or V_{IHH}).

All SPI interface signals are high-voltage tolerant.



Note 1: If high voltage commands are desired, some type of external circuitry needs to be implemented.

FIGURE 6-1: *Typical SPI Interface Block Diagram.*

6.1 SDI, SDO, SCK, and $\overline{\text{CS}}$ Operation

The operation of the four SPI interface pins are discussed in this section. These pins are:

- SDI (Serial Data In)
- SDO (Serial Data Out)
- SCK (Serial Clock)
- $\overline{\text{CS}}$ (Chip Select)

The serial interface works on either 8-bit or 16-bit boundaries depending on the selected command. The Chip Select ($\overline{\text{CS}}$) pin frames the SPI commands.

6.1.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal into the device. The value on this pin is latched on the rising edge of the SCK signal.

6.1.2 SERIAL DATA OUT (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{\text{CS}}$ pin is forced to the active level (V_{IL} or V_{IHH}), the SDO pin will be driven. The state of the SDO pin is determined by the serial bit's position in the command, the command selected, and if there is a command error state (CMDERR).

6.1.3 SERIAL CLOCK (SCK) (SPI FREQUENCY OF OPERATION)

The SPI interface is specified to operate up to 10 MHz. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency.

TABLE 6-1: SCK FREQUENCY (1)

Memory Type Access		Command	
		Read	**Write, Increment, Decrement**
Volatile Memory	SDI, SDO	10 MHz	10 MHz

Note 1: This is the maximum clock frequency without an external pull-up resistor.

6.1.4 THE $\overline{\text{CS}}$ SIGNAL

The Chip Select ($\overline{\text{CS}}$) signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{\text{CS}}$ signal must transition from the inactive state (V_{IH}) to an active state (V_{IL} or V_{IHH}).

After the $\overline{\text{CS}}$ signal has gone active, the SDO pin is driven and the clock bit counter is reset.

> **Note:** There is a required delay after the $\overline{\text{CS}}$ pin goes active to the 1st edge of the SCK pin.

If an error condition occurs for an SPI command, then the command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the $\overline{\text{CS}}$ pin to the V_{IH} level.

When the $\overline{\text{CS}}$ pin returns to the inactive state (V_{IH}) the SPI module resets (including the Address Pointer). While the $\overline{\text{CS}}$ pin is in the inactive state (V_{IH}), the serial interface is ignored. This allows the host controller to interface to other SPI devices using the same SDI, SDO and SCK signals.

The $\overline{\text{CS}}$ pin has an internal pull-up resistor. The resistor is disabled when the voltage on the $\overline{\text{CS}}$ pin is at the V_{IL} level. This means that when the $\overline{\text{CS}}$ pin is not driven, the internal pull-up resistor will pull this signal to the V_{IH} level. When the $\overline{\text{CS}}$ pin is driven low (V_{IL}), the resistance becomes very large to reduce the device current consumption.

The high voltage capability of the $\overline{\text{CS}}$ pin allows High Voltage commands. Support of High Voltage commands allows circuit compatibility with the corresponding nonvolatile device.

6.2 The SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The mode is determined by the state of the SDI pin on the rising edge of the 1st clock bit (of the 8-bit byte).

6.2.1 MODE 0,0

In **Mode 0,0**: SCK Idle state = low (V_{IL}), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

6.2.2 MODE 1,1

In **Mode 1,1**: SCK Idle state = high (V_{IH}), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

6.3 SPI Waveforms

Figure 6-2 through Figure 6-5 show the different SPI command waveforms. Figure 6-2 and Figure 6-3 are read and write commands. Figure 6-4 and Figure 6-5 are Increment and Decrement commands. Support of High Voltage commands allows circuit compatibility with the corresponding nonvolatile device.

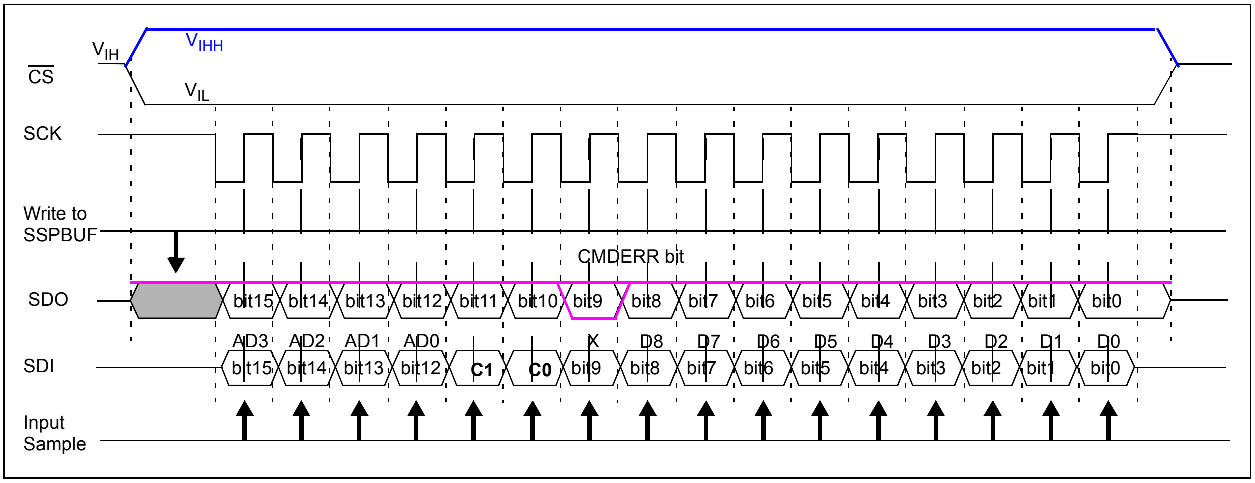


FIGURE 6-2: *16-Bit Commands (Write, Read) – SPI Waveform (Mode 1,1).*

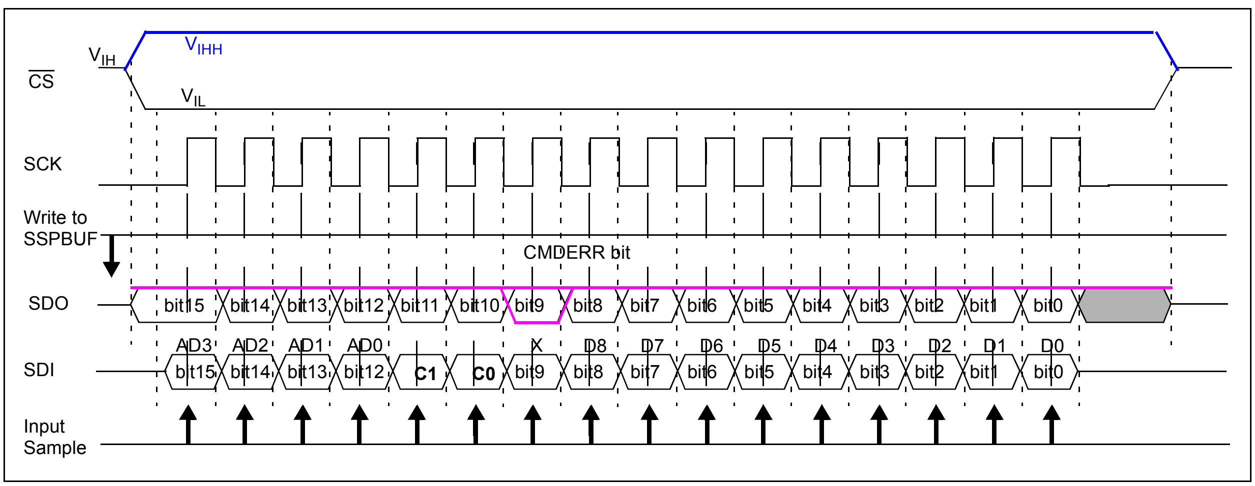


FIGURE 6-3: *16-Bit Commands (Write, Read) – SPI Waveform (Mode 0,0).*

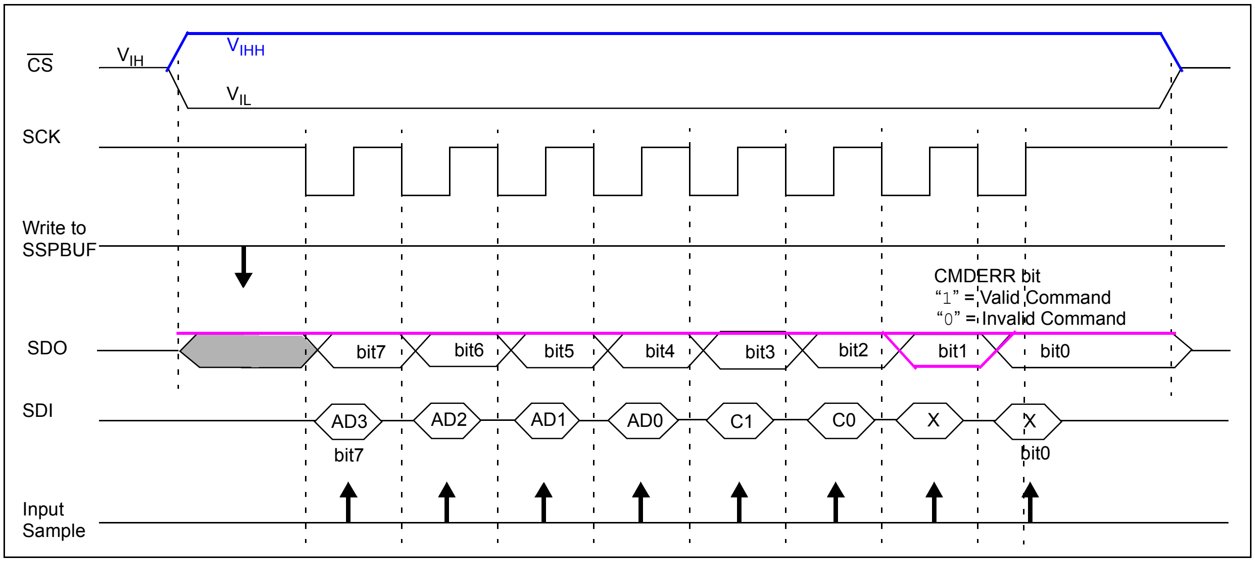


FIGURE 6-4: *8-Bit Commands (Increment, Decrement) – SPI Waveform with PIC MCU (Mode 1,1).*

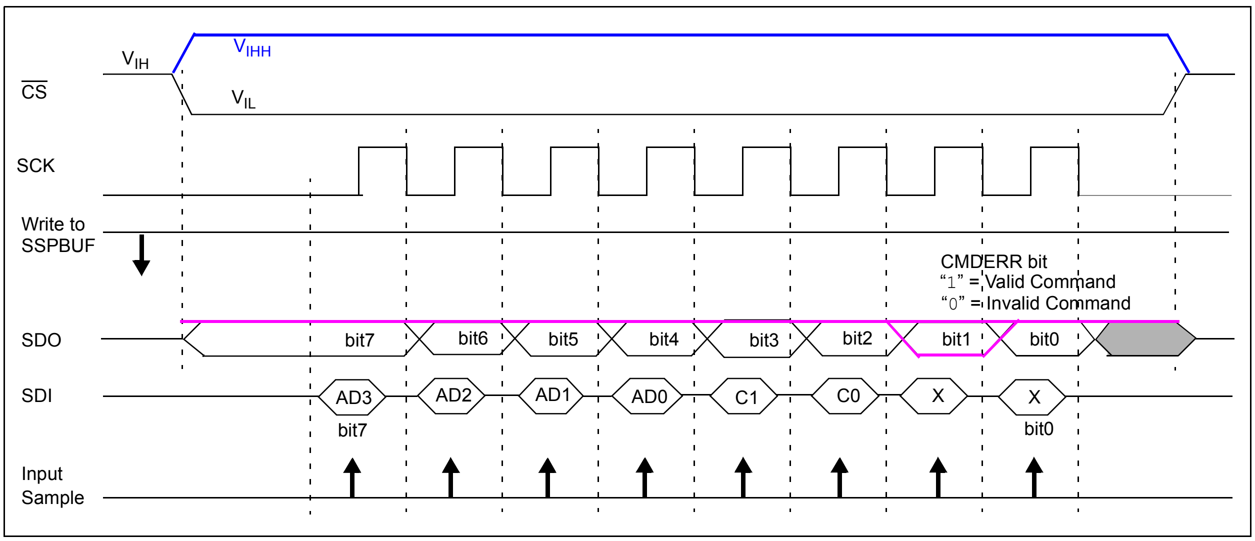


FIGURE 6-5: *8-Bit Commands (Increment, Decrement) – SPI Waveform with PIC MCU (Mode 0,0).*

7.0 DEVICE COMMANDS

The MCP43XX's SPI command format supports 16 memory address locations and four commands. Each command has two modes:

- Normal Serial Commands
- High-Voltage Serial Commands

Normal serial commands are those where the $\overline{CS}$ pin is driven to V_{IL}. With high-voltage serial commands, the $\overline{CS}$ pin is driven to V_{IHH}. In each mode, there are four possible commands. These commands are shown in Table 7-1.

The 8-bit commands (**Increment Wiper** and **Decrement Wiper** commands) contain a command byte, see Figure 7-1, while 16-bit commands (**Read Data** and **Write Data** commands) contain a command byte and a data byte. The command byte contains two data bits, see Figure 7-1.

Table 7-2 shows the supported commands for each memory location and the corresponding values on the SDI and SDO pins.

Table 7-3 shows an overview of all the SPI commands and their interaction with other device features.

7.1 Command Byte

The command byte has three fields, the address, the command, and 2 data bits, see Figure 7-1. Currently only one of the data bits is defined (D8). This is for the Write command.

The device memory is accessed when the master sends a proper command byte to select the desired operation. The memory location getting accessed is contained in the command byte's AD3:AD0 bits. The action desired is contained in the command byte's C1:C0 bits, see Table 7-1. C1:C0 determines if the desired memory location will be read, written, incremented (wiper setting +1) or decremented (wiper setting -1). The Increment and Decrement commands are only valid on the volatile wiper registers.

As the command byte is being loaded into the device (on the SDI pin), the device's SDO pin is driving. The SDO pin will output high bits for the first six bits of that command. On the 7th bit, the SDO pin will output the CMDERR bit state (see **Section 7.3 "Error Condition"**). The 8th bit state depends on the command selected.

TABLE 7-1: COMMAND BIT OVERVIEW

C1:C0 Bit States	Command	# of Bits	Operates on Volatile/ Nonvolatile memory
11	Read Data	16-Bits	Both
00	Write Data	16-Bits	Both
01	Increment	8-Bits	Volatile Only
10	Decrement	8-Bits	Volatile Only

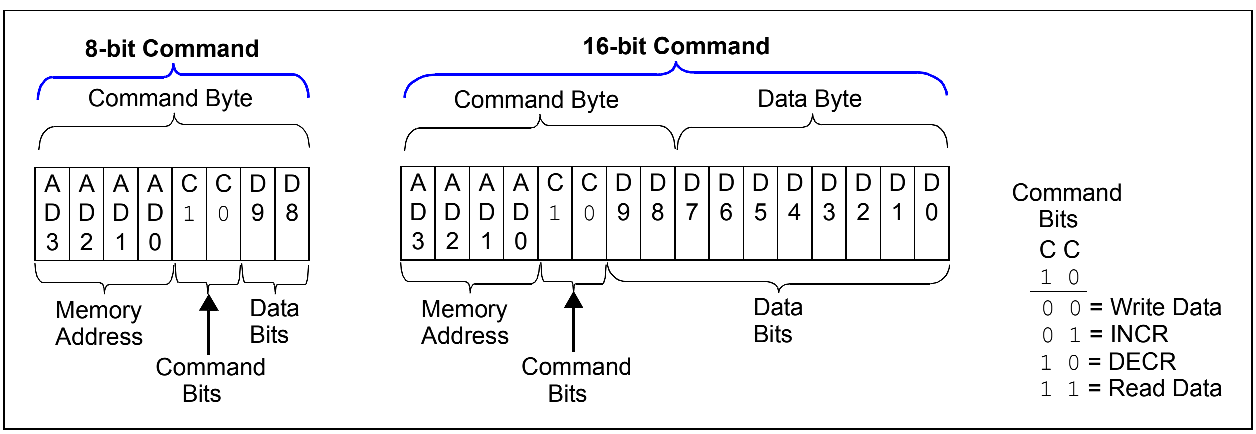


FIGURE 7-1: *General SPI Command Formats.*

TABLE 7-2: MEMORY MAP AND THE SUPPORTED COMMANDS

Address		Command	Data (10-bits) (1)	SPI String (Binary)	
Value	Function			MOSI (SDI pin)	MISO (SDO pin) (2)
00h	Volatile Wiper 0	Write Data	nn nnnn nnnn	0000 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0000 11nn nnnn nnnn	1111 111n nnnn nnnn
		Increment Wiper	—	0000 0100	1111 1111
		Decrement Wiper	—	0000 1000	1111 1111
01h	Volatile Wiper 1	Write Data	nn nnnn nnnn	0001 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0001 11nn nnnn nnnn	1111 111n nnnn nnnn
		Increment Wiper	—	0001 0100	1111 1111
		Decrement Wiper	—	0001 1000	1111 1111
02h	Reserved	None	—	—	—
03h	Reserved	None	—	—	—
04h (3)	Volatile TCON 0 Register	Write Data	nn nnnn nnnn	0100 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0100 11nn nnnn nnnn	1111 111n nnnn nnnn
05h	Reserved	None	—	—	—
06h	Volatile Wiper 2	Write Data	nn nnnn nnnn	0110 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0110 11nn nnnn nnnn	1111 111n nnnn nnnn
		Increment Wiper	—	0110 0100	1111 1111
		Decrement Wiper	—	0110 1000	1111 1111
07h	Volatile Wiper 3	Write Data	nn nnnn nnnn	0111 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0111 11nn nnnn nnnn	1111 111n nnnn nnnn
		Increment Wiper	—	0111 0100	1111 1111
		Decrement Wiper	—	0111 1000	1111 1111
08h	Reserved	None	—	—	—
09h	Reserved	None	—	—	—
0Ah (3)	Volatile TCON 1 Register	Write Data	nn nnnn nnnn	1010 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	1010 11nn nnnn nnnn	1111 111n nnnn nnnn
0Bh-0Fh	Reserved	None	—	—	—

Note 1: The data memory is only 9-bits wide, so the MSb is ignored by the device.
2: All these address/command combinations are valid, so the CMDERR bit is set. Any other address/command combination is a command error state and the CMDERR bit will be clear.
3: Increment or Decrement commands are invalid for these addresses.

7.2 Data Byte

Only the Read command and the Write command use the data byte, see Figure 7-1. These commands concatenate the 8 bits of the data byte with the one data bit (D8) contained in the command byte to form 9-bits of data (D8:D0). The command byte format supports up to 9-bits of data so that the 8-bit resistor network can be set to full scale (100h or greater). This allows wiper connections to Terminal A and to Terminal B.

The D9 bit is currently unused, and corresponds to the position on the SDO data of the CMDERR bit.

7.3 Error Condition

The CMDERR bit indicates if the four address bits received (AD3:AD0) and the two command bits received (C1:C0) are a valid combination (see Table 4-2). The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The command error bit will also be low if a write to a nonvolatile address has been specified and another SPI command occurs before the $\overline{CS}$ pin is driven inactive (V_{IH}).

SPI commands that do not have a multiple of 8 clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the inactive state (V_{IH}).

7.3.1 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks have been received. Some commands also require the $\overline{CS}$ pin to be forced inactive (V_{IH}). If the $\overline{CS}$ pin is forced to the inactive state (V_{IH}) the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that this noise corrupts the value of the data being clocked into the MCP43XX or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device, or a command error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the active state is detected (V_{IH} to V_{IL} or V_{IH} to V_{IHH}).

Note 1:	When data is not being received by the MCP43XX, It is recommended that the $\overline{CS}$ pin be forced to the inactive level (V_{IL})
2:	It is also recommended that long continuous command strings should be broken down into single commands or shorter continuous command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI commands.

7.4 Continuous Commands

The device supports the ability to execute commands continuously. While the $\overline{CS}$ pin is in the active state (V_{IL} or V_{IHH}). Any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin driven active (V_{IL} or V_{IHH}).
2. Read Command.
3. Increment Command (Wiper 0).
4. Increment Command (Wiper 0).
5. Decrement Command (Wiper 1).
6. Write Command (volatile memory).
7. $\overline{CS}$ pin driven inactive (V_{IH}).

Note 1: It is recommended that while the $\overline{CS}$ pin is active, only one type of command should be issued. When changing commands, it is recommended to take the $\overline{CS}$ pin inactive then force it back to the active state.

2: It is also recommended that long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

TABLE 7-3: COMMANDS

Command Name	# of Bits	High Voltage (V_{IHH}) on CS pin?
Write Data	16-Bits	—
Read Data	16-Bits	—
Increment Wiper	8-Bits	—
Decrement Wiper	8-Bits	—
High-Voltage **Write Data**	16-Bits	Yes
High-Voltage **Read Data**	16-Bits	Yes
High-Voltage **Increment Wiper**	8-Bits	Yes
High-Voltage **Decrement Wiper**	8-Bits	Yes

7.5 Write Data Normal and High Voltage

The Write command is a 16-bit command. The format of the command is shown in Figure 7-2.

A Write command to a volatile memory location changes that location after a properly formatted Write command (16-clock) have been received.

7.5.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{CS}$ pin be in the active state (V_{IL} or V_{IHH}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 16-bit Write command (command byte and data byte) is then clocked in on the SCK and SDI pins. Once all 16 bits have been received, the specified volatile address is updated. A write will not occur if the write command isn't exactly 16 clocks pulses. This protects against system issues from corrupting the nonvolatile memory locations.

Figure 6-2 and Figure 6-3 show possible waveforms for a single write.

	COMMAND BYTE								DATA BYTE								
SDI	AD3	AD2	AD1	AD0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
SDO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid Address/Command combination
	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Invalid Address/Command combination (1)

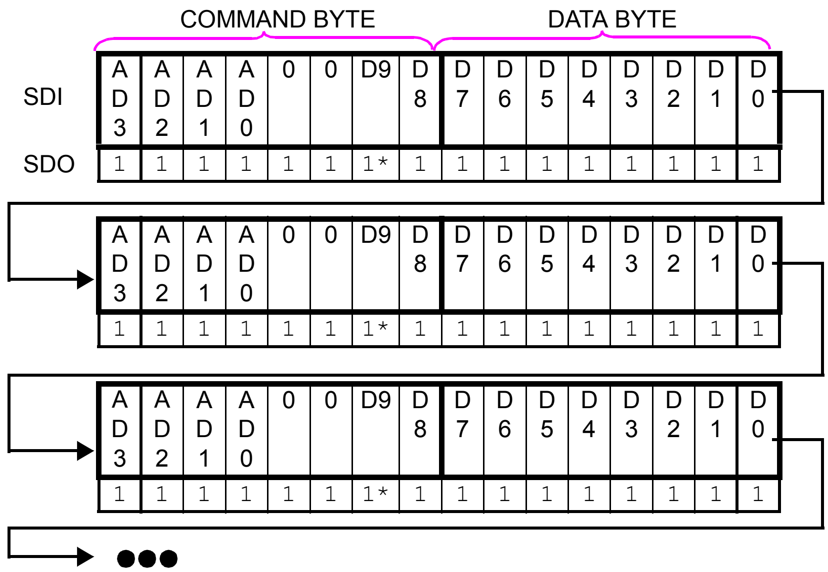
Note 1: If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-2: *Write Command – SDI and SDO States.*

7.5.2 CONTINUOUS WRITES TO VOLATILE MEMORY

Continuous writes are possible only when writing to the volatile memory registers (address 00h, 01h and 04h).

Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.



Note 1: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive (V_{IH}).

FIGURE 7-3: *Continuous Write Sequence.*

7.6 Read Data Normal and High Voltage

The Read command is a 16-bit command. The format of the command is shown in Figure 7-4.

The first 6 bits of the Read command determine the address and the command. The 7th clock will output the CMDERR bit on the SDO pin. The remaining 9-clocks the device will transmit the 9 data bits (D8:D0) of the specified address (AD3:AD0).

Figure 7-4 shows the SDI and SDO information for a Read command.

7.6.1 SINGLE READ

The read operation requires that the $\overline{CS}$ pin be in the active state (V_{IL} or V_{IHH}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL} or V_{IHH}). The 16-bit Read command (command byte and data byte) is then clocked in on the SCK and SDI pins. The SDO pin starts driving data on the 7th bit (CMDERR bit) and the addressed data comes out on the 8th through 16th clocks. Figure 6-2 through Figure 6-3 show possible waveforms for a single read.

COMMAND BYTE / DATA BYTE

SDI	AD3	AD2	AD1	AD0	1	1	X	X	X	X	X	X	X	X	X	X	
SDO	1	1	1	1	1	1	1	D8	D7	D6	D5	D4	D3	D2	D1	D0	Valid Address/Command combination
	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Attempted Memory Read of Reserved Memory location

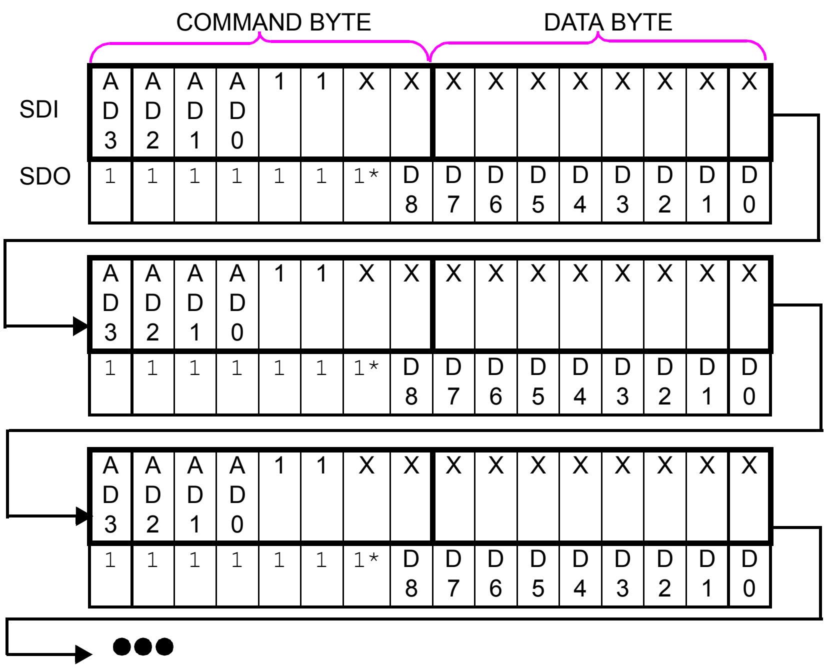
READ DATA

FIGURE 7-4: *Read Command – SDI and SDO States.*

7.6.2 CONTINUOUS READS

Continuous reads allow the devices memory to be read quickly. Continuous reads are possible to all memory locations.

Figure 7-5 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.



Note 1: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive (V_{IH}).

FIGURE 7-5: *Continuous Read Sequence.*

7.7 Increment Wiper Normal and High Voltage

The Increment command is an 8-bit command. The Increment command can only be issued to volatile memory locations. The format of the command is shown in Figure 7-6.

An Increment command to the volatile memory location changes that location after a properly formatted command (8-clocks) have been received.

Increment commands provide a quick and easy method to modify the value of the volatile wiper location by +1 with minimal overhead.

COMMAND BYTE

(INCR COMMAND (n+1))

SDI	AD3	AD2	AD1	AD0	0	1	X	X	
SDO	1	1	1	1	1	1	1*	1	**Note 1, 2**
	1	1	1	1	1	1	0	0	**Note 1, 3**

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

2: Valid Address/Command combination.

3: Invalid Address/Command combination all following SDO bits will be low until the CMDERR condition is cleared. (the $\overline{CS}$ pin is forced to the inactive state).

4: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive (V_{IH}).

FIGURE 7-6: *Increment Command – SDI and SDO States.*

Note: Table 7-2 shows the valid addresses for the Increment Wiper command. Other addresses are invalid.

7.7.1 SINGLE INCREMENT

Typically, the $\overline{CS}$ pin starts at the inactive state (V_{IH}), but may already be in the active state due to the completion of another command.

Figure 6-4 through Figure 6-5 show possible waveforms for a single increment. The increment operation requires that the $\overline{CS}$ pin be in the active state (V_{IL} or V_{IHH}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL} or V_{IHH}). The 8-bit Increment command (command byte) is then clocked in on the SDI pin by the SCK pins. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will increment up to 100h on 8-bit devices and 80h on 7-bit devices. After the wiper value has reached full scale (8-bit = 100h, 7-bit = 80h), the wiper value will not be incremented further. If the wiper register has a value between 101h and 1FFh, the Increment command is disabled. See Table 7-4 for additional information on the Increment command versus the current volatile wiper value.

The increment operations only require the Increment command byte while the $\overline{CS}$ pin is active (V_{IL} or V_{IHH}) for a single increment.

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

TABLE 7-4: INCREMENT OPERATION VS. VOLATILE WIPER VALUE

Current Wiper Setting		Wiper (W) Properties	Increment Command Operates?
7-bit Pot	8-bit Pot		
3FFh 081h	3FFh 101h	Reserved (Full Scale (W = A))	No
080h	100h	Full Scale (W = A)	No
07Fh 041h	0FFh 081	W = N	Yes
040h	080h	W = N (Mid-scale)	
03Fh 001h	07Fh 001	W = N	
000h	000h	Zero Scale (W = B)	Yes

7.7.2 CONTINUOUS INCREMENTS

Continuous increments are possible only when writing to the volatile memory registers (address 00h, 01h, 06h and 07h).

Figure 7-7 shows a continuous increment sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

When executing an continuous Increment commands, the selected wiper will be altered from n to n+1 for each Increment command received. The wiper value will increment up to 100h on 8-bit devices and 80h on 7-bit devices. After the wiper value has reached full scale (8-bit = 100h, 7-bit = 80h), the wiper value will not be incremented further. If the wiper register has a value between 101h and 1FFh, the Increment command is disabled.

Increment commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met.

When executing a continuous command string, the Increment command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions (on the SCK pin do not cause the wiper setting to change). Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

	COMMAND BYTE (INCR COMMAND (n+1))								COMMAND BYTE (INCR COMMAND (n+2))								COMMAND BYTE (INCR COMMAND (n+3))								
SDI	AD3	AD2	AD1	AD0	0	1	X	X	AD3	AD2	AD1	AD0	0	1	X	X	AD3	AD2	AD1	AD0	0	1	X	X	
SDO	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	**Note 1, 2**
	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	**Note 3, 4**

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

2: Valid Address/Command combination.

3: Invalid Address/Command combination.

4: If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-7: *Continuous Increment Command – SDI and SDO States.*

7.8 Decrement Wiper Normal and High Voltage

The Decrement command is an 8-bit command. The Decrement command can only be issued to volatile memory locations. The format of the command is shown in Figure 7-6.

A Decrement command to the volatile memory location changes that location after a properly formatted command (8 clocks) have been received.

Decrement commands provide a quick and easy method to modify the value of the volatile wiper location by -1 with minimal overhead.

COMMAND BYTE

(DECR COMMAND (n+1))

SDI	AD3	AD2	AD1	AD0	1	0	X	X	
SDO	1	1	1	1	1	1	1*	1	**Note 1, 2**
	1	1	1	1	1	1	0	0	**Note 1, 3**

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

2: Valid Address/Command combination.

3: Invalid Address/Command combination all following SDO bits will be low until the CMDERR condition is cleared. (the $\overline{CS}$ pin is forced to the inactive state).

4: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive (V_{IH}).

FIGURE 7-8: *Decrement Command – SDI and SDO States.*

Note: Table 7-2 shows the valid addresses for the Decrement Wiper command. Other addresses are invalid.

7.8.1 SINGLE DECREMENT

Typically, the $\overline{CS}$ pin starts at the inactive state (V_{IH}), but may already be in the active state due to the completion of another command.

Figure 6-4 through Figure 6-5 show possible waveforms for a single decrement. The decrement operation requires that the $\overline{CS}$ pin be in the active state (V_{IL} or V_{IHH}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL} or V_{IHH}). Then the 8-bit Decrement command (command byte) is clocked in on the SDI pin by the SCK pins. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will decrement from the wiper's full scale value (100h on 8-bit devices and 80h on 7-bit devices). Above the wiper's full scale value (8-bit = 101h to 1FFh, 7-bit = 81h to FFh), the Decrement command is disabled. If the wiper register has a zero scale value (000h), then the wiper value will not decrement. See Table 7-5 for additional information on the Decrement command vs. the current volatile wiper value.

The Decrement commands only require the Decrement command byte, while the $\overline{CS}$ pin is active (V_{IL} or V_{IHH}) for a single decrement.

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired decrement occurs.

TABLE 7-5: DECREMENT OPERATION VS. VOLATILE WIPER VALUE

Current Wiper Setting		Wiper (W) Properties	Decrement Command Operates?
7-bit Pot	**8-bit Pot**		
3FFh 081h	3FFh 101h	Reserved (Full Scale (W = A))	No
080h	100h	Full Scale (W = A)	Yes
07Fh 041h	0FFh 081	W = N	Yes
040h	080h	W = N (Mid-scale)	
03Fh 001h	07Fh 001	W = N	
000h	000h	Zero Scale (W = B)	No

7.8.2 CONTINUOUS DECREMENTS

Continuous decrements are possible only when writing to the volatile memory registers (address 00h, 01h, and 04h).

Figure 7-9 shows a continuous decrement sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

When executing continuous Decrement commands, the selected wiper will be altered from n to n-1 for each Decrement command received. The wiper value will decrement from the wiper's full scale value (100h on 8-bit devices and 80h on 7-bit devices). Above the wiper's full scale value (8-bit = 101h to 1FFh, 7-bit = 81h to FFh), the Decrement command is disabled. If the Wiper register has a zero scale value (000h), then the wiper value will not decrement. See Table 7-5 for additional information on the Decrement command vs. the current volatile wiper value.

Decrement commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met.

When executing a continuous command string, the Decrement command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that "unexpected" transitions (on the SCK pin do not cause the wiper setting to change). Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired decrement occurs.

	COMMAND BYTE (DECR COMMAND (n-1))								COMMAND BYTE (DECR COMMAND (n-1))								COMMAND BYTE (DECR COMMAND (n-1))								
SDI	AD3	AD2	AD1	AD0	1	0	X	X	AD3	AD2	AD1	AD0	1	0	X	X	AD3	AD2	AD1	AD0	1	0	X	X	
SDO	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	**Note 1, 2**
	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	**Note 3, 4**

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

2: Valid Address/Command combination.

3: Invalid Address/Command combination.

4: If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-9: *Continuous Decrement Command – SDI and SDO States.*

8.0 APPLICATIONS EXAMPLES

Digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP433X/435X devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations (V_{DD} = 2.7V to 5.5V).

8.1 Split Rail Applications

All inputs that would be used to interface to a host controller support high voltage on their input pin. This allows the MCP43XX device to be used in split power rail applications.

An example of this is a battery application where the PIC® MCU is directly powered by the battery supply (4.8V) and the MCP43XX device is powered by the 3.3V regulated voltage.

For SPI applications, these inputs are:

- $\overline{\text{CS}}$
- SCK
- SDI (or SDI/SDO)
- $\overline{\text{RESET}}$

Figure 8-1 through Figure 8-2 show three example split rail systems. In this system, the MCP43XX interface input signals need to be able to support the PIC MCU output high voltage (V_{OH}).

In Example #1 (Figure 8-1), the MCP43XX interface input signals need to be able to support the PIC MCU output high voltage (V_{OH}). If the split rail voltage delta becomes too large, then the customer may be required to do some level shifting due to MCP43XX V_{OH} levels related to host controller V_{IH} levels.

In Example #2 (Figure 8-2), the MCP43XX interface input signals need to be able to support the lower voltage of the PIC MCU output high voltage level (V_{OH}).

Table 8-1 shows an example PIC microcontroller I/O voltage specifications and the MCP43XX specifications. So this PIC MCU operating at 3.3V will drive a V_{OH} at 2.64V, and for the MCP43XX operating at 5.5V, the V_{IH} is 2.47V. Therefore, the interface signals meet specifications.

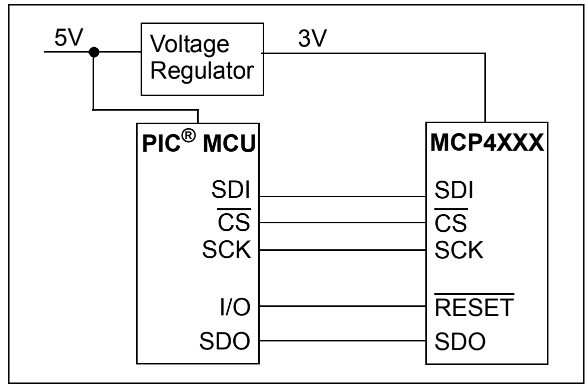


FIGURE 8-1: *Example Split Rail System 1.*

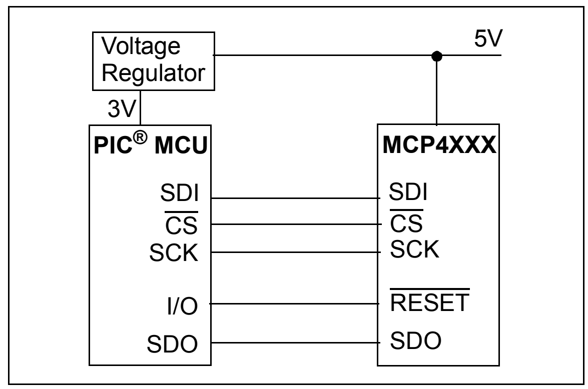


FIGURE 8-2: *Example Split Rail System 2.*

TABLE 8-1: V_{OH} – V_{IH} COMPARISONS

PIC® MCU (1)			MCP4XXX (2)			Comment
V_{DD}	V_{IH}	V_{OH}	V_{DD}	V_{IH}	V_{OH}	
5.5	4.4	4.4	2.7	1.215	— (3)	
5.0	4.0	4.0	3.0	1.35	— (3)	
4.5	3.6	3.6	3.3	1.485	— (3)	
3.3	2.64	2.64	4.5	2.025	— (3)	
3.0	2.4	2.4	5.0	2.25	— (3)	
2.7	2.16	2.16	5.5	2.475	— (3)	

Note 1: V_{OH} minimum = 0.8 * V_{DD};
V_{OL} maximum = 0.6V
V_{IH} minimum = 0.8 * V_{DD};
V_{IL} maximum = 0.2 * V_{DD};

2: V_{OH} minimum (SDA only) =;
V_{OL} maximum = 0.2 * V_{DD}
V_{IH} minimum = 0.45 * V_{DD};
V_{IL} maximum = 0.2 * V_{DD}

3: The only MCP4XXX output pin is SDO, which is open-drain (or open-drain with internal pull-up) with high voltage support

8.2 Techniques to Force the $\overline{CS}$ Pin to V_{IHH}

The circuit in Figure 8-3 shows a method using the TC1240A doubling charge pump. When the SHDN pin is high, the TC1240A is off, and the level on the $\overline{CS}$ pin is controlled by the PIC® microcontrollers (MCUs) IO2 pin.

When the SHDN pin is low, the TC1240A is on and the V_{OUT} voltage is 2 * V_{DD}. The resistor R_1 allows the $\overline{CS}$ pin to go higher than the voltage such that the PIC MCU's IO2 pin "clamps" at approximately V_{DD}.

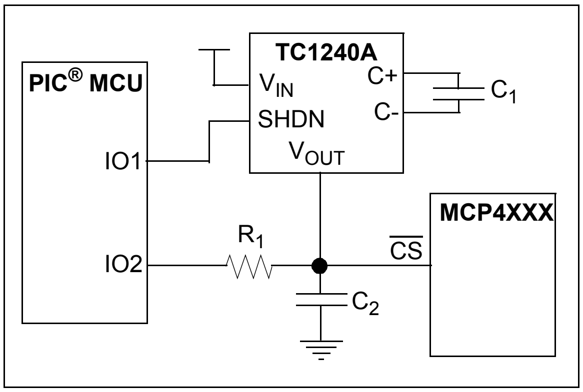


FIGURE 8-3: *Using the TC1240A to Generate the V_{IHH} Voltage.*

The circuit in Figure 8-4 shows the method used on the MCP402X Nonvolatile Digital Potentiometer Evaluation Board (Part Number: MCP402XEV). This method requires that the system voltage be approximately 5V. This ensures that when the PIC10F206 enters a brown-out condition, there is an insufficient voltage level on the $\overline{CS}$ pin to change the stored value of the wiper. The *"MCP402X Nonvolatile Digital Potentiometer Evaluation Board User's Guide"* (DS51546) contains a complete schematic.

GP0 is a general purpose I/O pin, while GP2 can either be a general purpose I/O pin or it can output the internal clock.

For the serial commands, configure the GP2 pin as an input (high-impedance). The output state of the GP0 pin will determine the voltage on the $\overline{CS}$ pin (V_{IL} or V_{IH}).

For high-voltage serial commands, force the GP0 output pin to output a high level (V_{OH}) and configure the GP2 pin to output the internal clock. This will form a charge pump and increase the voltage on the $\overline{CS}$ pin (when the system voltage is approximately 5V).

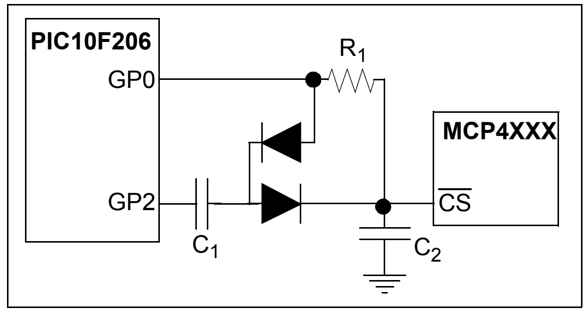


FIGURE 8-4: *MCP4XXX Nonvolatile Digital Potentiometer Evaluation Board (MCP402XEV) implementation to generate the V_{IHH} voltage.*

8.3 Using Shutdown Modes

Figure 8-5 shows a possible application circuit where the independent terminals could be used. Disconnecting the wiper allows the transistor input to be taken to the bias voltage level (disconnecting A and or B may be desired to reduce system current). Disconnecting Terminal A modifies the transistor input by the R_{BW} rheostat value to the Common B. Disconnecting Terminal B modifies the transistor input by the R_{AW} rheostat value to the Common A. The Common A and Common B connections could be connected to V_{DD} and V_{SS}.

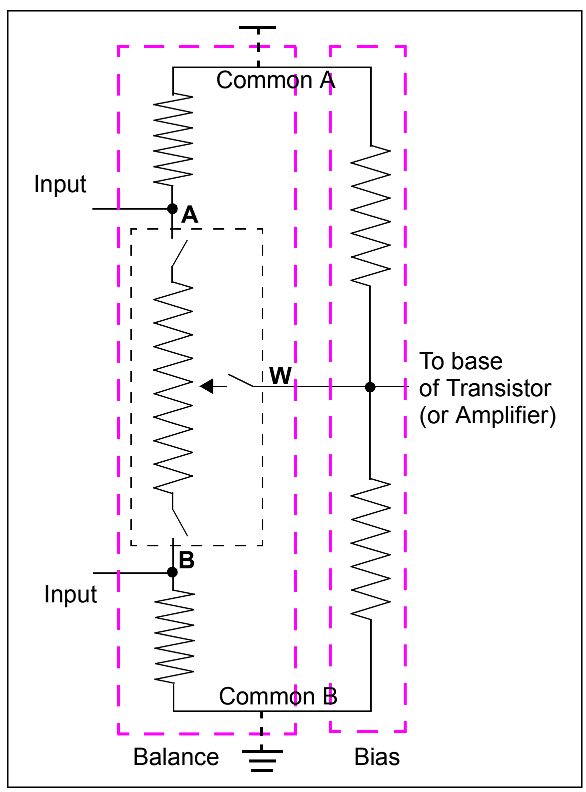


FIGURE 8-5: *Example Application Circuit using Terminal Disconnects.*

8.4 Design Considerations

In the design of a system with the MCP43XX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.4.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-6 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

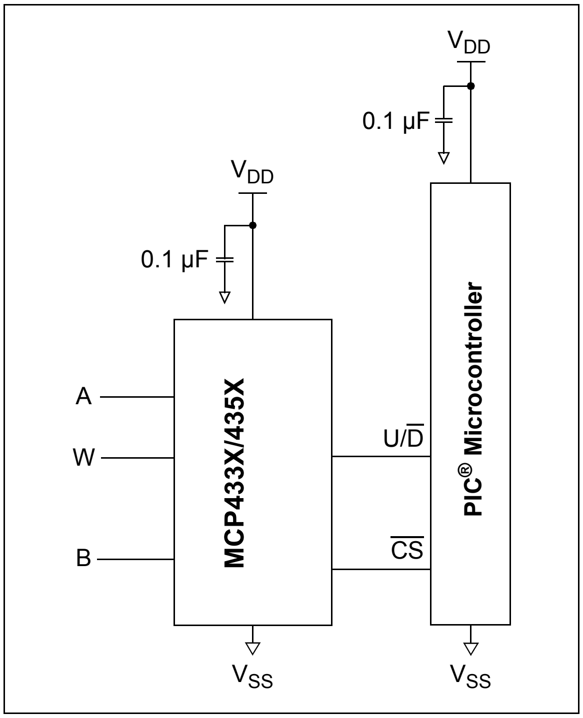


FIGURE 8-6: *Typical Microcontroller Connections.*

8.4.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **Footprint Compatibility**
- **PCB Area Requirements**

8.4.2.1 Noise

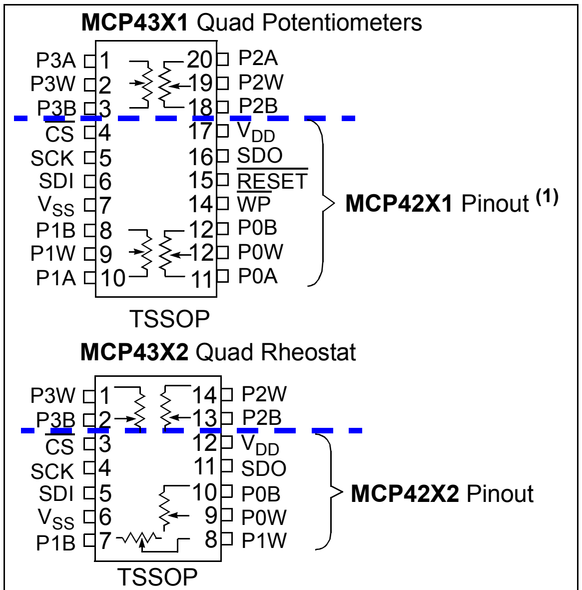
Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP43XX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

8.4.2.2 Footprint Compatibility

The specification of the MCP43XX pinouts was done to allow systems to be designed to easily support the use of either the dual (MCP42XX) or quad (MCP43XX) device.

Figure 8-7 shows how the dual pinout devices fit on the quad device footprint. For the Rheostat devices, the dual device is in the MSOP package, so the footprints would need to be offset from each other.



Note 1: Pin 15 (RESET) is the Shutdown (SHDN) pin on the MCP42x1 device.

FIGURE 8-7: *Quad Pinout (TSSOP Package) vs. Dual Pinout.*

Figure 8-8 shows possible layout implementations for an application to support the quad and dual options on the same PCB.

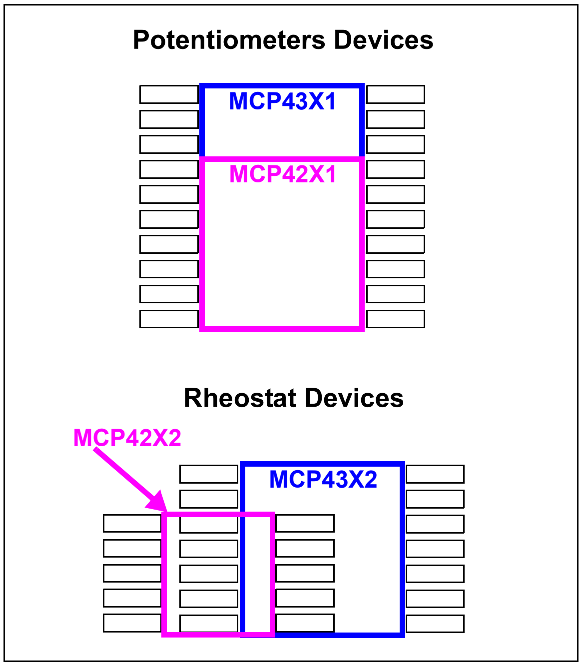


FIGURE 8-8: Layout to support Quad and Dual Devices.

8.4.2.3 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the package dimensions and area for the different package options. The table also shows the relative area factor compared to the smallest area. For space critical applications, the QFN package would be the suggested package.

TABLE 8-2: PACKAGE FOOTPRINT (1)

Package			Package Footprint			
Pins	Type	Code	Dimensions (mm) X	Dimensions (mm) Y	Area (mm^2)	Relative Area
14	TSSOP	ST	5.10	6.40	32.64	2.04
20	QFN	ML	4.00	4.00	16.00	1
20	TSSOP	ST	6.60	6.40	42.24	2.64

Note 1: Does not include recommended land pattern dimensions.

8.4.3 RESISTOR TEMPCO

Characterization curves of the resistor temperature coefficient (Tempco) are shown in Figure 2-11, Figure 2-32, Figure 2-52, and Figure 2-72.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end to end change is R_{AB} resistance.

8.4.4 HIGH VOLTAGE TOLERANT PINS

High voltage support (V_{IHH}) on the Serial Interface pins supports in-circuit accommodation of split rail applications and power supply sync issues.

9.0 DEVELOPMENT SUPPORT

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP43XX devices. The currently available tools are shown in Table 9-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

TABLE 9-1: DEVELOPMENT TOOLS

Board Name	Part #	Supported Devices
20-pin TSSOP and SSOP Evaluation Board	TSSOP20EV	MCP43XX
MCP4361 Evaluation Board (1)	MCP43XXEV	MCP4361
MCP42XX Digital Potentiometer PICtail™ Plus Demo Board	MCP42XXDM-PTPLS	MCP42XX
MCP4XXX Digital Potentiometer Daughter Board (2)	MCP4XXXDM-DB	MCP42XXX, MCP42XX, MCP4021 and MCP4011

Note 1: This Evaluation Board is planned to be available by March 2010. This board uses the TSSOP20EV PCB and requires the PICkit™ Serial Analyzer (see User's Guide for details). This kit also includes 1 blank TSSOP20EV PCB.

2: Requires the use of a PICDEM™ Demo board (see User's Guide for details).

TABLE 9-2: TECHNICAL DOCUMENTATION

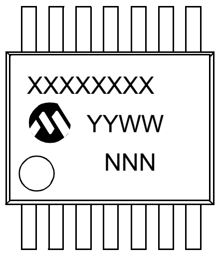
Application Note Number	Title	Literature #
AN1080	Understanding Digital Potentiometers Resistor Variations	DS01080
AN737	Using Digital Potentiometers to Design Low-Pass Adjustable Filters	DS00737
AN692	Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect	DS00692
AN691	Optimizing the Digital Potentiometer in Precision Circuits	DS00691
AN219	Comparing Digital Potentiometers to Mechanical Potentiometers	DS00219
—	Digital Potentiometer Design Guide	DS22017
—	Signal Chain Design Guide	DS21825

NOTES:

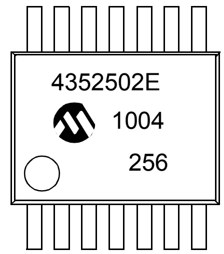
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

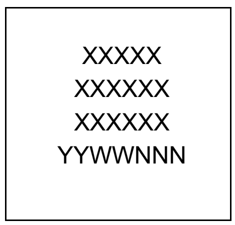
14-Lead TSSOP



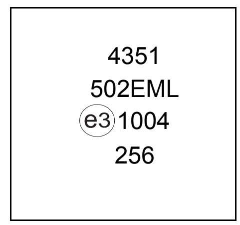
Example



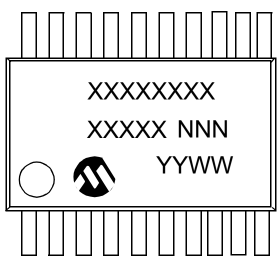
20-Lead QFN (4x4)



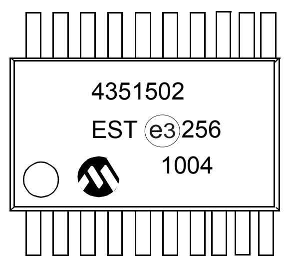
Example



20-Lead TSSOP



Example

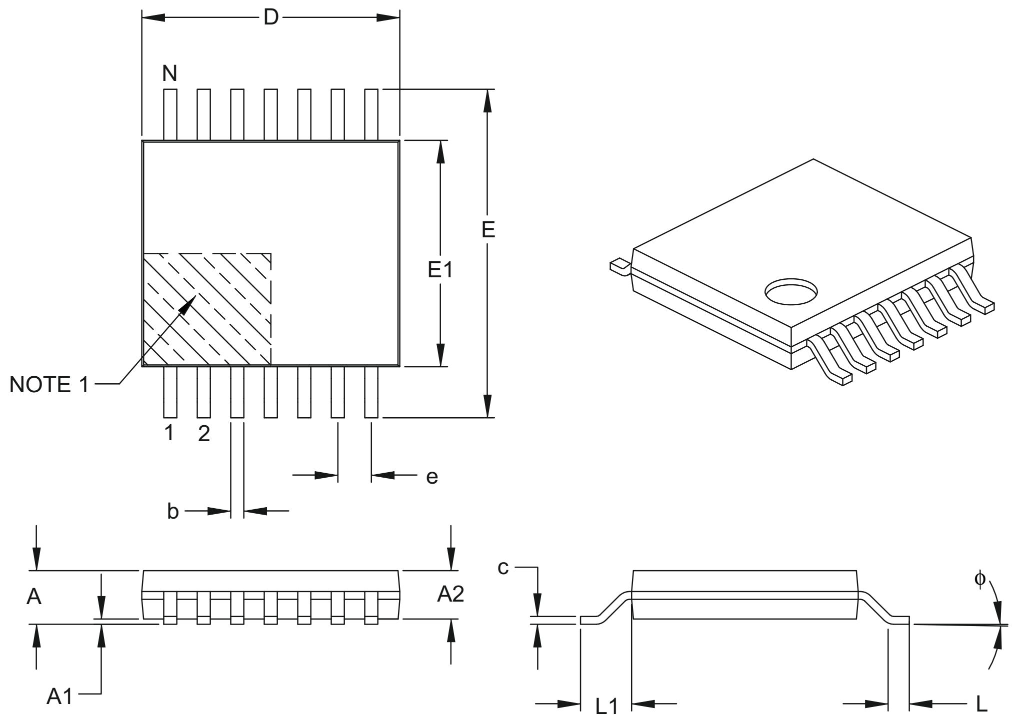


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

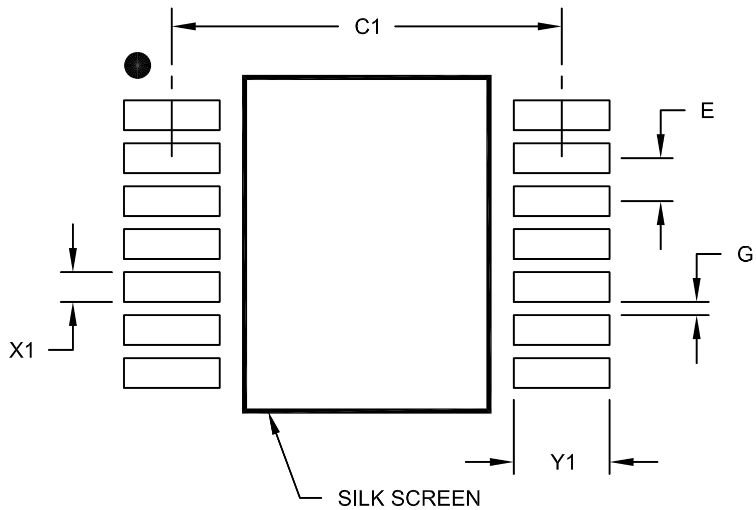
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

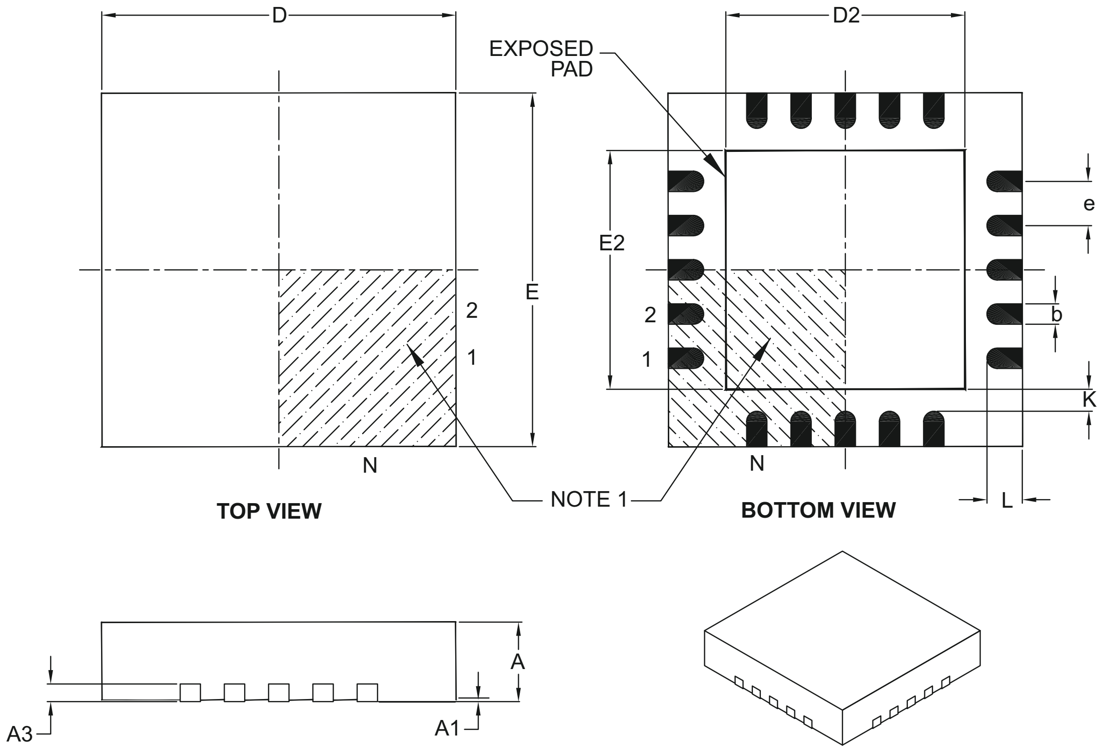
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

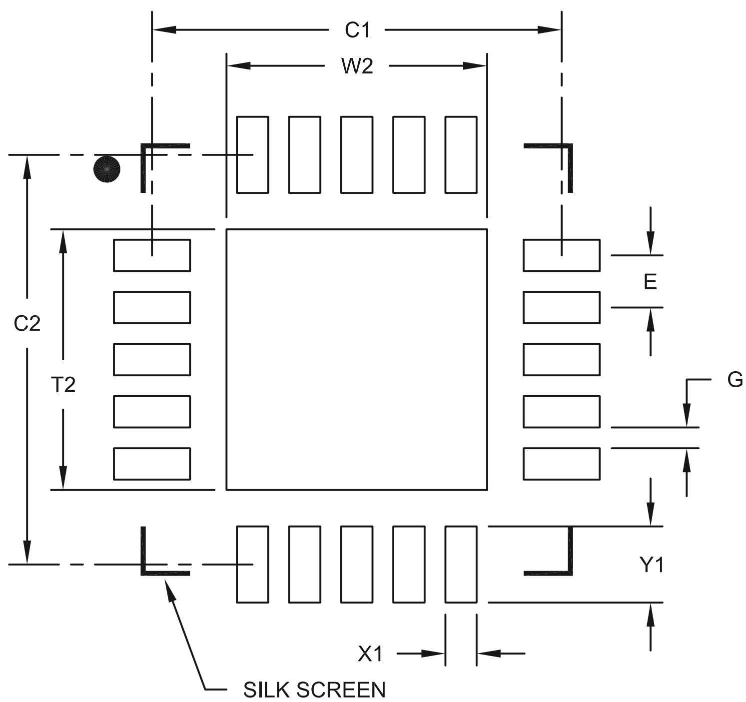
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

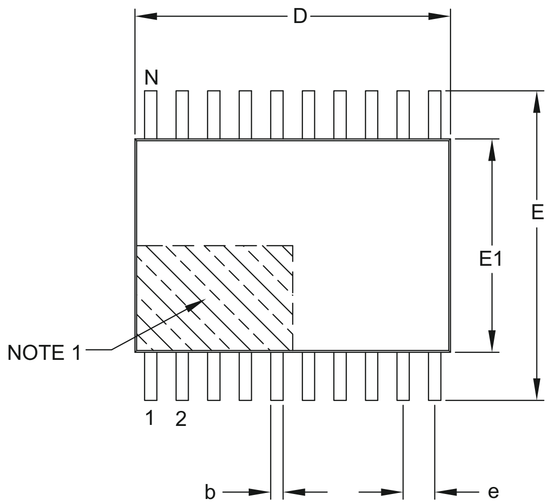
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

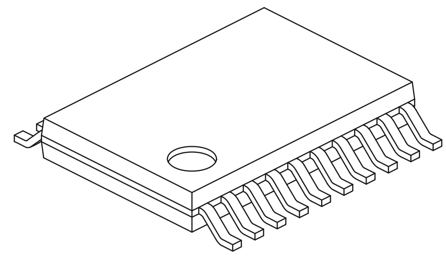
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

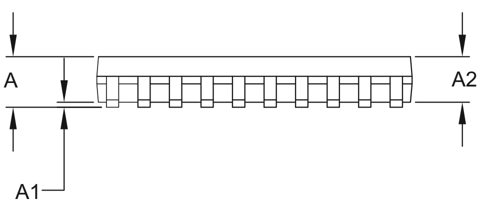
Microchip Technology Drawing No. C04-2126A

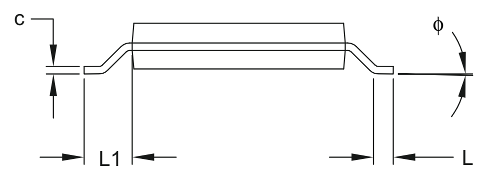
20-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

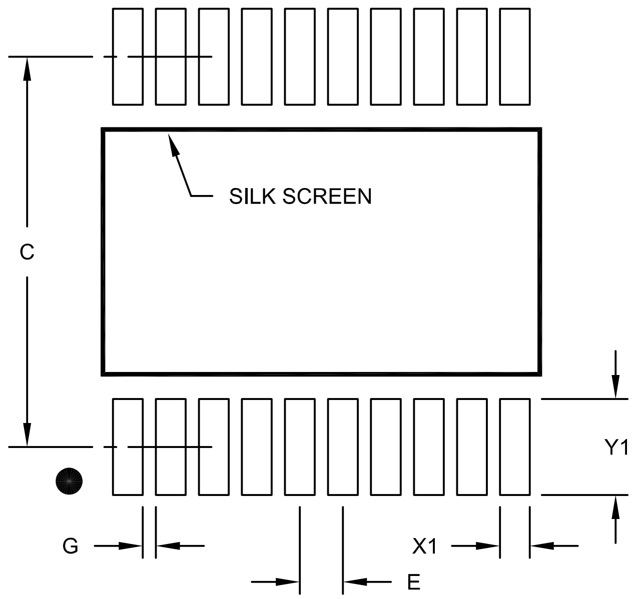
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088B

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

NOTES:

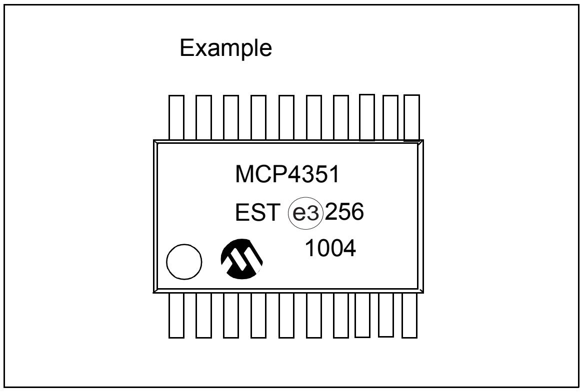
APPENDIX A: REVISION HISTORY

Revision A (March 2010)

- Original Release of this Document.

Note: Original TSSOP-20 device samples used the example marking shown in Figure A-1. Future device samples will usE the part marking shown in Section 10.

Figure A-1: Old example TSSOP-20 device marking.



NOTES:

APPENDIX B: CHARACTERIZATION DATA ANALYSIS

Some designers may desire to understand the device operational characteristics outside of the specified operating conditions of the device.

Applications where the knowledge of the resistor network characteristics could be useful include battery powered devices and applications that experience brown-out conditions.

In battery applications the application voltage decays over time until new batteries are installed. As the voltage decays, the system will continue to operate. At some voltage level, the application will be below its specified operating voltage range. This is dependent on the individual components used in the design. It is still useful to understand the device characteristics to expect when this low-voltage range is encountered. Unlike a microcontroller which can use an external supervisor device to force the controller into the Reset state, a digital potentiometer's resistance characteristic is not specified. But understanding the operational characteristics can be important in the design of the applications circuit for this low-voltage condition.

Other application system scenarios where understanding the low-voltage characteristics of the resistor network could be important is for system brown out conditions.

For the MCP433X/435X devices, the analog operation is specified at a minimum of 2.7V. Device testing has Terminal A connected to the device V_{DD} (for potentiometer configuration only) and Terminal B connected to V_{SS}.

B.1 Low-Voltage Operation

This appendix gives an overview of CMOS semiconductor characteristics at lower voltages. This is important so that the 1.8V resistor network characterization graphs of the MCP433X/435X devices can be better understood.

For this discussion, we will use the 5 kΩ device data. This data was chosen since the variations of wiper resistance has much greater implications for devices with smaller R_{AB} resistances.

Figure B-1 shows the worst case R_{BW} error from the average R_{BW} as a percentage, while Figure B-2 shows the R_{BW} resistance verse wiper code graph. Nonlinear behavior occurs at approximately wiper code 160. This is better shown in Figure B-2, where the R_{BW} resistance changes from a linear slope. This change is due to the change in the wiper resistance.

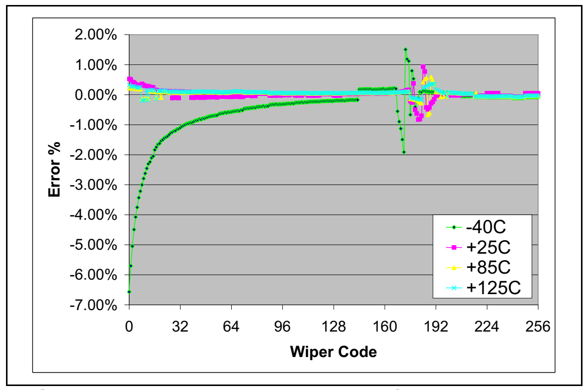


FIGURE B-1: *1.8V Worst Case R_{BW} Error from Average R_{BW} (R_{BW0}-R_{BW3}) vs. Wiper Code and Temperature (V_{DD} = 1.8V, I_W = 190 µA).*

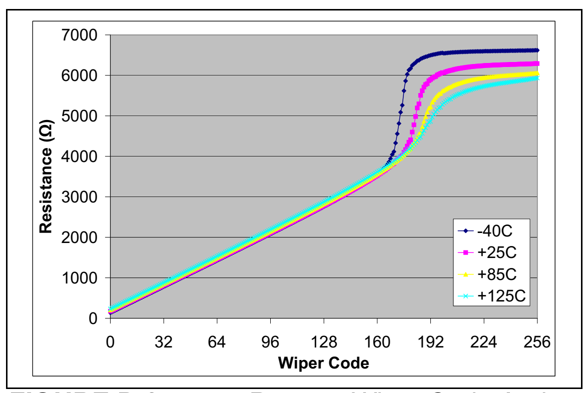


FIGURE B-2: *R_{BW} vs. Wiper Code And Temperature (V_{DD} = 1.8V, I_W = 190 µA).*

Figure B-3 and Figure B-4 show the wiper resistance for V_{DD} voltages of 5.5, 3.0, 1.8 Volts. These graphs show that as the resistor ladder wiper node voltage (V_{WCn}) approaches the $V_{DD}/2$ voltage, the wiper resistance increases. These graphs also show the different resistance characteristics of the NMOS and PMOS transistors that make up the wiper switch. This is demonstrated by the wiper code resistance curve, which does not mirror itself around the mid-scale code (wiper code = 128).

So why is the R_W graphs showing the maximum resistance at about mid-scale (wiper code = 128) and the R_{BW} graphs showing the issue at code 160?

This requires understanding low-voltage transistor characteristics as well as how the data was measured.

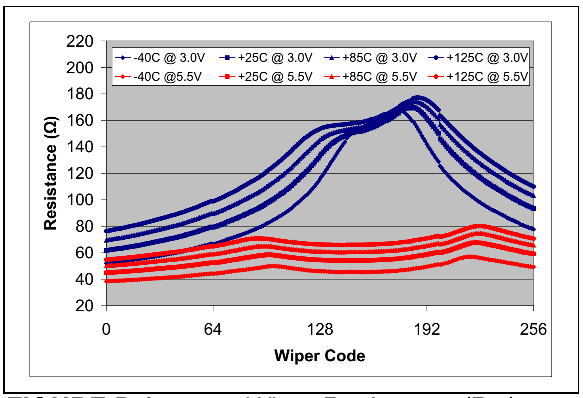


FIGURE B-3: *Wiper Resistance (R_W) vs. Wiper Code and Temperature (V_{DD} = 5.5V, I_W = 900 UA; V_{DD} = 3.0V, I_W = 480 µA).*

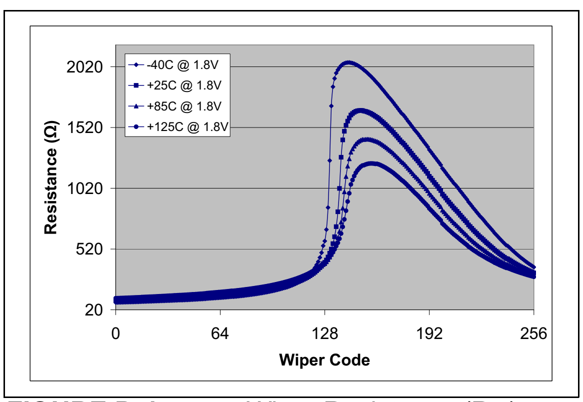


FIGURE B-4: *Wiper Resistance (R_W) vs. Wiper Code and Temperature (V_{DD} = 1.8V, I_W = 260 µA).*

The method in which the data was collected is important to understand. Figure B-5 shows the technique that was used to measure the R_{BW} and R_W resistance. In this technique Terminal A is floating and Terminal B is connected to ground. A fixed current is then forced into the wiper (I_W) and the corresponding wiper voltage (V_W) is measured. Forcing a known current through R_{BW} (I_W) and then measuring the voltage difference between the wiper (V_W) and Terminal A (V_A), the wiper resistance (R_W) can be calculated, see Figure B-5. Changes in I_W current will change the wiper voltage (V_W). This may effect the device's wiper resistance (R_W).

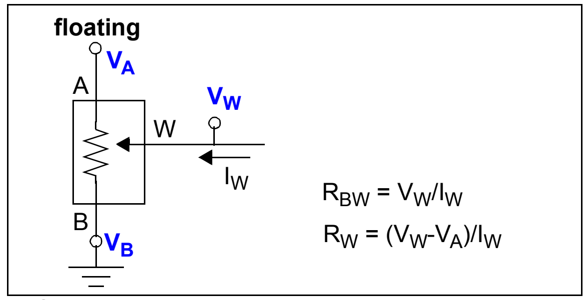
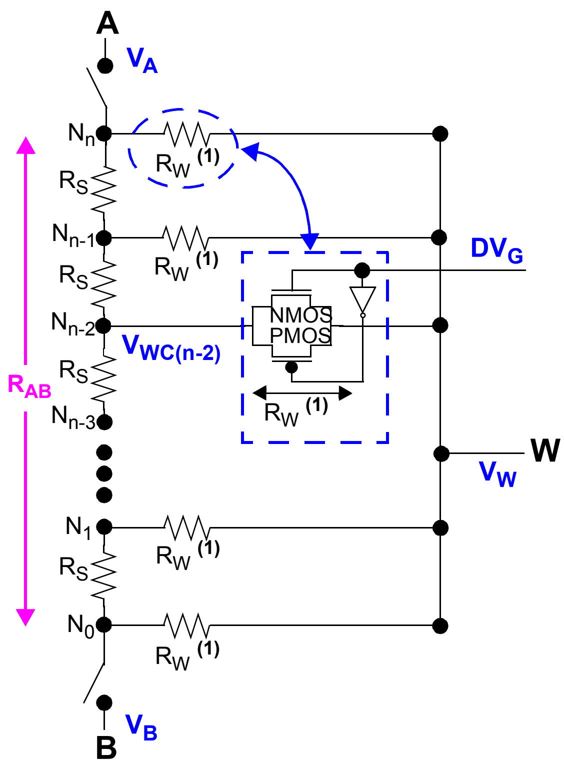


FIGURE B-5: *R_{BW} and R_W Measurement.*

Figure B-6 shows a block diagram of the resistor network where the R_{AB} resistor is a series of 256 R_S resistors. These resistors are polysilicon devices. Each wiper switch is an analog switch made up of an NMOS and PMOS transistor. A more detailed figure of the wiper switch is shown in Figure B-7. The wiper resistance is influenced by the voltage on the wiper switches nodes (V_G, V_W and V_{WCn}). Temperature also influences the characteristics of the wiper switch, see Figure B-4.

The NMOS transistor and PMOS transistor have different characteristics. These characteristics as well as the wiper switch node voltages determine the R_W resistance at each wiper code. The variation of each wiper switch's characteristics in the resistor network is greater then the variation of the R_S resistors.

The voltage on the resistor network node (V_{WCn}) is dependent upon the wiper code selected and the voltages applied to V_A, V_B and V_W. The wiper switch V_G voltage to V_W or V_{WCn} voltage determines how strongly the transistor is turned on. When the transistor is weakly turned on the wiper resistance R_W will be high. When the transistor is strongly turned on, the wiper resistance (R_W) will be in the typical range.

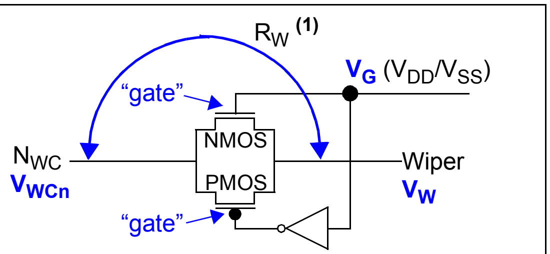


Note 1: The wiper resistance is dependent on several factors including, wiper code, device V_{DD}, Terminal voltages (on A, B and W), and temperature.

FIGURE B-6: *Resistor Network Block Diagram.*

The characteristics of the wiper is determined by the characteristics of the wiper switch at each of the resistor networks tap points. Figure B-7 shows an example of a wiper switch. As the device operational voltage becomes lower, the characteristics of the wiper switch change due to a lower voltage on the V_G signal.

Figure B-7 shows an implementation of a wiper switch. When the transistor is turned off, the switch resistance is in the Giga Ωs. When the transistor is turned on, the switch resistance is dependent on the V_G, V_W and V_{WCn} voltages. This resistance is referred to as R_W.



Note 1: Wiper Resistance (R_W) depends on the voltages at the wiper switch nodes (V_G, V_W and V_{WCn}).

FIGURE B-7: *Wiper Switch.*

So looking at the wiper voltage (V_W) for the 3.0V and 1.8V data gives the graphs in Figure B-8 and Figure B-9. In the 1.8V graph, as the V_W approaches 0.8V, the voltage increases nonlinearly. Since V = I * R, and the current (I_W) is constant, it means that the device resistance increased nonlinearly at around wiper code 160.

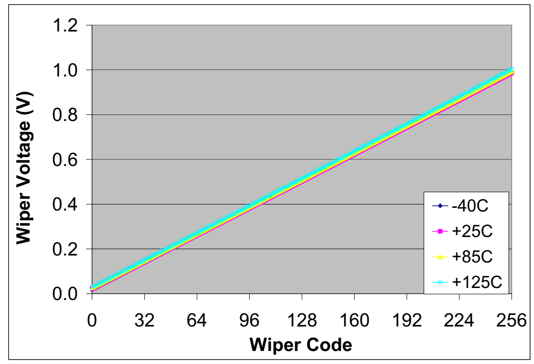


FIGURE B-8: *Wiper Voltage (V_W) vs. Wiper Code (V_{DD} = 3.0V, I_W = 190 µA).*

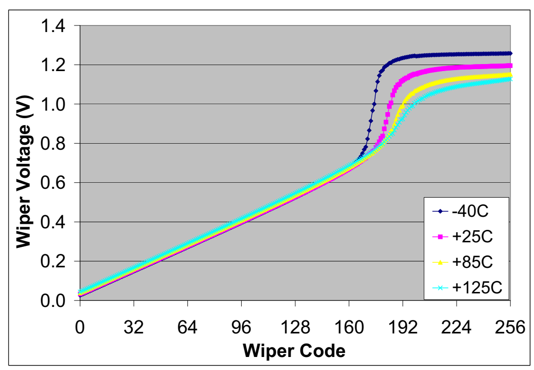


FIGURE B-9: *Wiper Voltage (V_W) vs. Wiper Code (V_{DD} = 1.8V, I_W = 190 µA).*

Using the simulation models of the NMOS and PMOS devices for the MCP43XX analog switch (Figure B-10), we plot the device resistance when the devices are turned on. Figure B-11 and Figure B-12 show the resistances of the NMOS and PMOS devices as the V_{IN} voltage is increased. The wiper resistance (R_W) is simply the parallel resistance on the NMOS and PMOS devices ($R_W = R_{NMOS} \parallel R_{PMOS}$). Below the threshold voltage for the NMOS ad PMOS devices, the resistance becomes very large (Giga Ωs). In the transistors active region, the resistance is much lower. For these graphs, the resistances are on different scales. Figure B-13 and Figure B-14 only plots the NMOS and PMOS device resistance for their active region and the resulting wiper resistance. For these graphs, all resistances are on the same scale.

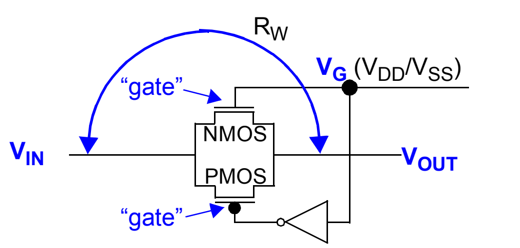


FIGURE B-10: *Analog Switch.*

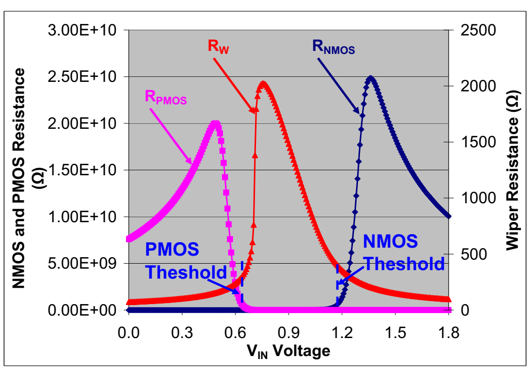


FIGURE B-11: *NMOS and PMOS Transistor Resistance (R_{NMOS}, R_{PMOS}) and Wiper Resistance (R_W) VS. V_{IN} (V_{DD} = 3.0V).*

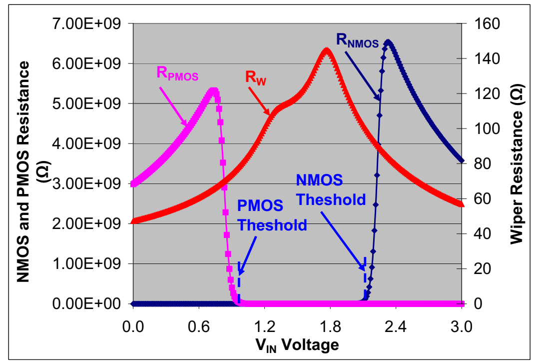


FIGURE B-12: *NMOS and PMOS Transistor Resistance (R_{NMOS}, R_{PMOS}) and Wiper Resistance (R_W) VS. V_{IN} (V_{DD} = 1.8V).*

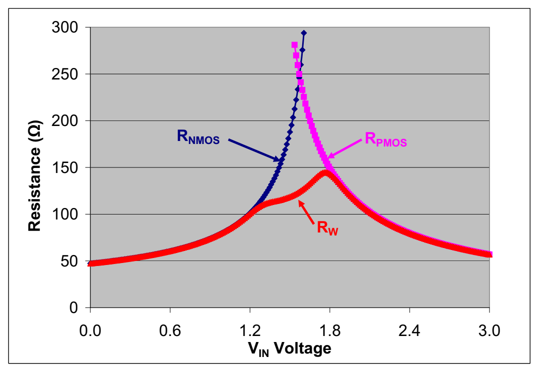


FIGURE B-13: *NMOS and PMOS Transistor Resistance (R_{NMOS}, R_{PMOS}) and Wiper Resistance (R_W) VS. V_{IN} (V_{DD} = 3.0V).*

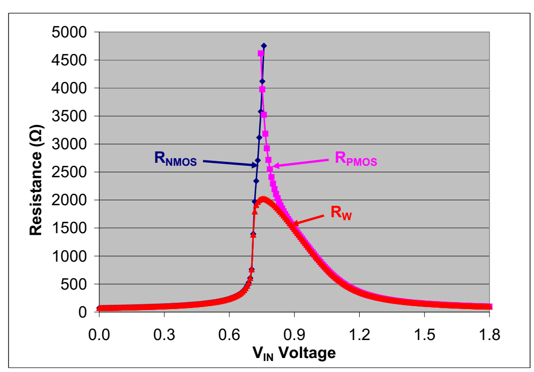


FIGURE B-14: *NMOS and PMOS Transistor Resistance (R_{NMOS}, R_{PMOS}) and Wiper Resistance (R_W) VS. V_{IN} (V_{DD} = 1.8V).*

B.2 Optimizing Circuit Design for Low-Voltage Characteristics

The low-voltage nonlinear characteristics can be minimized by application design. The section will show two application circuits that can be used to control a programmable reference voltage (V_{OUT}).

Minimizing the low-voltage nonlinear characteristics is done by keeping the voltages on the wiper switch nodes at a voltage where either the NMOS or PMOS transistor is turned on.

An example of this is if we are using a digital potentiometer for a voltage reference (V_{OUT}). Lets say that we want V_{OUT} to range from 0.5 * V_{DD} to 0.6 * V_{DD}.

In example implementation #1 (Figure B-15) we window the digital potentiometer using resistors R1 and R2. When the wiper code is at full scale the V_{OUT} voltage will be ≥ 0.6 * $V_{DD,}$ and when the wiper code is at zero scale the V_{OUT} voltage will be ≤ 0.5 * V_{DD}. Remember that the digital potentiometers R_{AB} variation must be included. Table B-1 shows that the V_{OUT} voltage can be selected to be between 0.455 * V_{DD} and 0.727 * V_{DD}, which includes the desired range. With respect to the voltages on the resistor network node, at 1.8V the V_A voltage would range from 1.29V to 1.31V while the V_B voltage would range from 0.82V to 0.86V. These voltages cause the wiper resistance to be in the nonlinear region (see Figure B-12). In Potentiometer mode, the variation of the wiper resistance is typically not an issue, as shown by the INL/DNL graph (Figure 2-7).

In example implementation #2 (Figure B-16) we use the digital potentiometer in Rheostat mode. The resistor ladder uses resistors R1 and R2 with R_{BW} at the bottom of the ladder. When the wiper code is at full scale, the V_{OUT} voltage will be ≥ 0.6 * V_{DD} and when the wiper code is at full scale the V_{OUT} voltage will be ≤ 0.5 * V_{DD}. Remember that the digital potentiometers R_{AB} variation must be included. Table B-2 shows that the V_{OUT} voltage can be selected to be between 0.50 * V_{DD} and 0.687 * V_{DD}, which includes the desired range. With respect to the voltages on the resistor network node, at 1.8V the V_W voltage would range from 0.29V to 0.38V. These voltages cause the wiper resistance to be in the linear region (see Figure B-12).

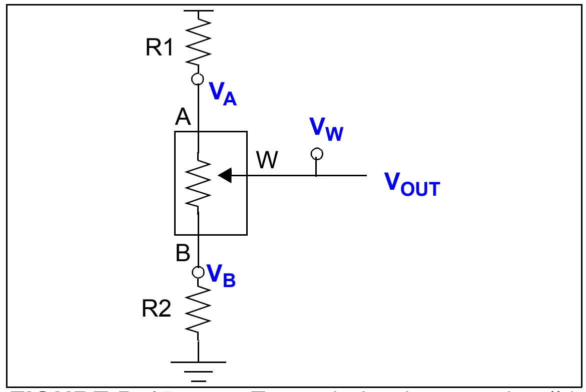


FIGURE B-15: Example Implementation #1.

TABLE B-1: EXAMPLE #1 VOLTAGE CALCULATIONS

	Variation		
	Min	**Typ**	**Max**
R1	12,000	12,000	12,000
R2	20,000	20,000	20,000
R_{AB}	8,000	10,000	12,000
V_{OUT} (@ FS)	0.714 V_{DD}	0.70 V_{DD}	0.727 V_{DD}
V_{OUT} (@ ZS)	0.476 V_{DD}	0.50 V_{DD}	0.455 V_{DD}
V_A	0.714 V_{DD}	0.70 V_{DD}	0.727 V_{DD}
V_B	0.476 V_{DD}	0.50 V_{DD}	0.455 V_{DD}

Legend: FS – Full Scale, ZS – Zero Scale

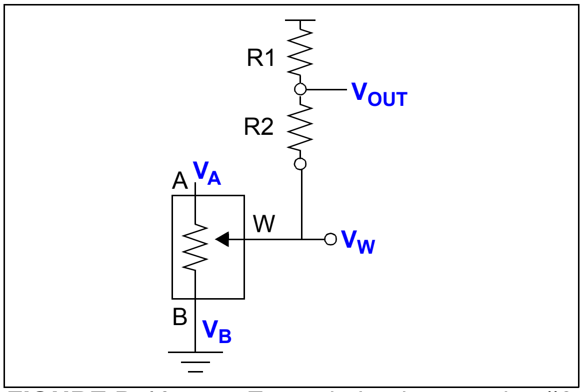


FIGURE B-16: Example Implementation #2.

TABLE B-2: EXAMPLE #2 VOLTAGE CALCULATIONS

	Variation		
	Min	**Typ**	**Max**
R1	10,000	10,000	10,000
R2	10,000	10,000	10,000
R_{BW} (max)	8,000	10,000	12,000
V_{OUT} (@ FS)	0.667 V_{DD}	0.643 V_{DD}	0.687 V_{DD}
V_{OUT}(@ ZS)	0.50 V_{DD}	0.50 V_{DD}	0.50 V_{DD}
V_W (@ FS)	0.333 V_{DD}	0.286 V_{DD}	0.375 V_{DD}
V_W (@ ZS)	V_{SS}	V_{SS}	V_{SS}

Legend: FS – Full Scale, ZS – Zero Scale

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XXX	X	/XX
Device	Resistance Version	Temperature Range	Package

Device:	MCP4331:	Quad Volatile 7-bit Potentiometer
	MCP4331T:	Quad Volatile 7-bit Potentiometer (Tape and Reel)
	MCP4332:	Quad Volatile 7-bit Rheostat
	MCP4332T:	Quad Volatile 7-bit Rheostat (Tape and Reel)
	MCP4351:	Quad Volatile 8-bit Potentiometer
	MCP4351T:	Quad Volatile 8-bit Potentiometer (Tape and Reel)
	MCP4352:	Quad Volatile 8-bit Rheostat
	MCP4352T:	Quad Volatile 8-bit Rheostat (Tape and Reel)
Resistance Version:	502	= 5 kΩ
	103	= 10 kΩ
	503	= 50 kΩ
	104	= 100 kΩ
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	ST	= Plastic Thin Shrink Small Outline (TSSOP), 14/20-lead
	ML	= Plastic Quad Flat No-lead (4x4 QFN), 20-lead

Examples:

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b) MCP4331T-502E/XX: T/R, 5 kΩ, 20-LD Device
c) MCP4331-103E/XX: 10 kΩ, 20-LD Device
d) MCP4331T-103E/XX: T/R, 10 kΩ, 20-LD Device
e) MCP4331-503E/XX: 50 kΩ, 20-LD Device
f) MCP4331T-503E/XX: T/R, 50 kΩ, 20-LD Device
g) MCP4331-104E/XX: 100 kΩ, 20-LD Device
h) MCP4331T-104E/XX: T/R, 100 kΩ, 20-LD Device

a) MCP4332-502E/XX: 5 kΩ, 14-LD Device
b) MCP4332T-502E/XX: T/R, 5 kΩ, 14-LD Device
c) MCP4332-103E/XX: 10 kΩ, 14-LD Device
d) MCP4332T-103E/XX: T/R, 10 kΩ, 14-LD Device
e) MCP4332-503E/XX: 50 kΩ, 8LD Device
f) MCP4332T-503E/XX: T/R, 50 kΩ, 14-LD Device
g) MCP4332-104E/XX: 100 kΩ, 14-LD Device
h) MCP4332T-104E/XX: T/R, 100 kΩ, 14-LD Device

a) MCP4351-502E/XX: 5 kΩ, 20-LD Device
b) MCP4351T-502E/XX: T/R, 5 kΩ, 20-LD Device
c) MCP4351-103E/XX: 10 kΩ, 20-LD Device
d) MCP4351T-103E/XX: T/R, 10 kΩ, 20-LD Device
e) MCP4351-503E/XX: 50 kΩ, 20-LD Device
f) MCP4351T-503E/XX: T/R, 50 kΩ, 20-LD Device
g) MCP4351-104E/XX: 100 kΩ, 20-LD Device
h) MCP4351T-104E/XX: T/R, 100 kΩ, 20-LD Device

a) MCP4352-502E/XX: 5 kΩ, 14-LD Device
b) MCP4352T-502E/XX: T/R, 5 kΩ, 14-LD Device
c) MCP4352-103E/XX: 10 kΩ, 14-LD Device
d) MCP4352T-103E/XX: T/R, 10 kΩ, 14-LD Device
e) MCP4352-503E/XX: 50 kΩ, 14-LD Device
f) MCP4352T-503E/XX: T/R, 50 kΩ, 14-LD Device
g) MCP4352-104E/XX: 100 kΩ, 14-LD Device
h) MCP4352T-104E/XX: T/R, 100 kΩ, 14-LD Device

XX = ST for 14/20-lead TSSOP
= ML for 20-lead QFN

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