

74HC2G32; 74HCT2G32

Dual 2-input OR gate

Rev. 5 — 6 January 2014

Product data sheet

1. General description

The 74HC2G32; 74HCT2G32 is a dual 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - ◆ For 74HC2G32: CMOS level
 - ◆ For 74HCT2G32: TTL level
- Complies with JEDEC standard no. 7A
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to $+85\text{ °C}$ and -40 °C to $+125\text{ °C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G32DP 74HCT2G32DP	-40 °C to $+125\text{ °C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC2G32DC 74HCT2G32DC	-40 °C to $+125\text{ °C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HC2G32GD 74HCT2G32GD	-40 °C to $+125\text{ °C}$	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm	SOT996-2

4. Marking

Table 2. Marking code

Type number	Marking code ^[1]
74HC2G32DP	H32
74HCT2G32DP	T32
74HC2G32DC	H32
74HCT2G32DC	T32
74HC2G32GD	H32
74HCT2G32GD	T32

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

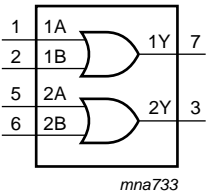


Fig 1. Logic symbol

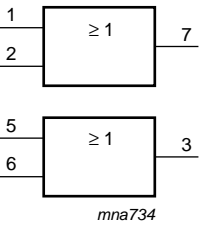


Fig 2. IEC logic symbol

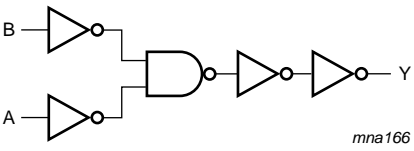


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

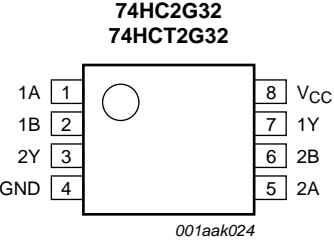


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

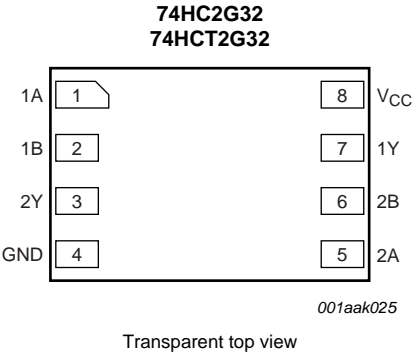


Fig 5. Pin configuration SOT996-2 (XSON8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	[1] -	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	[1] -	±20	mA
I _O	output current	$V_O = -0.5 \text{ V}$ to $(V_{CC} + 0.5 \text{ V})$	[1] -	25	mA
I _{CC}	supply current		[1] -	50	mA
I _{GND}	ground current		[1] -50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	dynamic power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
 For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
 For XSON8 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G32			74HCT2G32			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G32										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	4.18	4.32	-	4.13	-	3.7	-	V
	$I_O = -5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.68	5.81	-	5.63	-	5.2	-	V	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
	$I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	1.0	-	10	-	20	μA

Table 7. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	1.5	-	-	-	-	-	pF
74HCT2G32										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}$	4.18	4.32	-	4.13	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC} \text{ or } \text{GND}; V_{CC} = 5.5 \text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A}$	-	-	300	-	375	-	410	μA
C_I	input capacitance		-	1.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G32										
t_{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	24	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	9.0	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	7.0	13	-	16	-	20	ns
t_t	transition time	nY; see Figure 6 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	18	75	-	95	-	125	ns
		$V_{CC} = 4.5 \text{ V}$	-	6	15	-	19	-	25	ns
		$V_{CC} = 6.0 \text{ V}$		5	13	-	16	-	20	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}; f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]	-	10	-	-	-	-	-	pF

Table 8. Dynamic characteristics ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT2G32										
t_{pd}	propagation delay	nA, nB to nY; see Figure 6 [1] $V_{CC} = 4.5\text{ V}$	-	13	24	-	30	-	36	ns
t_t	transition time	nY; see Figure 6 [2] $V_{CC} = 4.5\text{ V}$	-	6	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_i = \text{GND to } V_{CC} - 1.5\text{ V}$	[3]	11	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{TLH} and t_{THL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

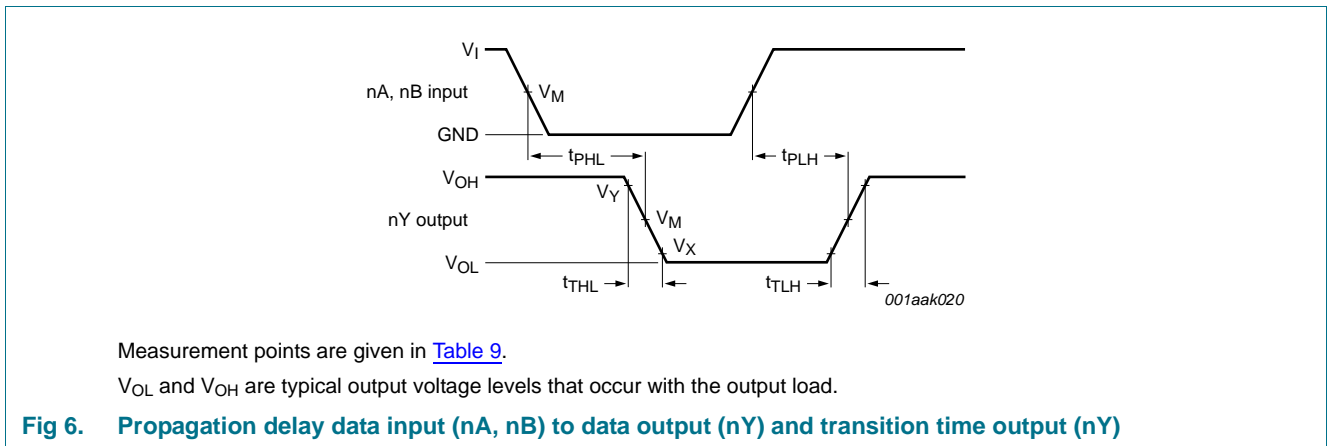
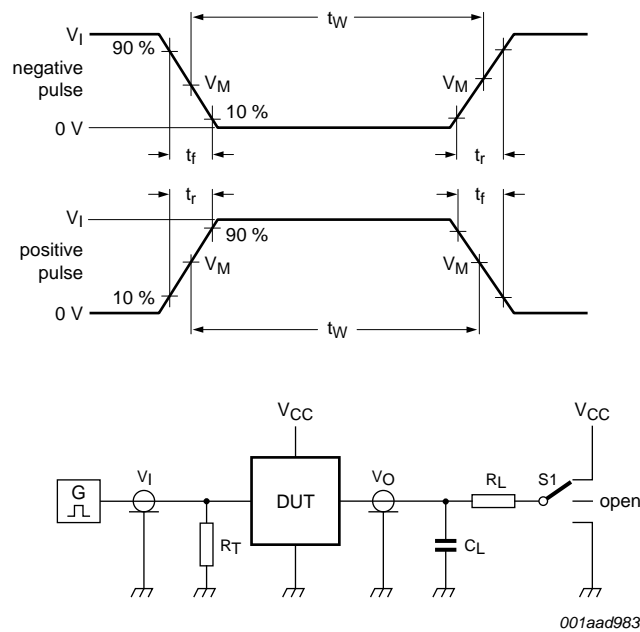


Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G32	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT2G32	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Load circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC2G32	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	open
74HCT2G32	GND to 3 V	≤ 6 ns	50 pF	1 k Ω	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

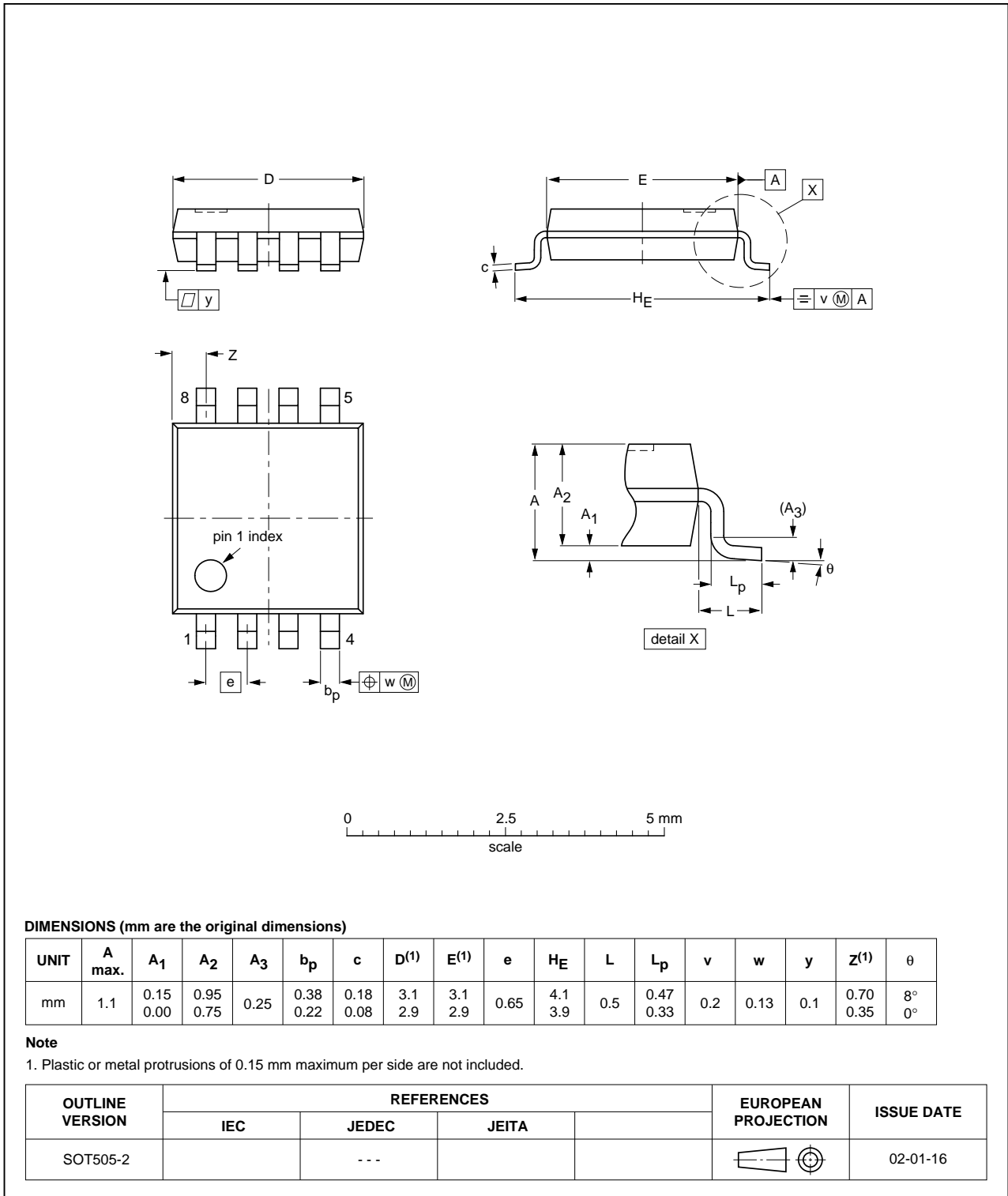


Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

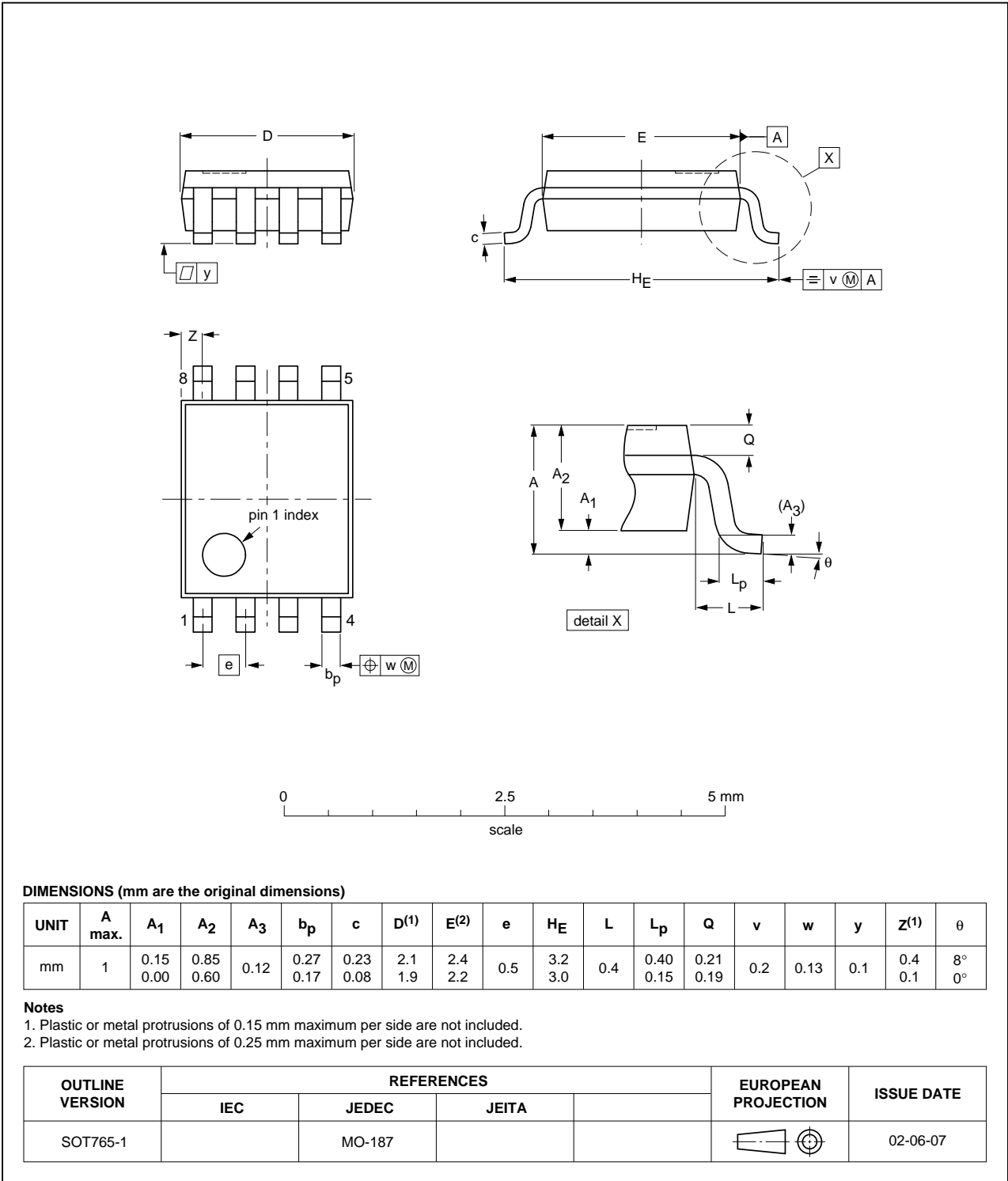


Fig 9. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

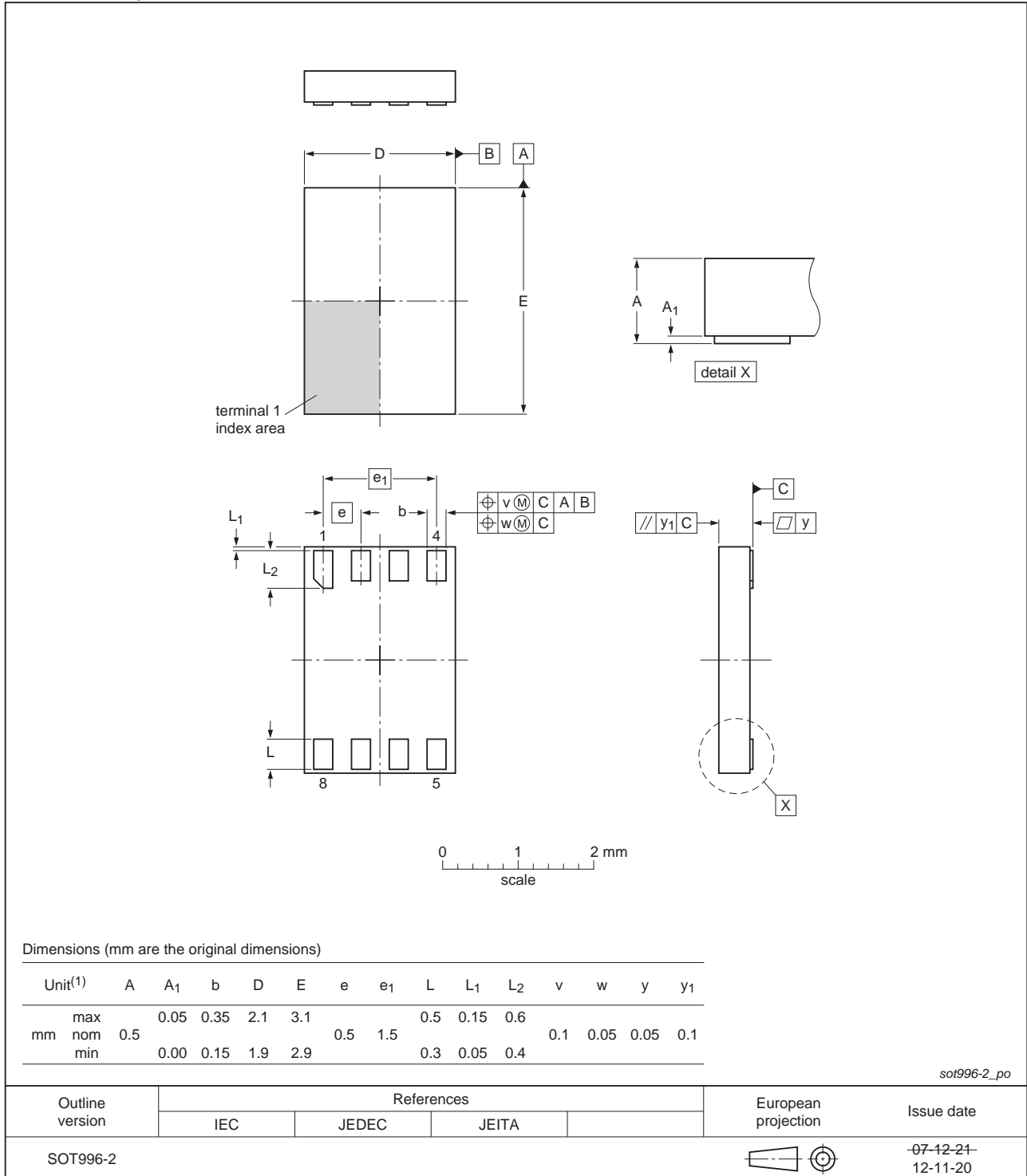


Fig 10. Package outline SOT996-2 (XSON8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G32 v.5	20140106	Product data sheet	-	74HC_HCT2G32 v.4
Modifications:	<ul style="list-style-type: none"> For 74HCT2G32 the conditions of C_{PD} are corrected to the family standard (errata). 			
74HC_HCT2G32 v.4	20130927	Product data sheet	-	74HC_HCT2G32 v.3
Modifications:	<ul style="list-style-type: none"> For type numbers 74HC2G32GD and 74HCT2G32GD XSON8U has changed to XSON8. 			
74HC_HCT2G32 v.3	20090512	Product data sheet	-	74HC_HCT2G32 v.2
74HC_HCT2G32 v.2	20031030	Product specification	-	74HC_HCT2G32 v.1
74HC_HCT2G32 v.1	20020717	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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