AOD9N50/AOI9N50

500V,9A N-Channel MOSFET

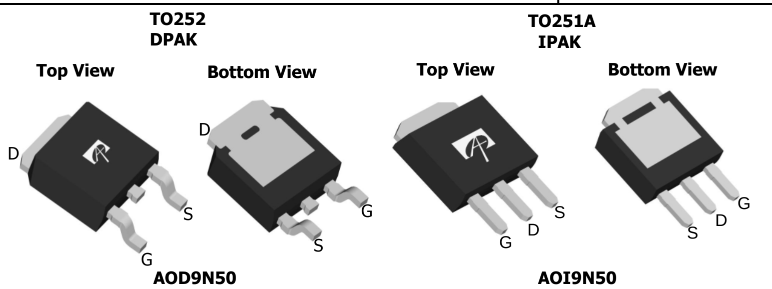
General Description

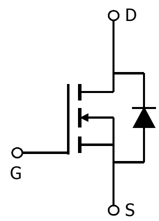
The AOD9N50 & AOI9N50 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.
By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS}	600V@150℃
I_D (at V_{GS}=10V)	9A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 0.86Ω

100% UIS Tested!
100% R_g Tested!





Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current[B]	T_C=25℃	I_D	9	A
	T_C=100℃		5.7	
Pulsed Drain Current [C]		I_{DM}	27	
Avalanche Current [C]		I_{AR}	3.8	A
Repetitive avalanche energy [C]		E_{AR}	216	mJ
Single pulsed avalanche energy [H]		E_{AS}	433	mJ
Peak diode recovery dv/dt		dv/dt	5	V/ns
Power Dissipation [B]	T_C=25℃	P_D	178	W
	Derate above 25°C		1.4	W/ °C
Junction and Storage Temperature Range		T_J, T_{STG}	-50 to 150	℃
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		T_L	300	℃

Thermal Characteristics				
Parameter	**Symbol**	**Typical**	**Maximum**	**Units**
Maximum Junction-to-Ambient [A,G]	$R_{\theta JA}$	45	55	℃/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	-	0.5	℃/W
Maximum Junction-to-Case[D,F]	$R_{\theta JC}$	0.5	0.7	℃/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C	500			V
		I_D=250µA, V_{GS}=0V, T_J=150°C		600		
BV_{DSS} /ΔTJ	Zero Gate Voltage Drain Current	ID=250µA, VGS=0V		0.56		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=500V, V_{GS}=0V			1	µA
		V_{DS}=400V, T_J=125°C			10	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±30V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=5V, I_D=250µA	3.3	3.9	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=4.5A		0.71	0.86	Ω
g_{FS}	Forward Transconductance	V_{DS}=40V, I_D=4.5A		9		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				9	A
I_{SM}	Maximum Body-Diode Pulsed Current				27	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	760	962	1160	pF
C_{oss}	Output Capacitance		65	98	130	pF
C_{rss}	Reverse Transfer Capacitance		4.5	8	12	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.5	3.2	5	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=400V, I_D=9A	15	19.5	24	nC
Q_{gs}	Gate Source Charge			4.6		nC
Q_{gd}	Gate Drain Charge			7.1		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=250V, I_D=9A, R_G=25Ω		24		ns
t_r	Turn-On Rise Time			44		ns
$t_{D(off)}$	Turn-Off DelayTime			55		ns
t_f	Turn-Off Fall Time			35		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=9A,dI/dt=100A/µs,V_{DS}=100V	260	332	400	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=9A,dI/dt=100A/µs,V_{DS}=100V	2.8	3.5	4.5	µC

A. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A=25°C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C.
G.These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.
H. L=60mH, I_{AS}=3.8A, V_{DD}=150V, R_G=10Ω, Starting T_J=25°C

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

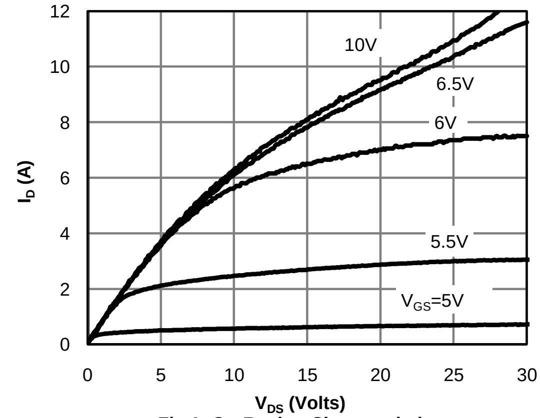


Fig 1: On-Region Characteristics

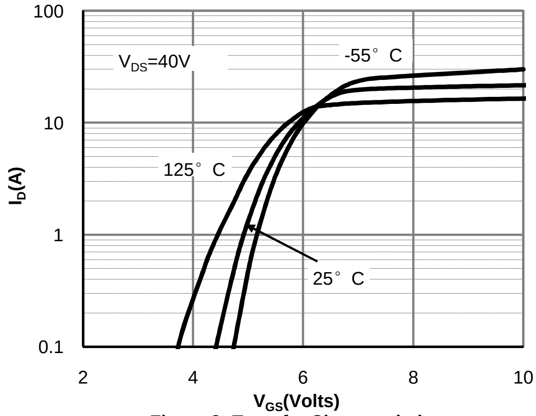


Figure 2: Transfer Characteristics

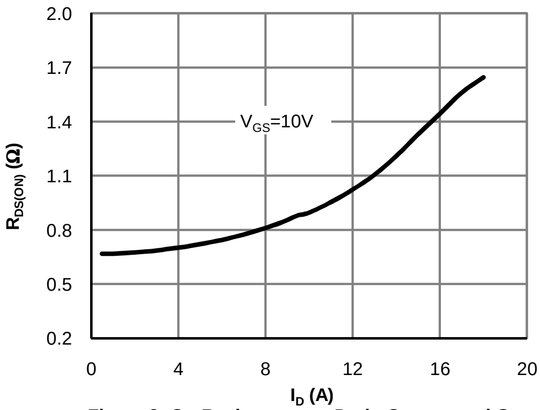


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

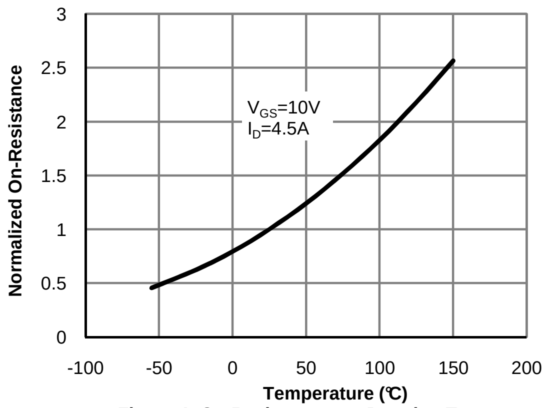


Figure 4: On-Resistance vs. Junction Temperature

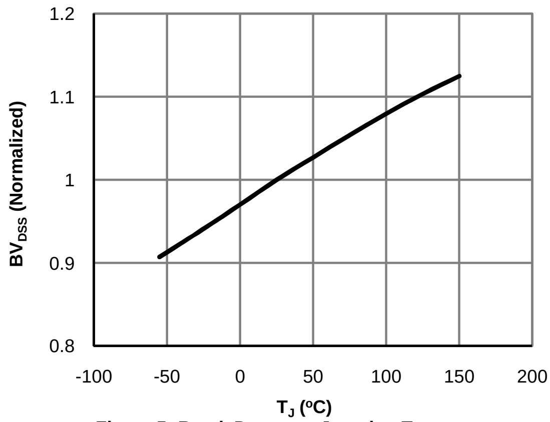


Figure 5: Break Down vs. Junction Temperature

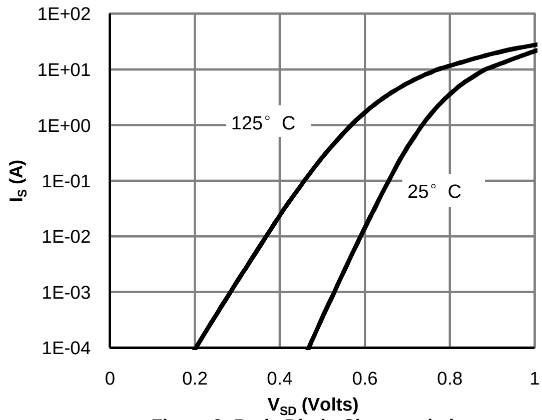


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

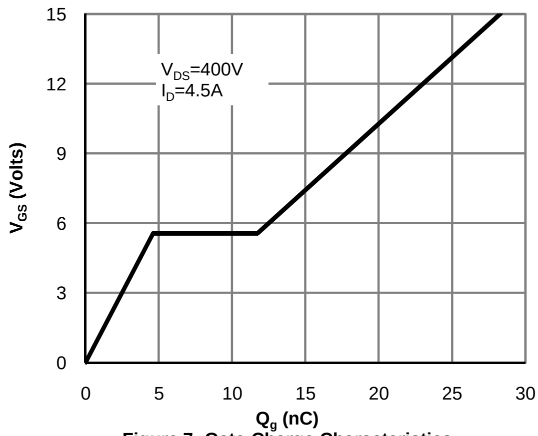


Figure 7: Gate-Charge Characteristics

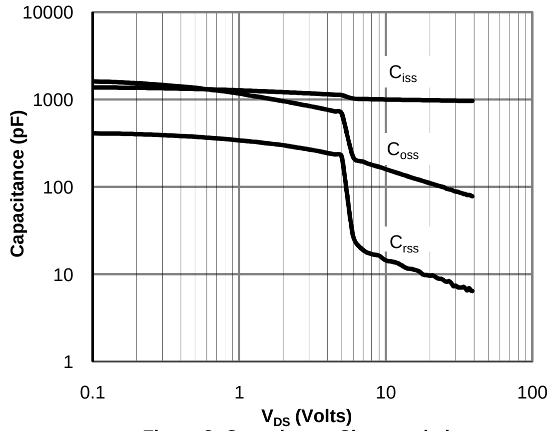


Figure 8: Capacitance Characteristics

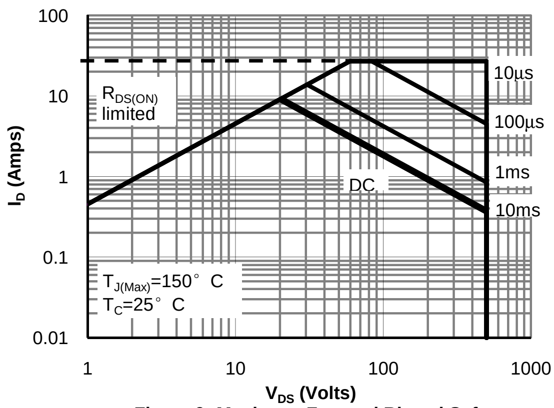


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

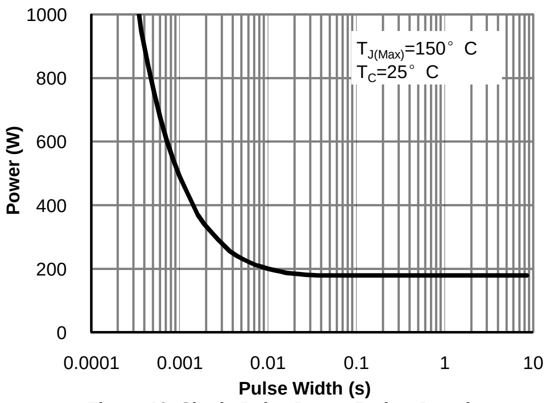


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

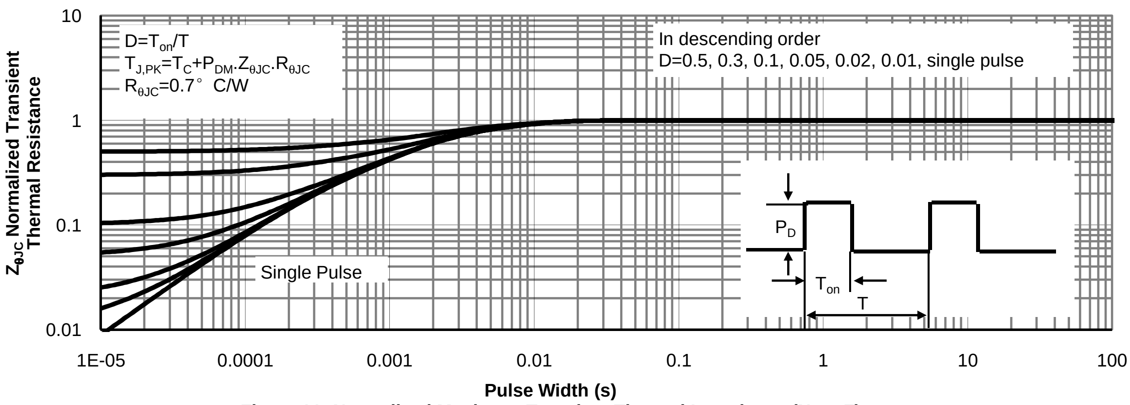


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

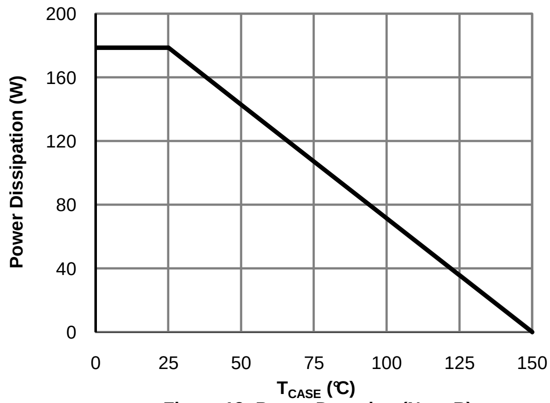


Figure 12: Power De-rating (Note B)

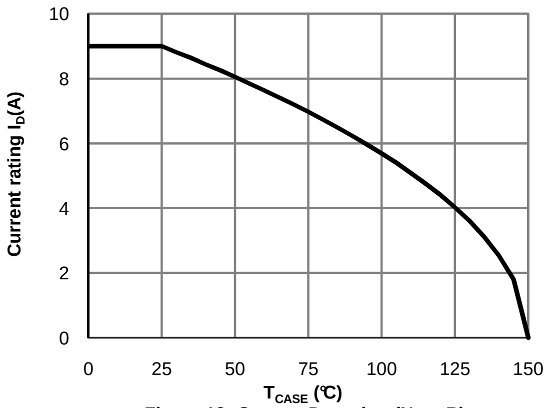


Figure 13: Current De-rating (Note B)

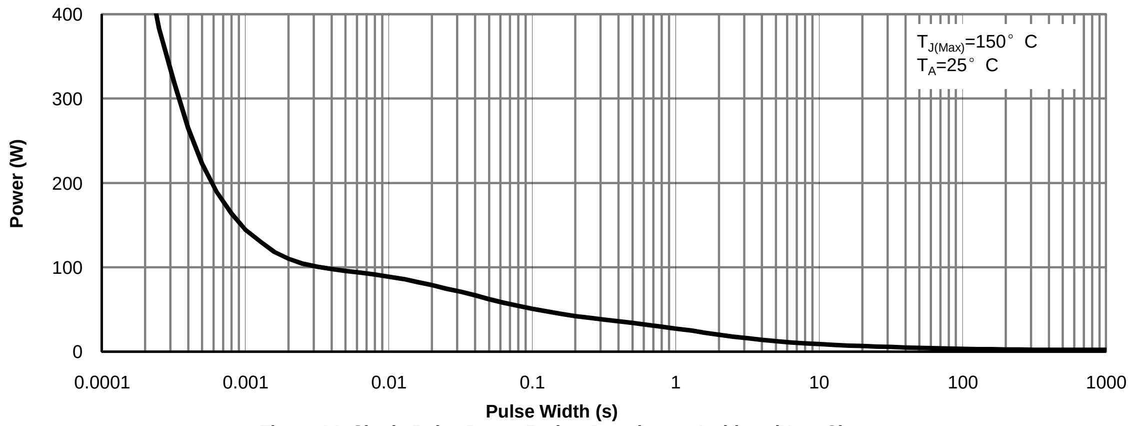


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

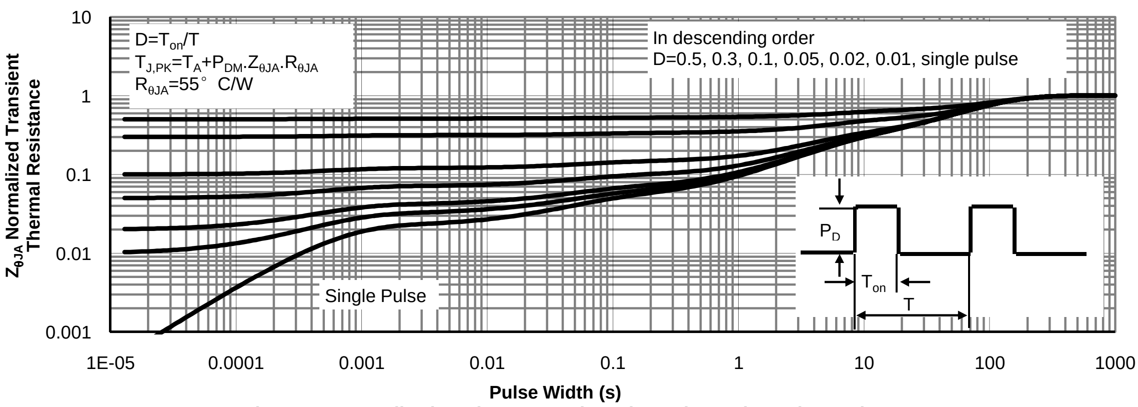
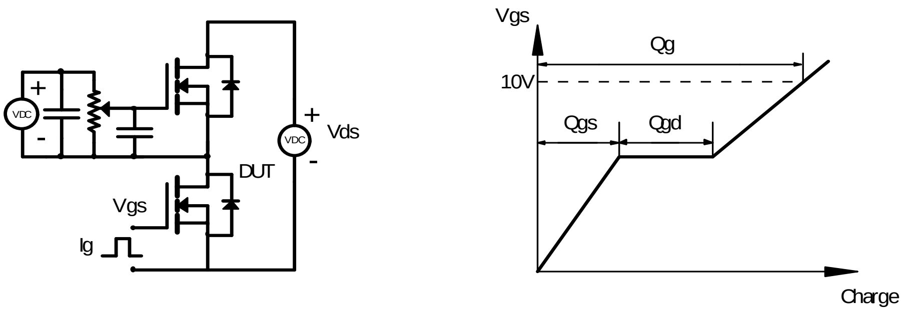
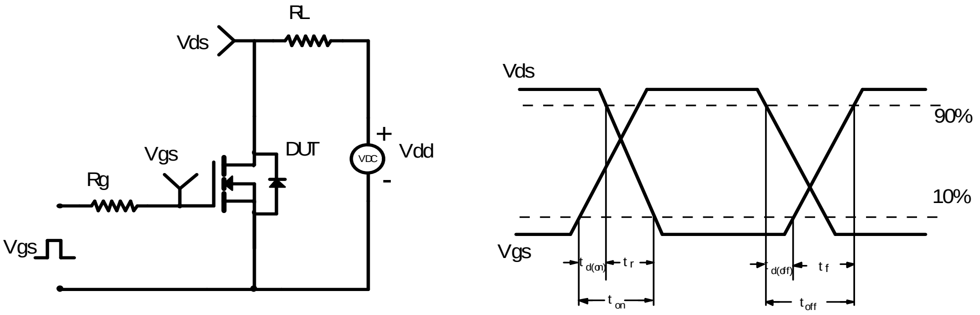


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

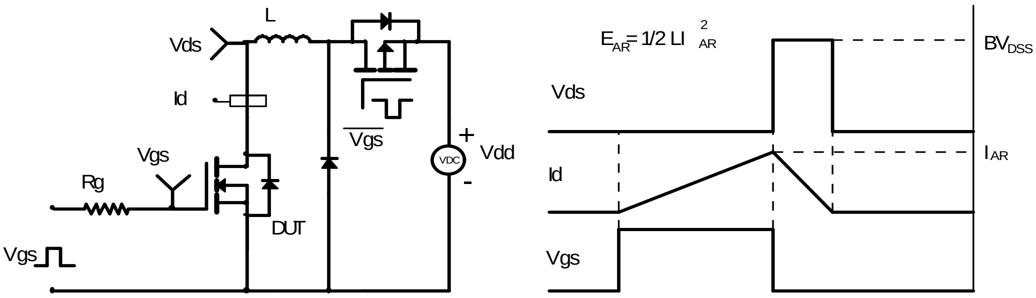
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms