Automotive-grade N-channel 600 V, 0.17 Ω typ., 17 A FDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data

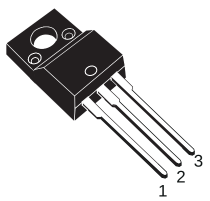
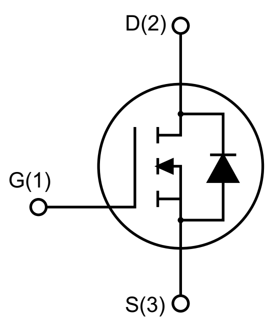


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STF22NM60ND	650 V	0.22 Ω	17 A

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This FDmesh™ II Power MOSFET with fast-recovery body diode is produced using MDmesh™ II technology. Utilizing a new strip-layout vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order code	Marking	Package	Packing
STF22NM60ND	22NM60ND	TO-220FP	Tube

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	±25	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	17	A
	Drain current (continuous) at T_C = 100 °C	10	
I_{DM}(1)(2)	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
dv/dt(3)	Peak diode recovery voltage slope	40	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C= 25 °C)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_J	Operating junction temperature		

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq$ 17 A, di/dt $\leq$ 600 A/µs, V_{DD} = 80% $V_{(BR)DSS;}$ $V_{DS(peak)} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.17	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	8.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	610	mJ

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
dv/dt(1)	Drain source voltage slope	V_{DD}= 480 V, I_D= 17 A, V_{GS}= 10 V		36		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			10	µA
		V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A		0.170	0.220	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1800	-	pF
C_{oss}	Output capacitance			90		pF
C_{rss}	Reverse transfer capacitance			8		pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	300	-	pF
$t_{d(on)}$	Turn-on delay time	V_{DD} =300 V, I_D = 8.5 A R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 19)*, *(see Figure 14)*	-	18	-	ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turn-off delay time			70		ns
t_f	Fall time			48		ns
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 17 A, V_{GS} = 10 V, *(see Figure 15)*	-	60		nC
Q_{gs}	Gate-source charge			13		nC
Q_{gd}	Gate-drain charge			30	-	nC
R_G	Gate input resistance	f =1 MHz Gate DC Bias=0 Test signal level = 20 mV Open drain	-	3	-	Ω

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				17	A
I_{SDM} (1)	Source-drain current (pulsed)				68	A
V_{SD} (2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, V_{DD} = 60 V di/dt=100 A/µs *(see Figure 16)*		150		ns
Q_{rr}	Reverse recovery charge			0.90		µC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A,V_{DD} = 60 V di/dt=100 A/µs, T_J = 150 °C *(see Figure 16)*		240		ns
Q_{rr}	Reverse recovery charge			2		µC
I_{RRM}	Reverse recovery current			16		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

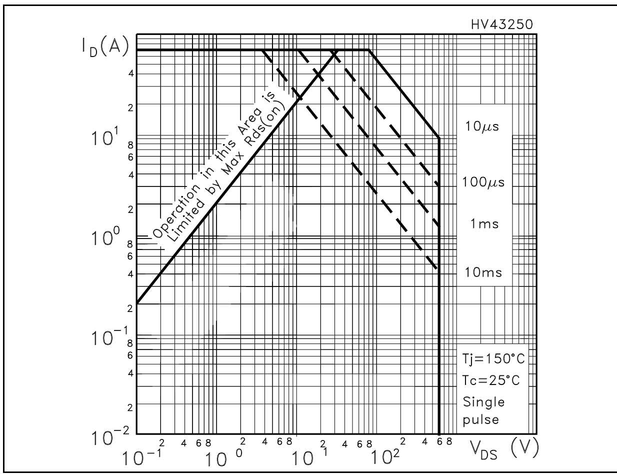


Figure 3. Thermal impedance

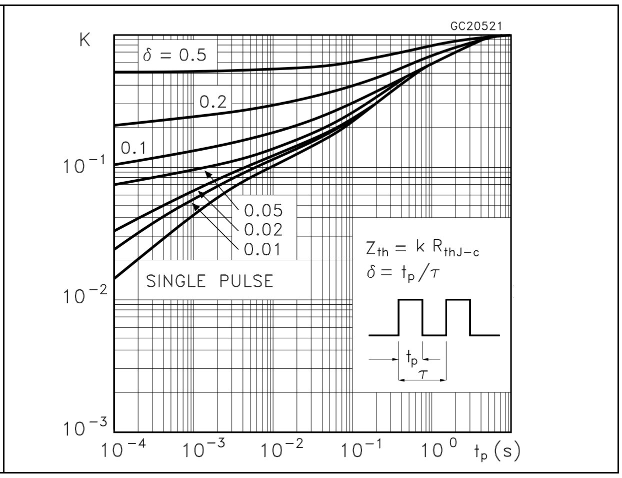


Figure 4. Output characteristics

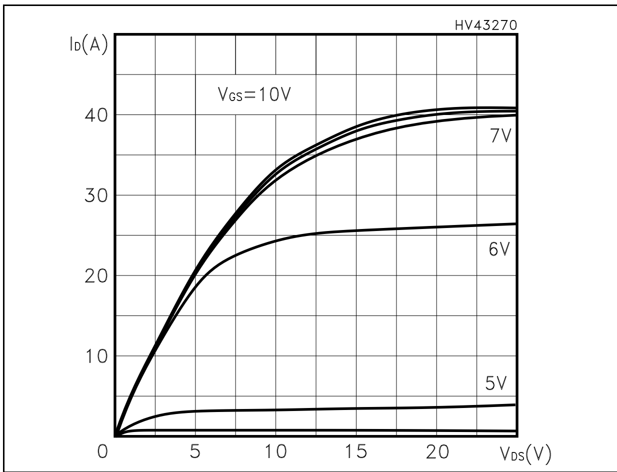


Figure 5. Transfer characteristics

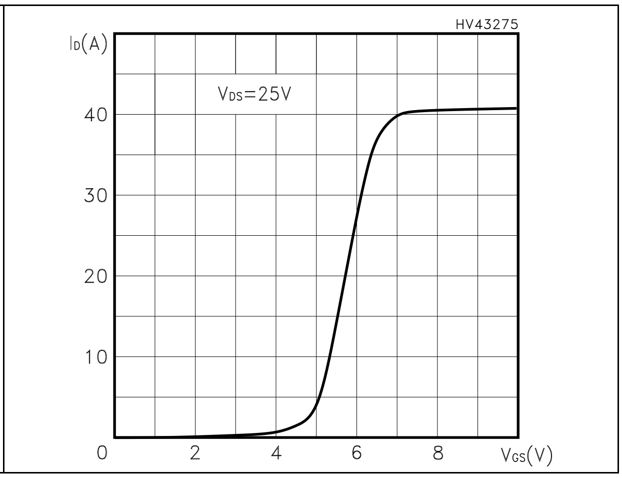


Figure 6. Transconductance

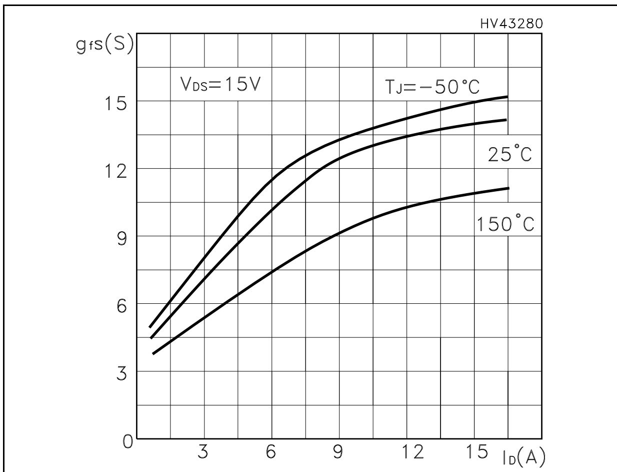


Figure 7. Static drain-source on-resistance

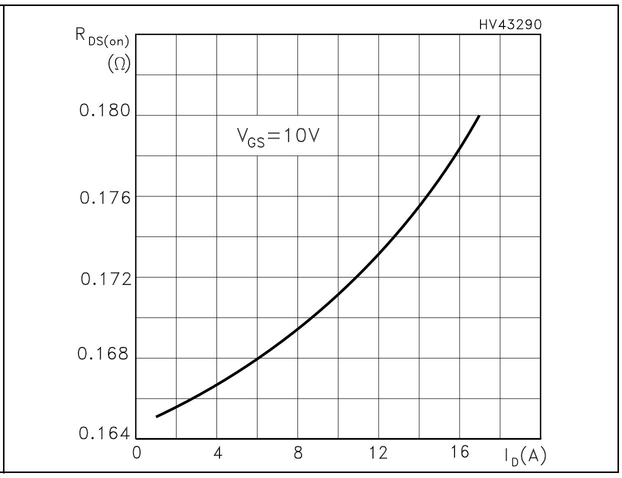


Figure 8. Gate charge vs gate-source voltage

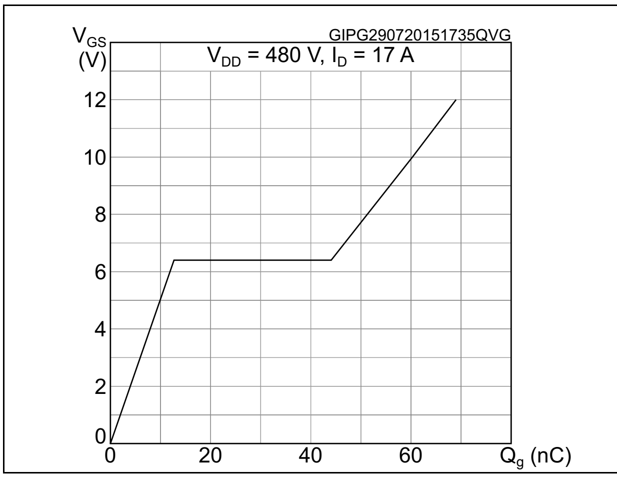


Figure 9. Capacitance variations

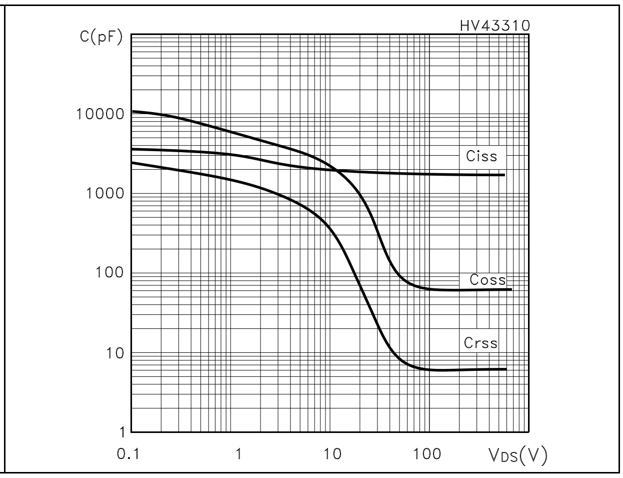


Figure 10. Normalized gate threshold voltage vs temperature

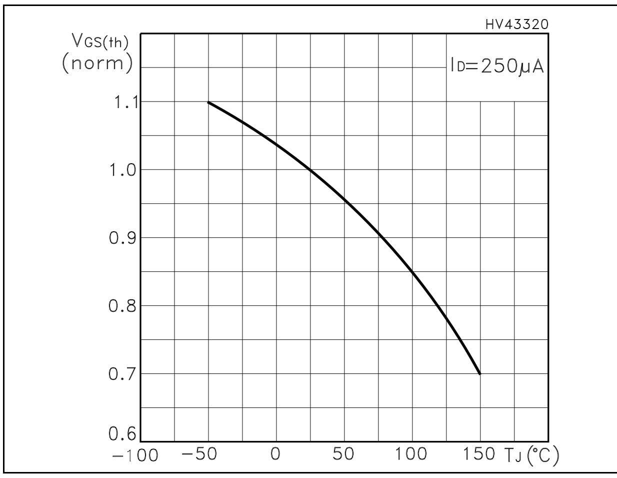


Figure 11. Normalized on-resistance vs temperature

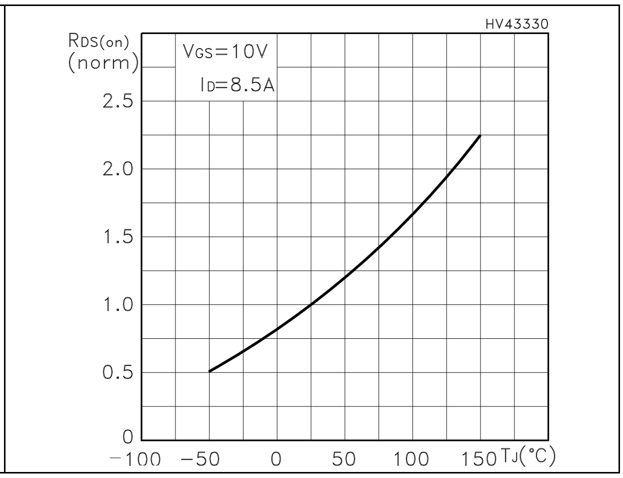


Figure 12. Source-drain diode forward characteristics

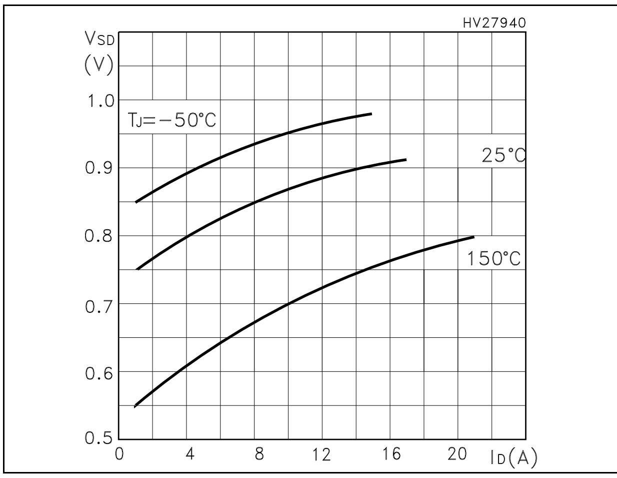
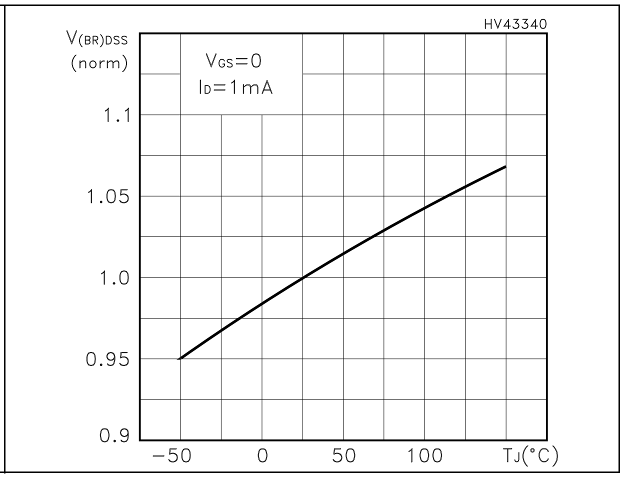


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

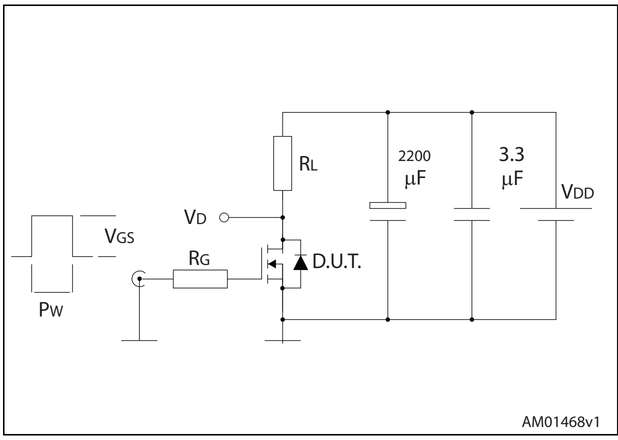


Figure 15. Gate charge test circuit

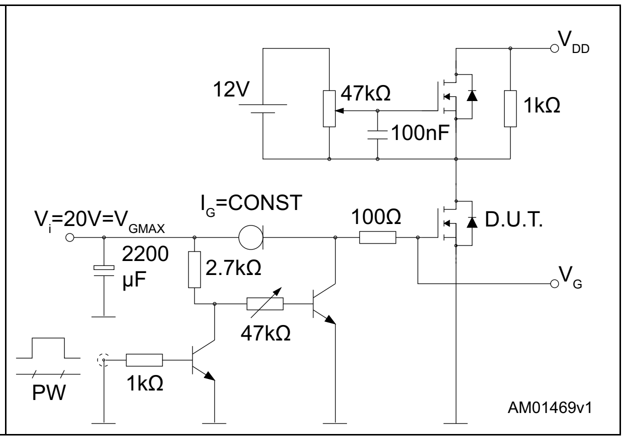


Figure 16. Test circuit for inductive load switching and diode recovery times

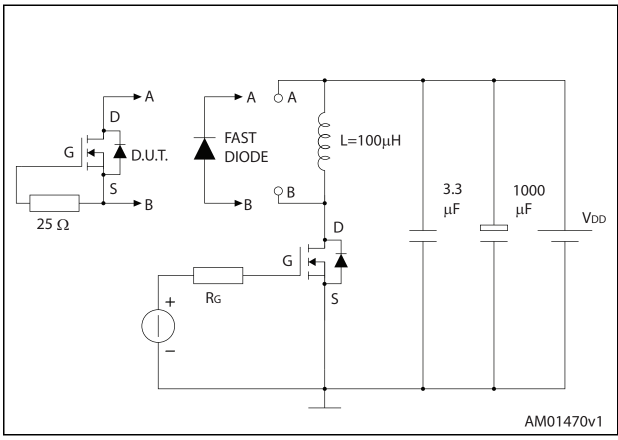


Figure 17. Unclamped inductive load test circuit

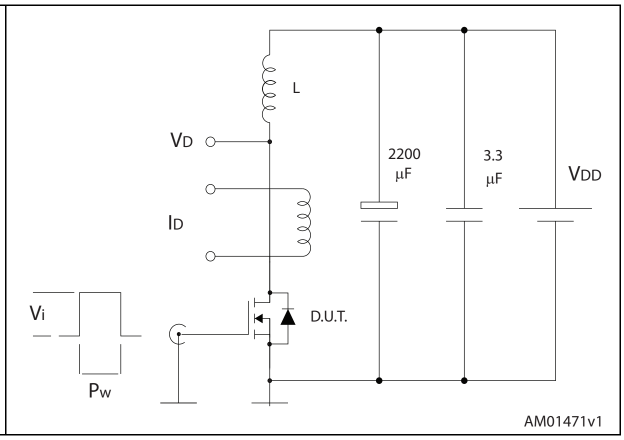


Figure 18. Unclamped inductive waveform

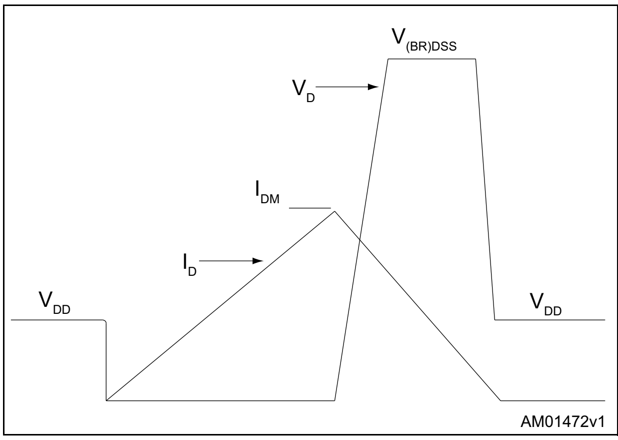
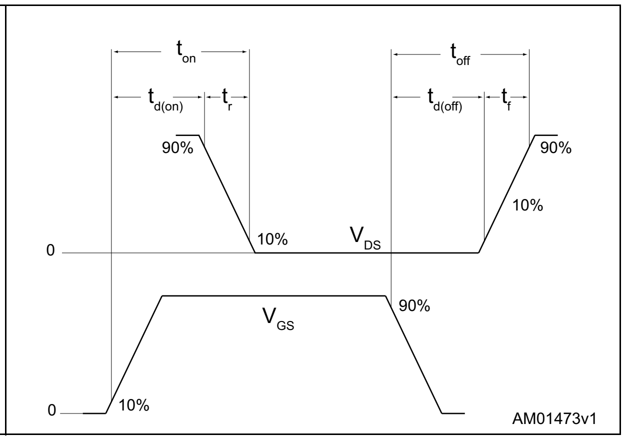


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline

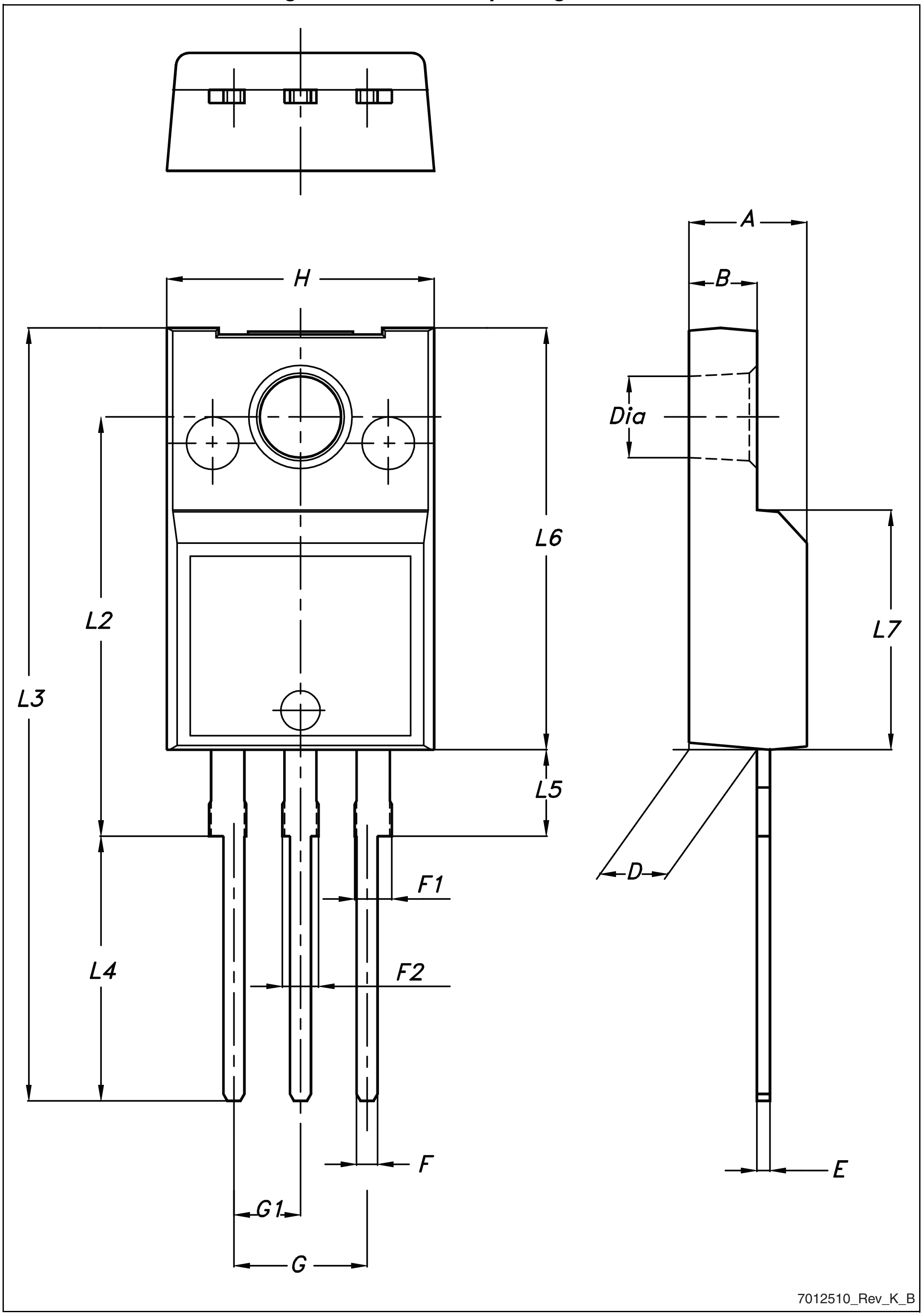


Table 8. TO-220FP package mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Sep-2014	1	First release.
03-Aug-2015	2	Text edits throughout document. Datasheet status promoted from preliminary to production data. Updated *Table 5*, *Table 6* and *Table 7* Updated *Figure 8* Updated *Section 3: Test circuits*