SYNCHRONOUS MOSFET CONTROLLER IN SO-8

Description

The ZXGD3110N8 is intended to drive a MOSFET configured as an ideal diode replacement. The device is comprised of a high voltage detector stage and gate driver. The detector monitors the voltage between the drain and the source of the MOSFET and if this voltage is less than the turn on threshold voltage of the controller a positive voltage is applied to the MOSFET's Gate Pin. As the load current decays to zero and the voltage between the drain and source of the MOSFET increases beyond the turn-off threshold value MOSFET is rapidly turned off.

Intelligent features of this IC are the Minimum Off-Time (T_{OFF}) and Minimum On-Time (T_{ON}), these features blanket the noise generated during the turn-on and turn-off instances of the power FET. Also Light Load Detection (LLD) for improved efficiency at light and no load, where synchronous rectification is no more beneficial. Other features include Undervoltage Lockout (UVLO), SYNC feature for CCM operation and low turn-off threshold voltage for improved efficiency.

Features

- Frequency of Operation up to 500kHz
- Suitable for Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM) and Critical (CrCM) Conduction Mode
- Minimum On-Time and Off-Time to Reduce Turn-On/Off Oscillations
- Intelligent Light Load Detection and Sleep Mode
- Turn-Off Propagation Delay Time 30ns
- Drain Voltage Rating of 200V
- Recommended Operating Voltage from 4.5V up to 12V
- Source and Sink Current of 2A and 4A Respectively
- Low Component Count
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

Applications

Flyback Converters in:

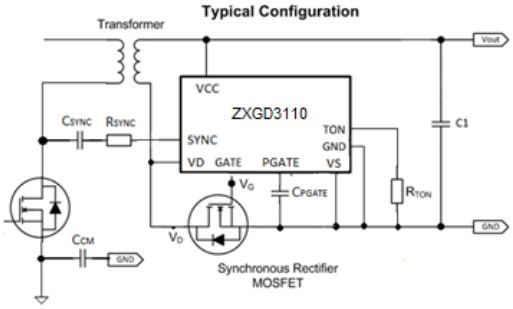
- Power Adaptors
- Auxiliary Power Supplies
- PoE Power Devices

Resonant Converters in:

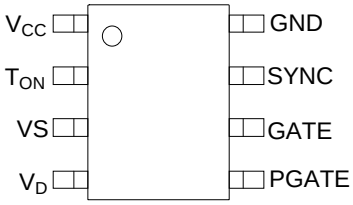
- High Power Adaptors
- 85+/90+ Compliant ATX and Server Power Supplies

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)



SO-8
Top View



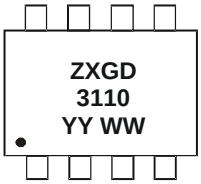
Top View
Pin-Out

Ordering Information (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
ZXGD3110N8TC	ZXGD3110	13	12	2,500

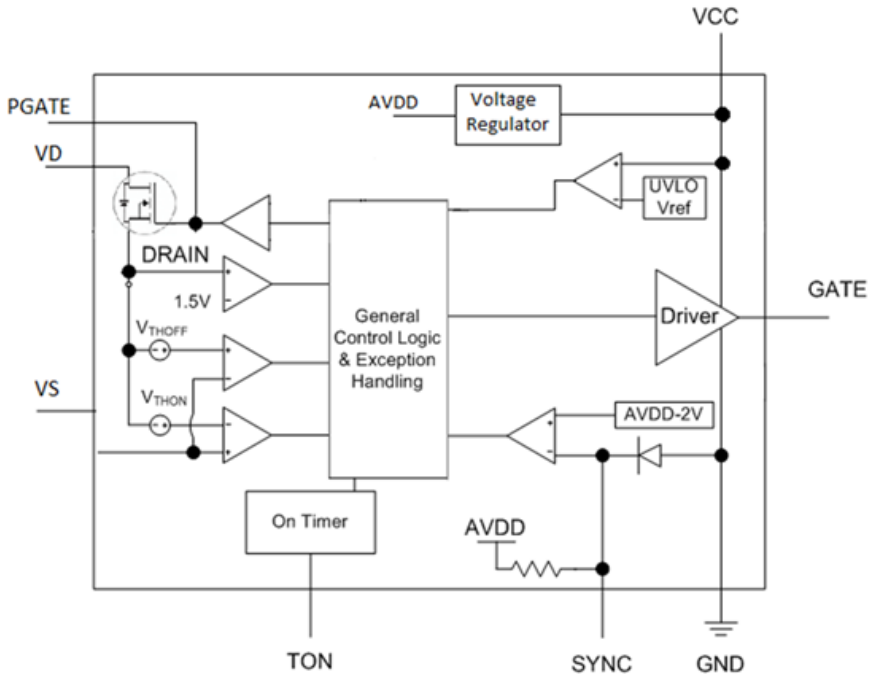
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free,"Green" and Lead-Free.
3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



ZXGD = Product Type Marking Code, Line 1
3110 = Product Type Marking Code, Line 2
YY = Year (ex: 15 = 2015)
WW = Week (01 - 53)

Functional Block Diagram



Pin Descriptions

Pin Number	Pin Name	Function
1	V_{CC}	**Power Supply Pin** V_{CC} supplies all the internal circuitry of the device. A DC supply is required to be connected to this pin. A 10µF or larger capacitor must be connected between this pin and GND Pin as close as possible. The device will not function until the V_{CC} has risen above the UVLO threshold. The device can safely be turned off by bringing V_{CC} below the UVLO threshold (minus the UVLO threshold hysteresis). If V_{CC} drops below the UVLO threshold (minus UVLO threshold hysteresis), the MOSFET is turned off and the $T_{OFF}/_{ON}$ Pin is internally connected to GND.
2	T_{ON}	**Minimum On-Time** Minimum on-time setting pin. Connect this pin to Ground via R_{TON} resistor.
3	V_S	**Source Voltage** Connect this pin to the source of the synchronous MOSFET.
4	V_D	**Drain Voltage** This pin needs to be connected as closely as possible to the transformer used in the application, to minimize the effects of parasitic inductance on the performance of the device. The device requires that V_D has a voltage greater than 1.5V and that the T_{OFF} timer has expired before the MOSFET is able to be activated. Once these conditions are met and the voltage sensed on the V_D Pin is 150mV lower than the V_S Pin, the gate output to the sync MOSFET will go high and the T_{ON} (minimum on-time) period is started. The MOSFET will remain on for at least the length of the minimum on-time. After the T_{ON} period, the MOSFET will remain on until the V_D to V_S voltage has reached to the V_{THOFF} threshold, at which point the gate output will go low. If the V_{THOFF} threshold is reached before the T_{ON} period has expired, the device will enter the Light Load Mode. Under this mode, the MOSFET will not be turned on the next switching cycle. The device will come out of light load, once the on-time of the synchronous MOSFET exceeds the set minimum on-time.
5	PGATE	**Protection MOSFET Gate** A 100nF capacitor should be connected between this pin and GND.
6	GATE	**Gate** Connect GATE to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The gate output can source >2A peak source current while turning on the sync MOSFET and can sink >4A peak current while turning on the sync MOSFET.
7	SYNC	**Gate Turn-Off Synchronization** If a falling edge is sensed on this pin, the gate output is pulled low, irrespective of the sensed drain to source voltage or the state of the T_{ON} timer. This characteristic allows the device to be easily used in a Continuous Conduction Mode (CCM) system. The SYNC Pin needs to be connected to a suitable control signal on the primary side of the convertor, using a high voltage isolation cap, transformer or other suitable means.
8	GND	**Ground** This is the reference potential for all internal comparators and thresholds. A 10µF decoupling capacitor is required to place as close as possible between V_{CC} and GND Pins.

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply Voltage, Relative to GND	V_{CC}	-0.3 to 15	V
Drain Pin Voltage	V_D	-1 to +200	V
Gate Output Voltage	V_G	12	V
Minimum Off-Time (T_{OFF}) Pin Voltage	SYNC	-0.3 to 6	V
Minimum On-Time (T_{ON}) Pin Voltage	V_{TON}	-0.3 to 6	V
Gate Driver Peak Source Current	I_{SOURCE}	5	A
Gate Driver Peak Sink Current	I_{SINK}	5	A
Input Voltage Range V_S	V_S	-1 to 1	V

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Power Dissipation Linear Derating Factor	(Note 5)	P_D	490 3.92	mW mW/°C
	(Note 6)		655 5.24	
	(Note 7)		720 5.76	
	(Note 8)		785 6.28	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	255	°C/W
	(Note 6)		191	
	(Note 7)		173	
	(Note 8)		159	
Thermal Resistance, Junction to Lead	(Note 9)	$R_{\theta JL}$	55	°C/W
Thermal Resistance, Junction to Case	(Note 10)	$R_{\theta JC}$	45	°C/W
Maximum Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-65 to +150	

ESD Ratings (Note 11)

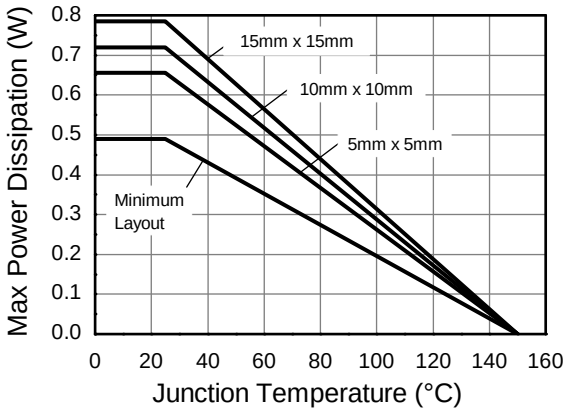
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge – Human Body Model	ESD HBM	2,000	V	1C
Electrostatic Discharge – Machine Model	ESD MM	500	V	C

Notes:
5. For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as Note (5), except Pin 1 (V_{CC}) and Pin 8 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
7. Same as Note (6), except both heatsinks are 10mm x 10mm.
8. Same as Note (6), except both heatsinks are 15mm x 15mm.
9. Thermal resistance from junction to solder-point at the end of each lead on Pin 1 (V_{CC}) and Pin 8 (GND).
10. Thermal resistance from junction to top of the case.
11. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Range	4.5	12	V
V_{DS}	Voltage Cross Drain and Source	-1	200	
F_{SW}	Switching Frequency	20	600	kHz
T_J	Operating Junction Temperature Range	-40	+125	°C
R_{TON}	T_{ON} Resistor Value	8.25	100	kΩ
C_{VCC}	V_{CC} Bypass Capacitor	10	—	µF
TW_{sync}	Sync Pulse Width	20	—	ns

Thermal Derating Curve



Derating Curve

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

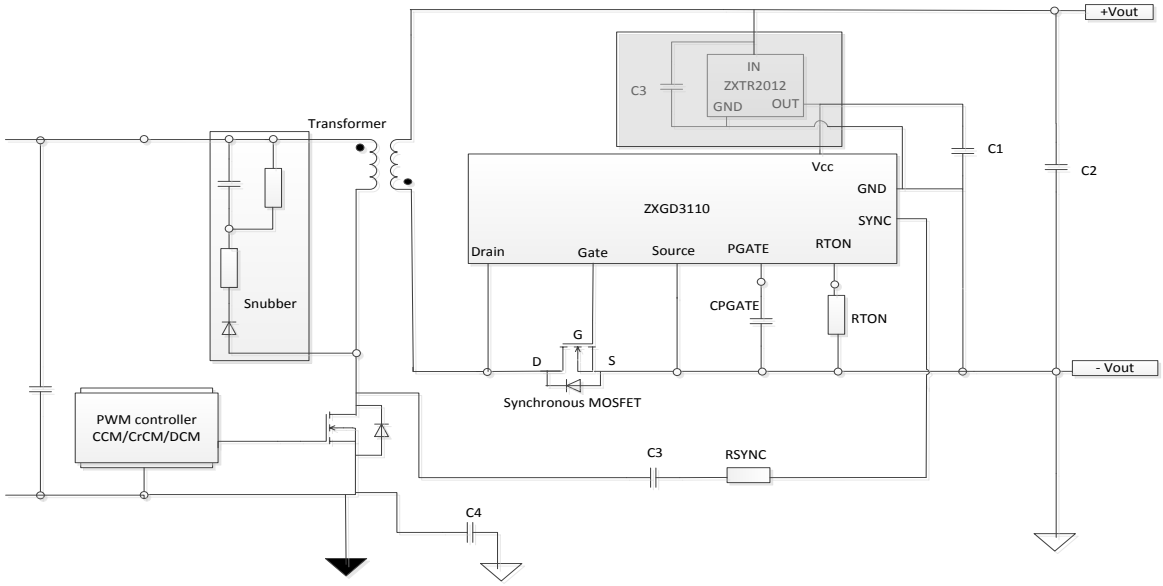
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVDD}	Internal Regulator Output	V_{CC} = 5.5V	—	4.5	—	V
		V_{CC} = 12V	—	4.7	—	V
ICC_{START}	Supply Current (Undervoltage)	V_{CC} = 2.6V	—	160	220	µA
ICC_{ON}	Supply Current (Enabled)	V_{CC} = 5.5V, F_{SW} = 100kHz C_{GATE} = 0pF	—	1.5	1.8	mA
		V_{CC} = 12V, F_{SW} = 100kHz C_{GATE} = 0pF	—	1.8	2.2	
		V_{CC} = 5.5V, F_{SW} = 100kHz C_{GATE} = 3,300pF	—	3.2	4	
		V_{CC} = 12V, F_{SW} = 100kHz C_{GATE} = 3,300pF	—	5	7	
Undervoltage Lockout (UVLO)						
$UVLO_{TH}$	V_{CC} Undervoltage Lockout Threshold Rising	—	2.8	3.0	3.20	V
$UVLO_{HYS}$	V_{CC} Undervoltage Lockout Threshold Hysteresis	—	—	200	—	mV
MOSFET Voltage Sensing						
V_{THARM}	Gate Re-Arming Threshold	V_D to GND, Rising	-1.3	-1.5	-1.7	V
V_{THON}	Gate Turn-On Threshold	(V_D-V_S) Falling, V_S = 0V	-220	-150	-80	mV
$V_{THOFFLV}$	Gate Turn-Off Threshold	(V_D-V_S) Rising, V_S = 0V, V_{CC} < 4.3V	-30	-20	-10	mV
$V_{THOFFHV}$	Gate Turn-Off Threshold	(V_D-V_S) Rising, V_S = 0V, V_{CC} > 4.3V	-10	-4	-1	mV
$T_{D(ON)}$	Gate Turn-On Propagation Delay	From V_{THON} to Gate > 1V	—	30	52	ns
$T_{D(OFF)}$	Gate Turn-Off Propagation Delay	From V_{THOFF} to Gate < 4V	—	30	62	ns
Minimum On-Time						
T_{ON-LR}	Minimum On-Time Low Resistance	R_{TON} = 8.25kΩ	0.26	0.34	0.42	µs
T_{ON-HR}	Minimum On-Time High Resistance	R_{TON} = 100kΩ	2.2	3	3.8	µs
Synchronization						
V_{THSYNC}	SYNC Falling Threshold	Gate Output from High to Low	V_{AVDD}-2.4	V_{AVDD}-2.0	V_{AVDD}-1.6	V
T_{SDLY}	SYNC Propagation Delay (Note 8)	SYNC Falling to Gate Falling 10%, 4.5V < V_{CC} < 5.5V	—	40	—	ns
R_{SYNC}	SYNC Pull Up Resistance (Note 8)	Internal Resistance from SYNC to V_{CC}, 4.5V < V_{CC} < 5.5V	—	2.0	—	kΩ

Electrical Characteristics (Continued) (@T_A = +25°C, unless otherwise specified.)

Gate Driver						
R_{GUP}	Gate Pull-Up Resistance Enabled	I_{GATE} = -100mA	—	2.3	—	Ω
R_{GDN}	Gate Pull-Down Resistance Enabled	I_{GATE} = 100mA	—	1.1	—	
I_{SOURCE}	Peak Gate Source Current	C_{GATE} = 22nF	—	3	—	A
I_{SINK}	Peak Gate Sink Current	C_{GATE} = 22nF	—	4	—	
V_{OHG}	Gate Output High Voltage	V_{CC} = 5V	4.7	—	—	V
		V_{CC} = 12V	9	—	—	
V_{OLG}	Gate Output Low Voltage	V_{CC} = 5V	—	—	0.3	
T_{FGATE}	Gate Fall Time	4V to 1V, C_{GATE} = 3,300pF, V_{CC} = 5V	—	14	42	ns
		9V to 1V, C_{GATE} = 3,300pF, V_{CC} = 12V	—	20	42	
T_{RGATE}	Gate Rise Time	1V to 4V, C_{GATE} = 3,300pF, V_{CC} = 5V	—	16	42	
		1V to 9V, C_{GATE} = 3,300pF, V_{CC} = 12V	—	20	42	
Exception Handling						
T_{OVER}	Overtemperature	—	—	+150	—	°C
$T_{RECOVER}$	Temperature to Recover from Overtemperature Exception	—	—	+125	—	°C

Typical Application Circuit

Less than 12V rails can be directly connected to the Vcc. For more than 12V operation, a regulator arrangement is suggested in the figure.



C3 of 1µF must be connected

CPGATE of 0.1µF must be connected

C1 of >10µF must be connected as close as possible to Vcc and ground with minimum track length

Typical Performance Characteristics

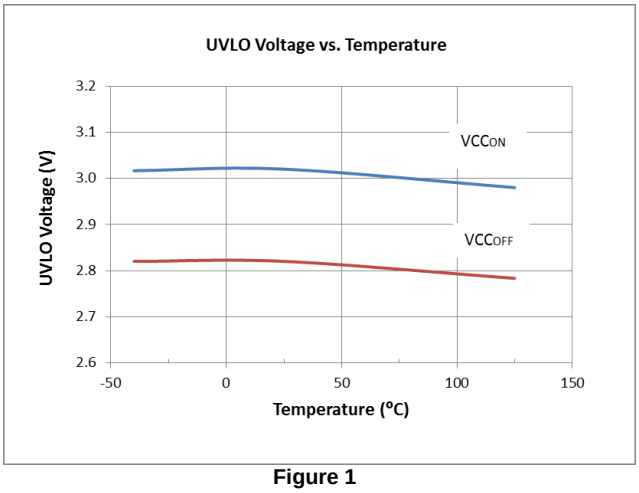


Figure 1

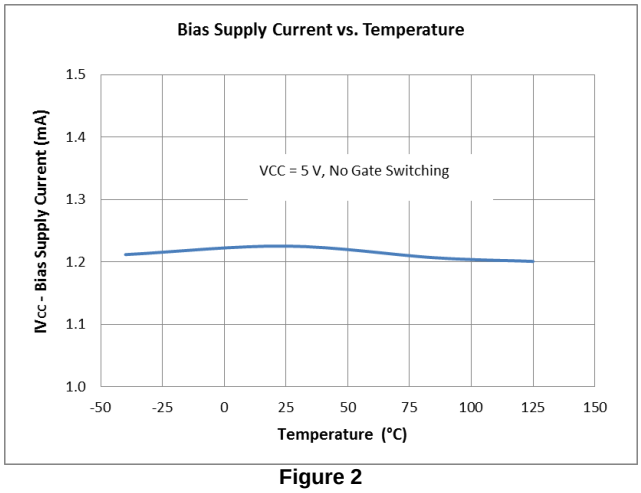


Figure 2

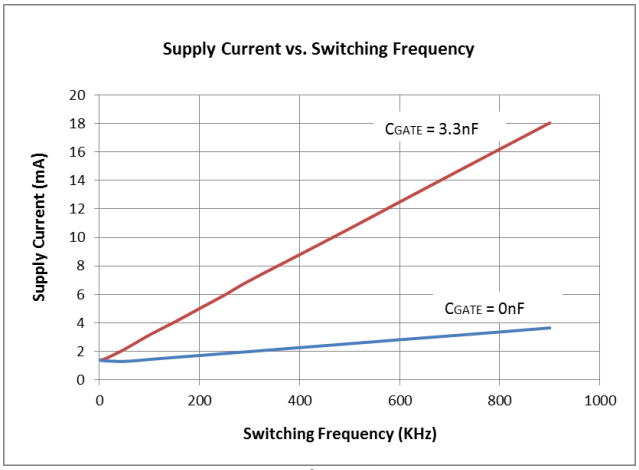


Figure 3

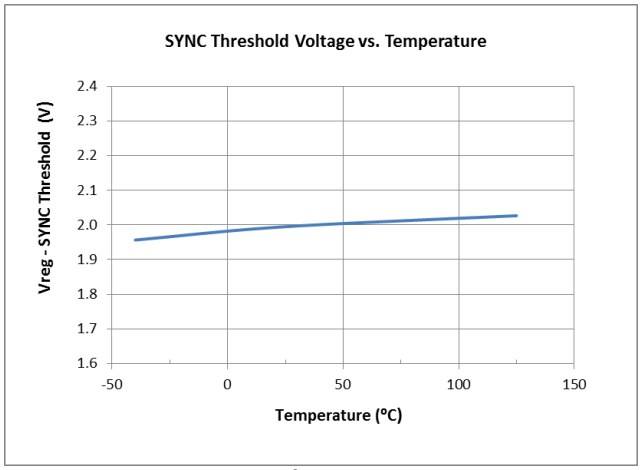


Figure 4

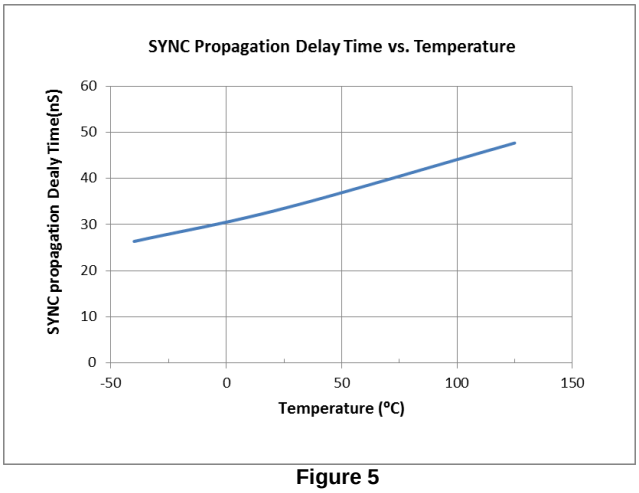


Figure 5

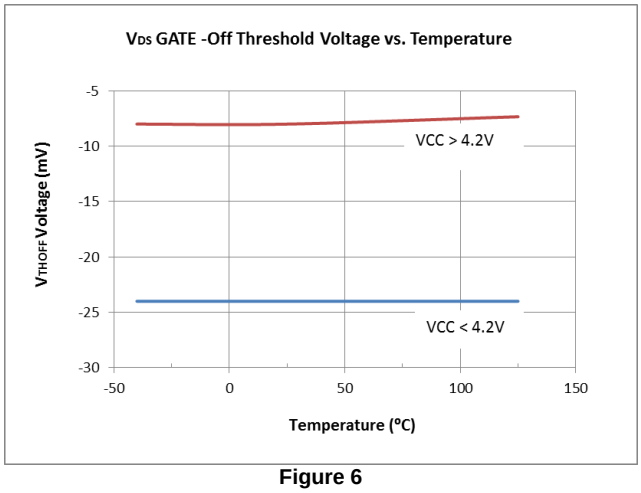


Figure 6

Typical Performance Characteristics (Continued)

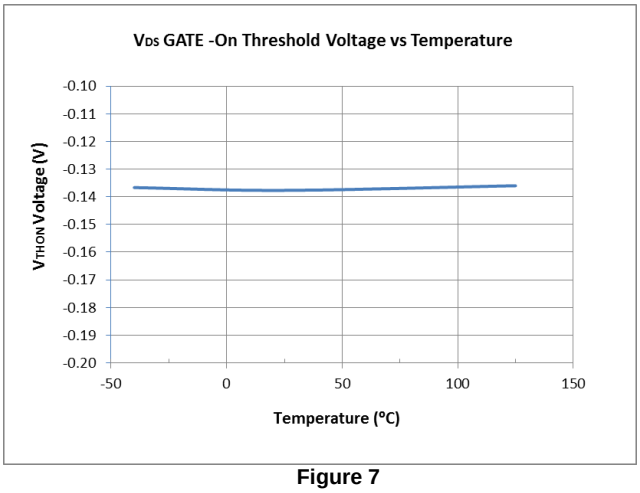


Figure 7

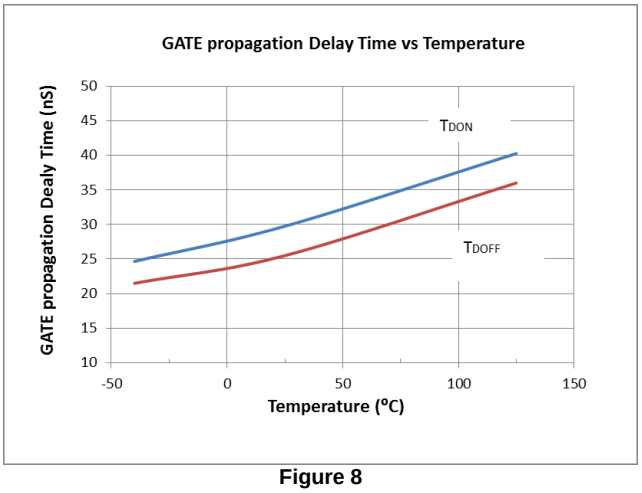


Figure 8

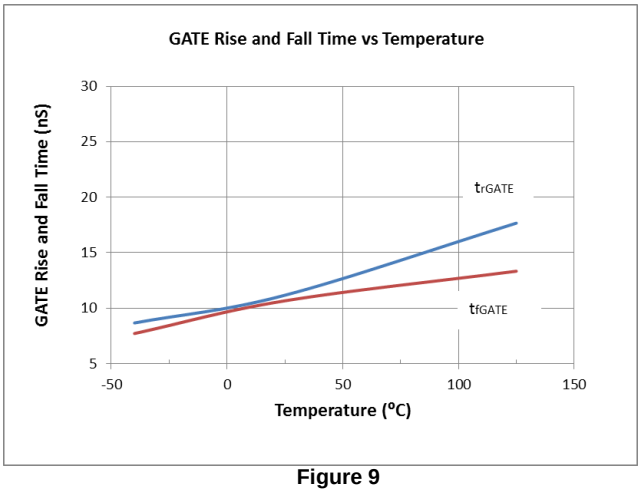


Figure 9

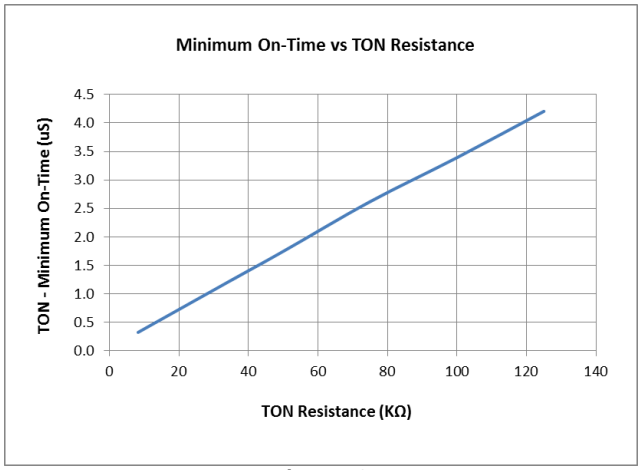


Figure 10

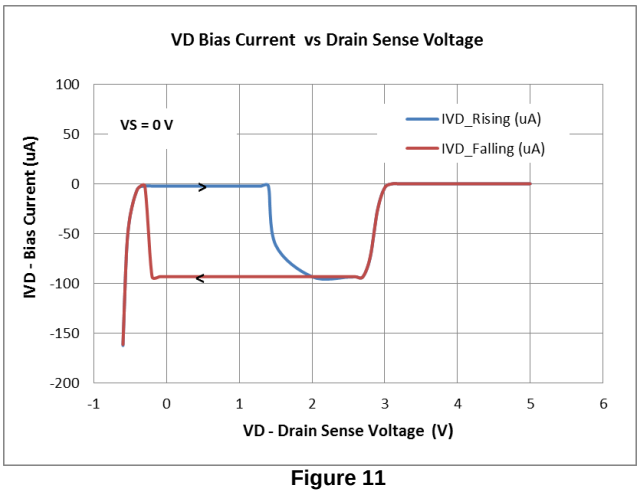
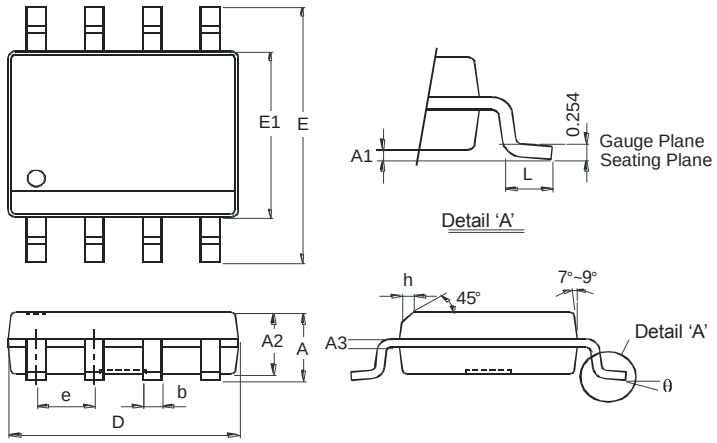


Figure 11

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

SO-8

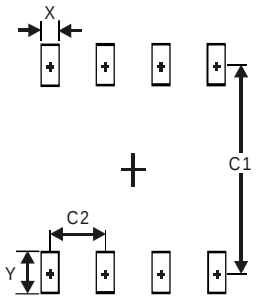


SO-8		
Dim	**Min**	**Max**
A	—	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	—	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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