ISL8018EVAL3Z Evaluation Board User Guide

Description

The ISL8018EVAL3Z evaluation board is intended for use by individuals with requirements for Point-of-Load applications sourcing from 2.7V to 5.5V. The ISL8018EVAL3Z is used for a complete demonstration of the performance of the ISL8018 low quiescent high efficiency synchronous buck regulator.

The ISL8018EVAL3Z evaluation board is a 76.2mmx76.2mm 4-layer FR4 board with 2oz copper in all layers. The complete converter occupies 438.71mm^2 area.

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 10V power supply with at least 15A source current capability or 5V battery
- Electronic loads capable of sinking current up to 10A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope
- Signal generator

Key Features

- High efficiency synchronous buck regulator with up to 97% efficiency
- ±10% output voltage margining
- Adjustable current limit
- Start-up with prebiased output
- Internal soft-start - 1ms or adjustable
- Soft-stop output discharge during disabled
- Adjustable frequency from 500kHz to 4MHz - default at 1MHz
- External synchronization up to 4MHz - master to slave phase shifting capability

References

ISL8018 datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL8018EVAL3Z	Evaluation Board

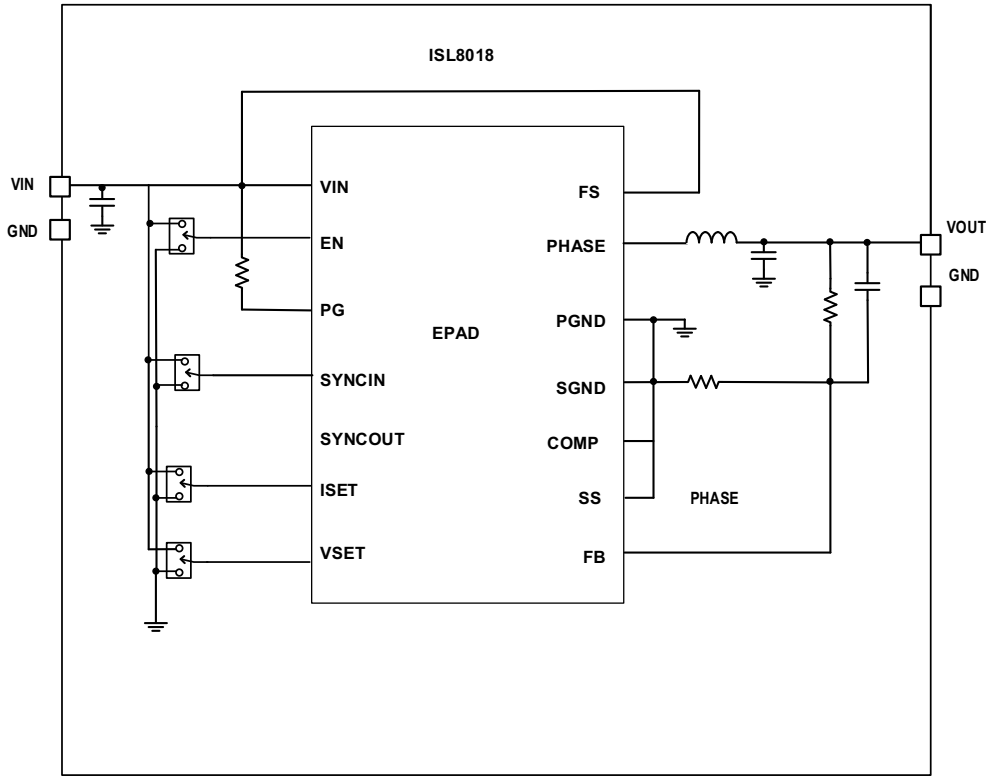

FIGURE 1. BLOCK DIAGRAM

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Copyright Intersil Americas LLC 2015. All Rights Reserved
Intersil (and design) is a trademark owned by Intersil Corporation or one of its subsidiaries.
All other trademarks mentioned are the property of their respective owners.

Quick Setup Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to VIN, the plus terminal to VIN (J1) and the negative return to PGND (J2).
3. Connect the output load to VOUT, the plus terminal to VOUT1 (J3) and the negative return to PGND (J4).
4. Verify that the position is PWM for S1.
5. Verify the position is OPEN for S2 and S3.
6. Verify that the position is ON for S4 and S5.
7. Turn on the power supply.
8. Verify the output voltage is 1.8V for VOUT1.

Switches Control

The ISL8018 evaluation board contains S1 through S5 for various controls of the ISL8018 circuitries. Table 1 details this function.

TABLE 1. SWITCH SETTINGS

S1	MODE	FUNCTION
1	PWM	Fixed PWM frequency at light load
3	PFM	Force continuous mode
S2	**ISET**	**PROGRAM OUTPUT CURRENT**
1	LOW	Set output load to 3A.
-	OPEN	Set output load to 8A.
3	HIGH	Set output load to 5A.
S3	**VSET**	**SET OUTPUT MARGIN**
1	LOW	Set output voltage -10%.
-	OPEN	No output voltage margin
3	HIGH	Set output voltage +10%.
S4	**ENABLE**	**FUNCTION**
1	OFF	Disable VOUT1
3	PFM	Enable VOUT1
S5	**ENABLE**	**FUNCTION**
1	OFF	Disable VOUT2
3	PFM	Enable VOUT2

Frequency Control

The ISL8018 has an FS pin that controls the frequency of operation. Programmable frequency allows for optimization between efficiency and external component size. Default switching frequency is 1MHz when FS is tied to VIN (R_6 = 0 and R_5 is open). By connecting R_5 to GND, the switching frequency could be changed from 500kHz (R_5 = 386k) to 4MHz (R_5 = 36k) according to Equation 1:

$$R_T[k\Omega] = \frac{200 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 1)}$$

When using R_5 to adjust the operational frequency, this also sets external compensation mode. Please refer to the ISL8018 datasheet for more details.

Soft-Start Control

Short CSS1 to SGND for internal soft-start (approximately 1ms). Populate CSS1 to adjust the soft-start time. This capacitor, along with an internal 1.8µA current source, sets the soft-start interval of the converter, t_{SS} as shown in Equation 2.

$$CSS1[\mu F] = 3.33 \cdot t_{SS}[s] \quad \text{(EQ. 2)}$$

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition. **For proper use, do no prebias output voltage more than regulation point.**

Synchronization Control

The ISL8018 can be synchronized from 500kHz to 4MHz by an external signal applied to the SYNCIN pin. The rising edge on the SYNCIN triggers the rising edge of the PHASE pulse. Make sure that the minimum on-time of the PHASE node is greater than 140ns.

SYNCOUT is a 250µA current pulse signal output triggered by the rising edge of the clock or the SYNCIN signal (whichever is greater in frequency) to drive the other ISL8018 and avoid the system's beat frequencies effects. To implement time shifting between the master circuit to the slave, it is recommended to add a capacitor, C_{13} as shown in Figure 4 of the schematic. The time delay from SYNCOUT_Master to SYNCIN_Slave is calculated in pF using Equation 3:

$$C_{13}(pF) = 0.333 \cdot (t - 20)(ns) \quad \text{(EQ. 3)}$$

Where, t is the desired time shift between the master and the slave circuits in ns. Care must be taken to include PCB parasitic capacitance of ~3pF to 10pF.

The maximum should be limited to 1/Fs-100ns to insure that SYNCOUT has enough time to discharge before the next cycle starts.

Evaluating the Other Output Voltage

The ISL8018EVAL3Z evaluation board output is preset to 1.8V for VOUT1, however, output voltages can be adjusted from 0.6V to 5V. The output voltage programming resistor, R_1, will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 0Ω and 200kΩ, as shown in Equation 4.

$$R_2 = R_1\left(\frac{VFB}{VO - VFB}\right) \quad \text{(EQ. 4)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated and R_1 is shorted. For faster response performance, add 10pF to 47pF in parallel to R_1, feedforward capacitor C_4. Check bode plot to insure optimum performance.

When internal compensation is used, we only need a few external components: input capacitance, the output capacitance, inductor, upper feedback resistor and lower feedback resistor. Feedforward capacitor is optional. The ceramic capacitor is recommended to be X5R or X7R.

In Table 2, the minimum output capacitor value is given for different output voltages with internal compensation. Notice that the voltage rating has large effect on the actual capacitance value for ceramic technology. The effective capacitance varies with different V_{OUT}, therefore, it is better to use a high voltage rating capacitor or a set of parallel lower voltage rating capacitors.

Additional output capacitance may be added to improve transient response and start-up performance.

With additional capacitance, please use external compensation for better loop response design. See the datasheet compensation section for more detail. Refer to Figures 11 through 16 for examples of $1.2V_{OUT}$ and $3.3V_{OUT}$ soft-start waveforms, load transient and relevant bode plot with external compensation configuration".

TABLE 2. COMPONENT VALUE SELECTION (REFER TO "ISL8018EVAL3Z Schematic" on page 4)

V_{OUT}	1.2V	1.5V	1.8V	2.5V	3.3V
C_1, C_2	22µF	22µF	22µF	22µF	22µF
C_7, C_8	66µF	66µF	47µF	47µF	47µF
C_4	33pF	33pF	10pF	10pF	10pF
L1	0.47µH	0.47~1µH	0.68~1.5µH	1~1.5µH	1~2.2µH
R1	100k	150k	200k	316k	450k
R2	100k	100k	100k	100k	100k

ISL8018EVAL3Z Evaluation Board

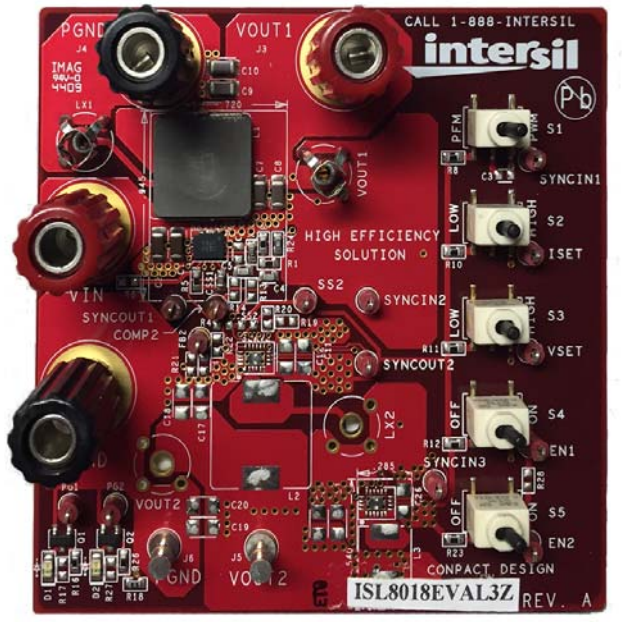

FIGURE 2. FRONT VIEW

FIGURE 3. BACK VIEW

ISL8018EVAL3Z Schematic

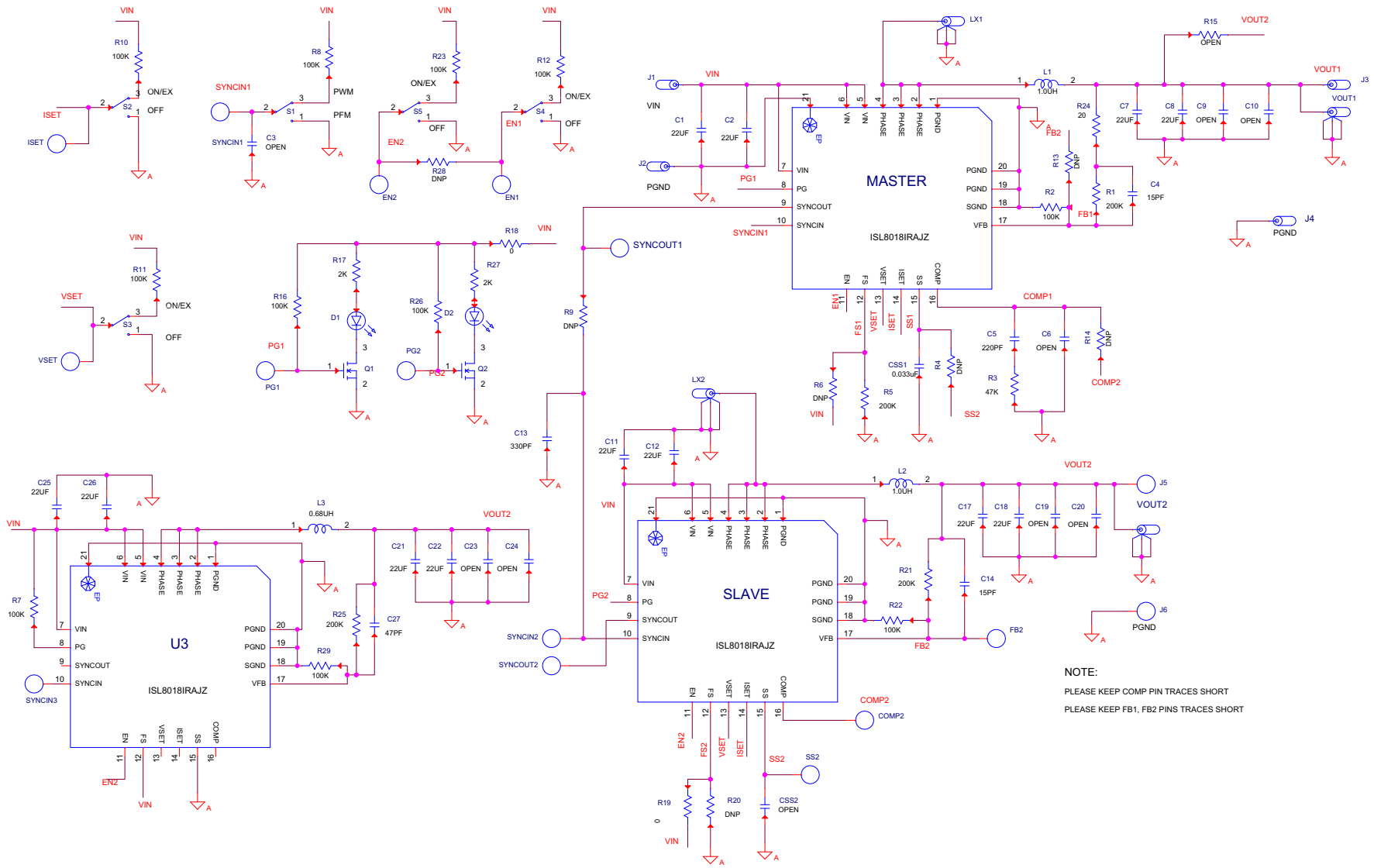

FIGURE 4. ISL8018EVAL3Z SCHEMATIC

TABLE 3. BILL OF MATERIALS

MANUFACTURER PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL8018EVAL3ZREVAPCB	1	ea.	SEE LABEL-RENAME BOARD	PWB-PCB, ISL8018EVAL3Z, REVA, ROHS	IMAGINEERING INC
GRM39C0G150J050AD	1	ea.	C4, C14	CAP, SMD, 0603, 15pF, 50V, 5%, NP0, ROHS	MURATA
C0603C0G500-221JNE	1	ea.	C5	CAP, SMD, 0603, 220pF, 50V, 5%, C0G, ROHS	VENKEL
06035C333JAT2A	1	ea.	CSS1	CAP, SMD, 0603, 0.033µF, 50V, 5%, X7R, ROHS	AVX
	0	ea.	C3, C6, CSS2	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	
C3216X5R0J226M160AA	5	ea.	C1, C2, C7, C8, C10	CAP, SMD, 1206, 22µF, 6.3V, 20%, X5R, 1.6mm Height, ROHS	TDK
GRM31CR60J476ME19L	1	ea.	C9	CAP, SMD, 1206, 47µF, 6.3V, 20%, X5R, ROHS	MURATA
	0	ea.	C19, C20, C23, C24	CAP, SMD, 1206, DNP-PLACE HOLDER, ROHS	
IHLP5050CEER1R0M01	1	ea.	L1	COIL-PWR INDUCTOR,SMD, 13mm, 1.0µH, 20%, 24A, ROHS	VISHAY
111-0702-001	2	ea.	J1, J3	CONN-GEN, BIND.POST, INSUL-RED, THMBNUT-GND	JOHNSON COMPONENTS
111-0703-001	2	ea.	J2, J4	CONN-GEN, BIND.POST, INSUL-BLK, THMBNUT-GND	JOHNSON COMPONENTS
131-4353-00	2	ea.	LX1, VOUT1	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX
1514-2	2	ea.	J5, J6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
5000	14	ea.	EN1, EN2, FB2, PG1, PG2, SS2, ISET, VSET, COMP2, SYNCIN1-SYNCIN3, SYNCOUT1, SYNCOUT2	CONN-MINI TEST PT, VERTICAL, RED, ROHS	KEYSTONE
LTST-C170CKT	2	ea.	D1, D2	LED-GaAs RED, SMD, 2x1.25mm, 100mW, 40mA, 10mcd, ROHS	LITEON/VISHAY
ISL8018IRAJZ	1	ea.	MASTER	IC-ADJ. 6A BUCK REGULATOR, 20P, QFN, 3x4, ROHS	INTERSIL
2N7002-7-F	2	ea.	Q1, Q2	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	DIODES, INC.
	0	ea.	R6, R9, R20, R28	RESISTOR,SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	
	0	ea.	R4, R7, R13, R14, R19, R21, R22, R25, R29	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	
ERJ-3EKF20R0V	1	ea	R24	RES, SMD, 0603, 20Ω, 1/10W, 1%, TF, ROHS	PANASONIC
CR0603-10W-000T	1	ea.	R18	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL

TABLE 3. BILL OF MATERIALS (Continued)

MANUFACTURER PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
CR0603-10W-1003FT	8	ea.	R2, R8, R10, R11, R12, R16, R23, R26	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	VENKEL
CR0603-10W-2003FT	2	ea.	R1, R5	RES, SMD, 0603, 200k, 1/10W, 1%, TF, ROHS	VENKEL
RC0603FR-0747KL	1	ea.	R3	RES, SMD, 0603, 47k, 1/10W, 1%, TF, ROHS	YAGEO
	0	ea.	R17, R27	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	
	0	ea.	R15	RES, SMD, 1210, DNP, DNP, DNP, TF, ROHS	
GT11MSCBE	3	ea.	S1, S4, S5	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT INDUSTRIES/C&K DIVISION
GT13MSCBE	2	ea.	S2, S3	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 3POS, ON-OFF-ON, ROHS	C&K COMPONENTS
SJ-5003SPBL	4	ea.	Bottom four corners.	BUMPONS, 0.44inW x 0.20inH, DOMETOP, BLACK	3M
212403-013	1	ea.	Place assembly in bag.	BAG, STATIC, 5x8, ZIPLOC, ROHS	INTERSIL
	0	ea.	C11, C12, C13, C14, C17, C18, C21, C22, C25, C26, C27	DO NOT POPULATE OR PURCHASE	
	0	ea.	L2, L3	DO NOT POPULATE OR PURCHASE	
	0	ea.	LX2, VOUT2	DO NOT POPULATE OR PURCHASE	
	0	ea.	U3, SLAVE	DO NOT POPULATE OR PURCHASE	

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL8018, the power loop is composed of the output inductor L's, the output capacitor C_{OUT}, the PHASE's pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin and the ground of the input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

ISL8018EVAL3Z Board Layout

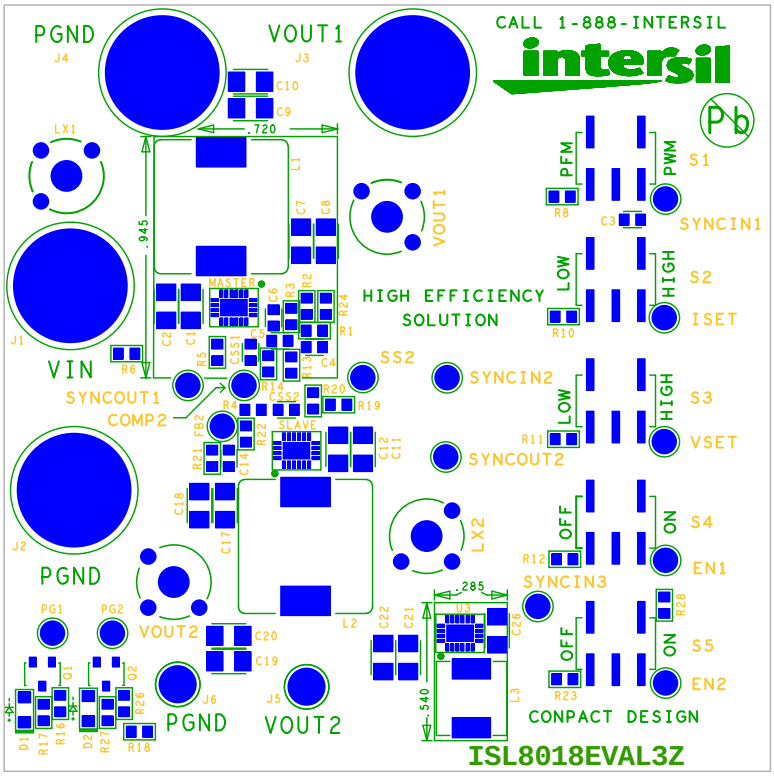

FIGURE 5. TOP LAYER COMPONENTS

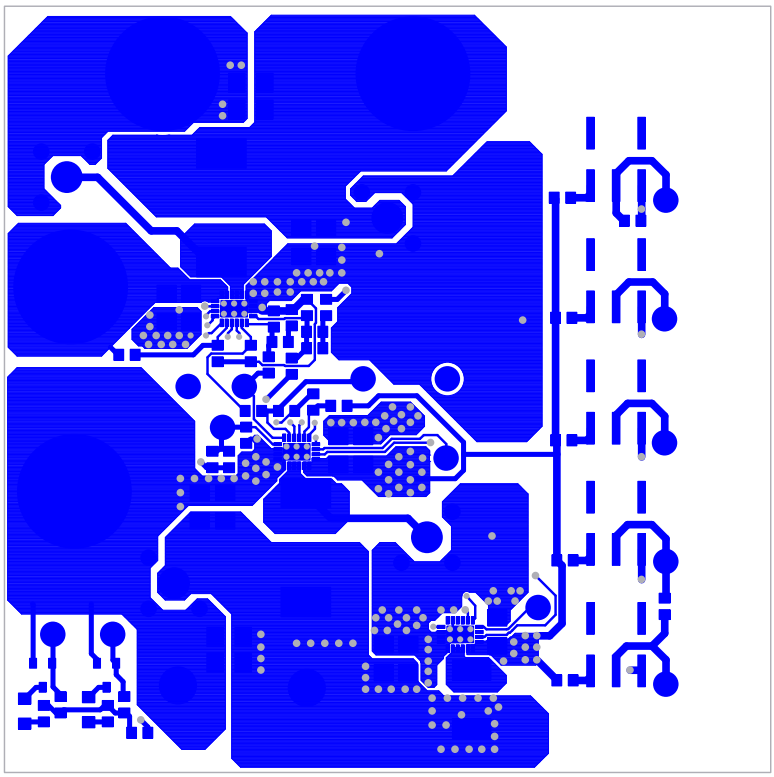

FIGURE 6. TOP LAYER ETCH

ISL8018EVAL3Z Board Layout (Continued)

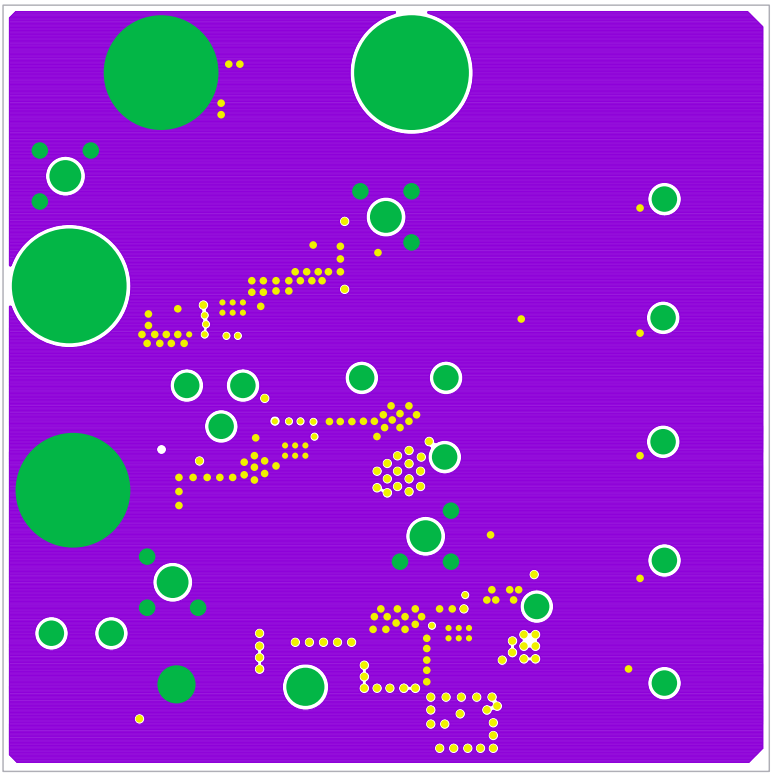

FIGURE 7. SECOND LAYER ETCH

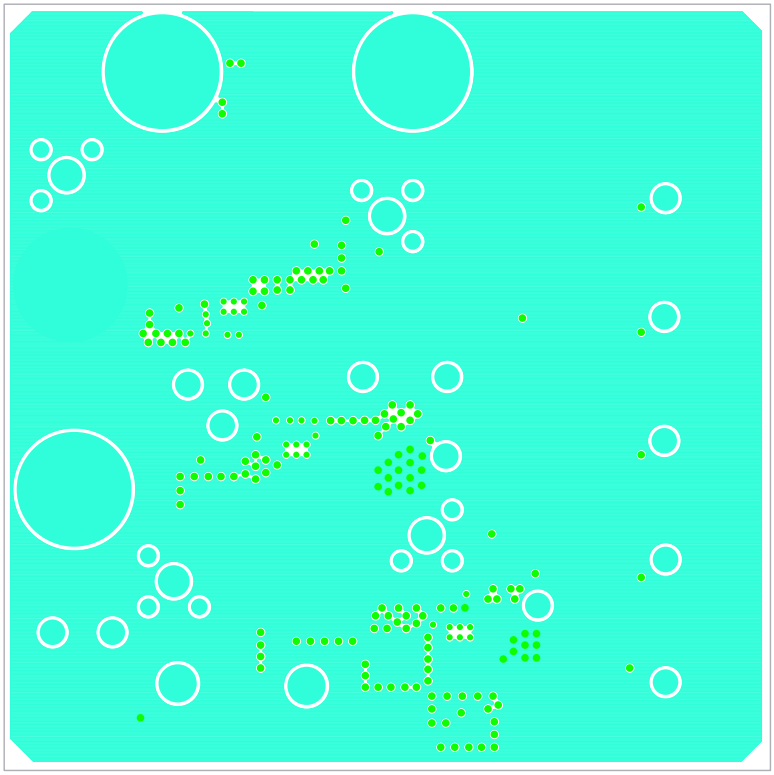

FIGURE 8. THIRD LAYER ETCH

ISL8018EVAL3Z Board Layout (Continued)

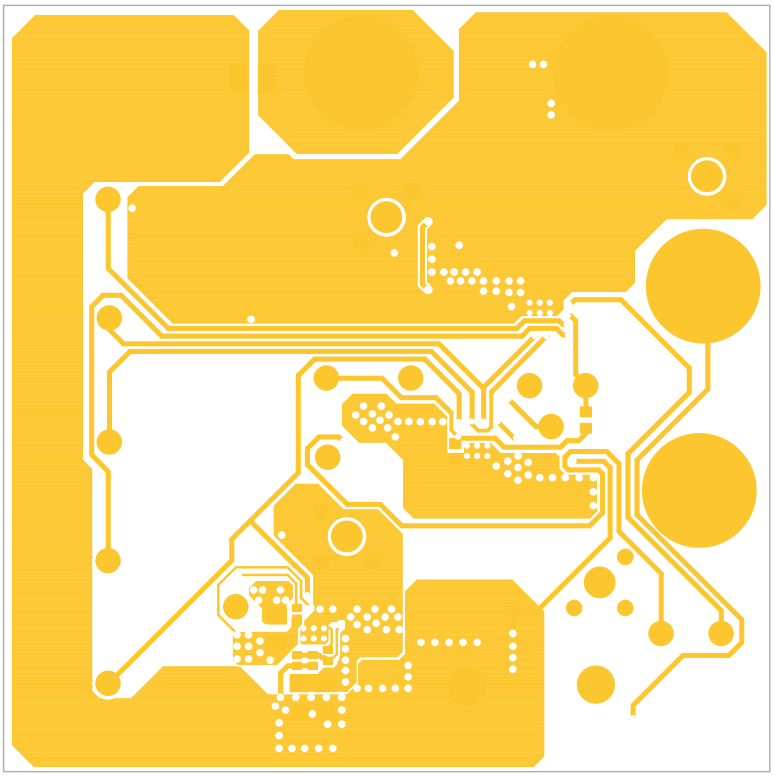

FIGURE 9. BOTTOM LAYER ETCH

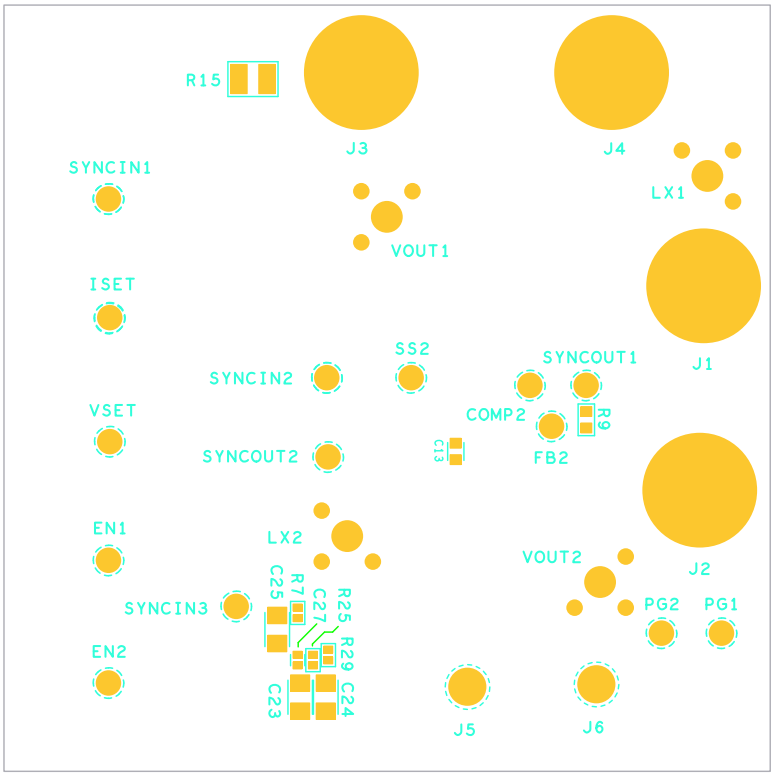

FIGURE 10. BOTTOM LAYER COMPONENTS

Typical Performance Curves

Unless noted: V_{IN} = 5.5V, f_{SW} = 1MHz, internal (soft-start).

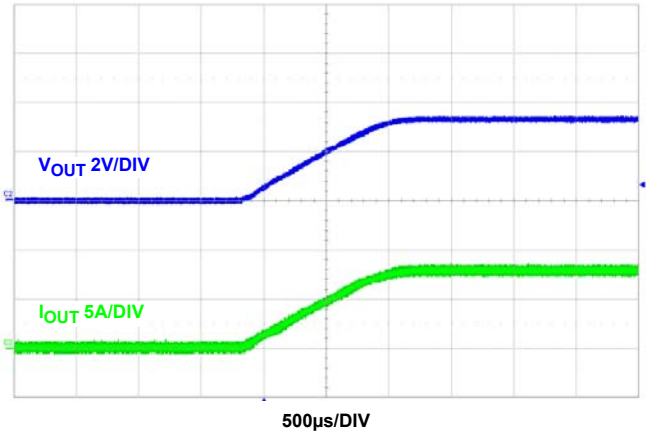

FIGURE 11. 3.3V_{OUT}, R_3 = 25k, C_5 = 470pF, C_{OUT} = 100µF (EFFECTIVE CAPACITANCE), C_4 = 47pF, L = 2.2µH

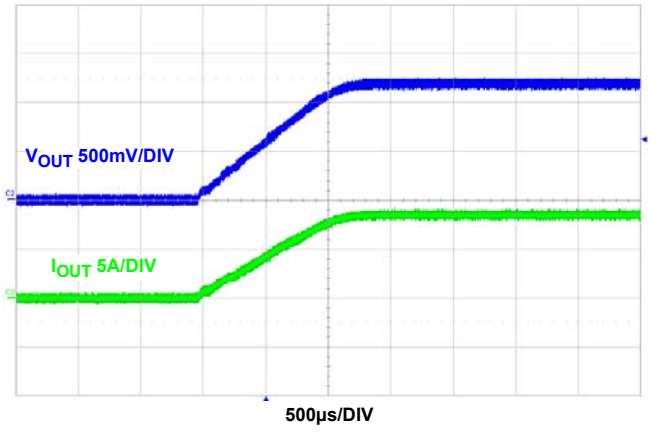

FIGURE 12. 1.2V_{OUT}, R_3 = 70k, C_5 = 220pF, C_{OUT} = 144µF (EFFECTIVE CAPACITANCE), C_4 = 33pF, L = 1µH

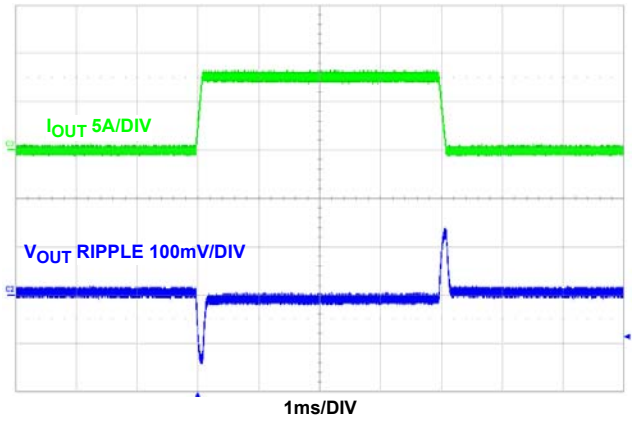

FIGURE 13. LOAD TRANSIENT 5.5V_{IN}/3.3V_{OUT}, R_3 = 25k, C_5 = 470pF, C_{OUT} = 100µF (EFFECTIVE CAPACITANCE), C_4 = 47pF, L = 2.2µH, SLEW RATE: 0.1A/µs

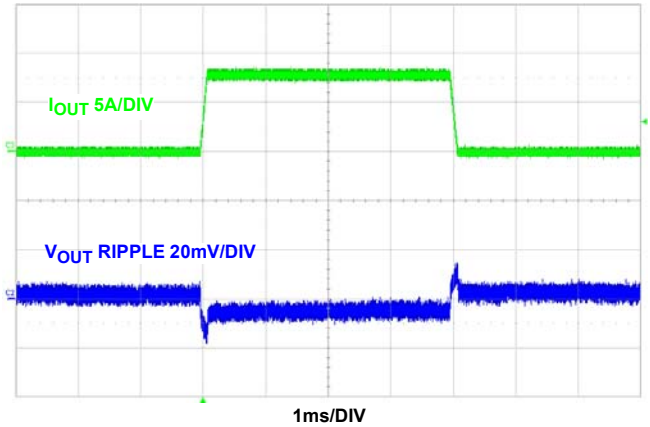

FIGURE 14. LOAD TRANSIENT 5.5V_{IN}/1.2V_{OUT}, R_3 = 70k, C_5 = 220pF, C_{OUT} = 144µF (EFFECTIVE CAPACITANCE), C_4 = 33pF, L = 1µH, SLEW RATE: 0.1A/µs

Typical Performance Curves Unless noted: V_{IN} = 5.5V, f_{SW} = 1MHz, internal (soft-start). **(Continued)**

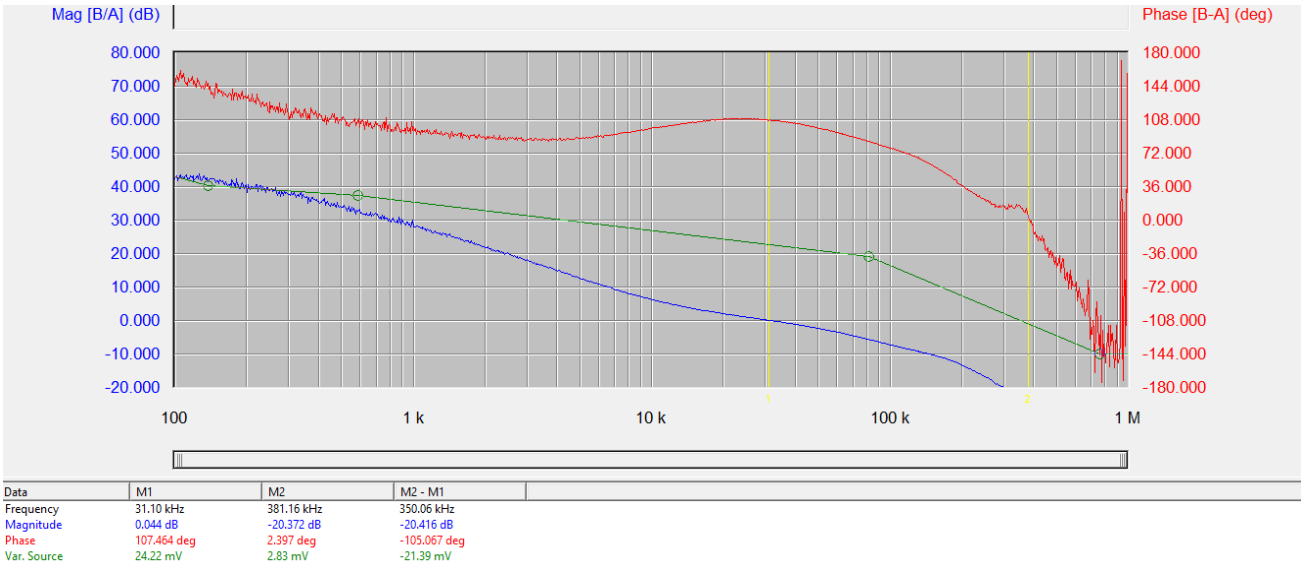

FIGURE 15. BODE PLOT 5.5V_{IN}/3.3V_{OUT} WITH FULL LOAD, R_3 = 25k, C_5 = 470pF, C_{OUT} = 100µF (EFFECTIVE CAPACITANCE), C_4 = 47pF, L = 2.2µH

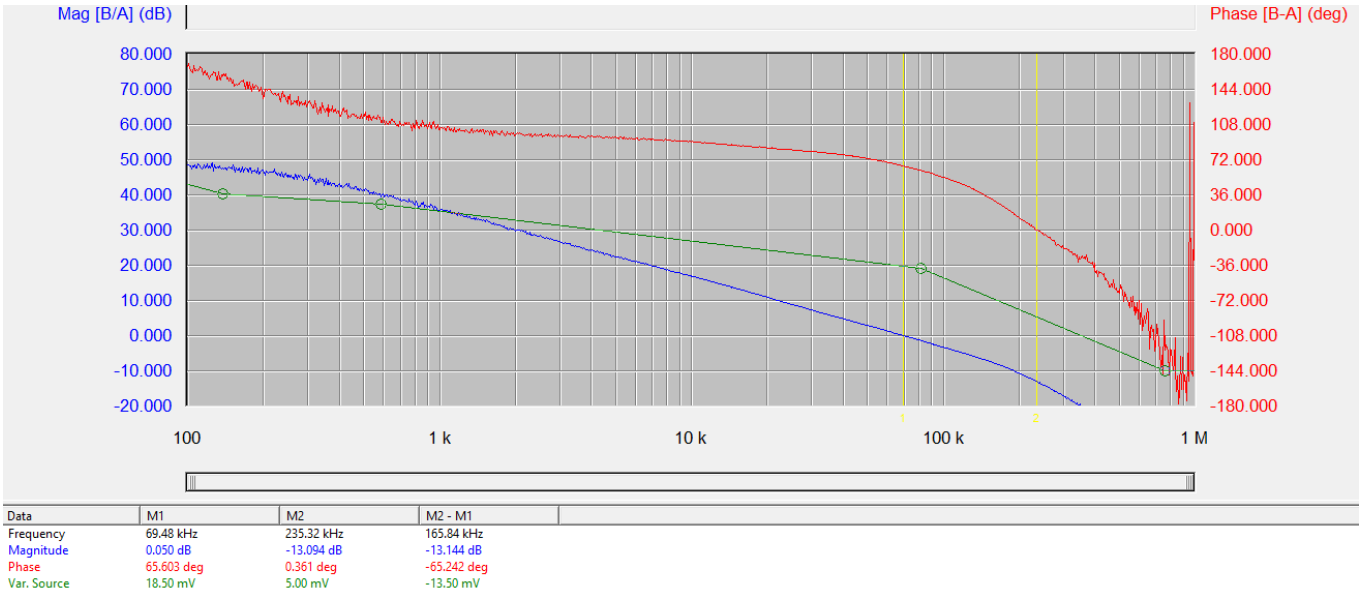

FIGURE 16. BODE PLOT 5.5V_{IN}/1.2V_{OUT} WITH FULL LOAD, R_3 = 70k, C_5 = 220pF, C_{OUT} = 144µF (EFFECTIVE CAPACITANCE), C_4 = 33pF, L = 1µH

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the document is current before proceeding.

For information regarding Intersil Corporation and its products, see www.intersil.com