Low Voltage, Level Shifting Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery

FEATURES

- **Optimized for Low Voltage Systems Down to 0.9V**
- **Bidirectional Buffer with Stuck Bus Recovery**
- **–200mV Offset In-Out/+300mV Offset Out-In**
- **30ms Stuck Bus Timeout**
- **Compatible with Non-Compliant V_{OL} I^2C Devices**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- **±6kV Human Body Model (HBM) ESD Protection**
- Isolates Input SDA and SCL Lines from Output
- Compatible with I^2C™, I^2C Fast Mode and SMBus
- READY Open-Drain Output
- 1V Precharge on SDAOUT and SCLOUT Lines
- Small 8-Lead (3mm × 3mm × 0.75mm) DFN and 8-Lead MSOP Packages

APPLICATIONS

- Live Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- RAID Systems
- ATCA

DESCRIPTION

The LTC®4308 hot swappable, 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. The LTC4308 provides bidirectional buffering, keeping the backplane and card capacitances isolated. Negative offset from output to input allows communication between output bus devices with high V_{OL} and devices on the low voltage input side, where bus supplies can be as low as 0.9V. If SDAOUT or SCLOUT are low for 30ms, the LTC4308 will automatically break the Input-Output connection. At this time the LTC4308 automatically generates up to 16 clock pulses on SCLOUT in an attempt to free the bus. A connection will resume if the stuck bus is cleared.

During insertion, the SDAOUT and SCLOUT lines are precharged to 1V to minimize bus disturbances. When driven high, the ENABLE input allows the LTC4308 to connect after a stop bit or bus idle condition. Driving ENABLE low breaks the connection between SDAIN and SDAOUT, SCLIN and SCLOUT. READY is an open-drain output which indicates that the backplane and card sides are connected.

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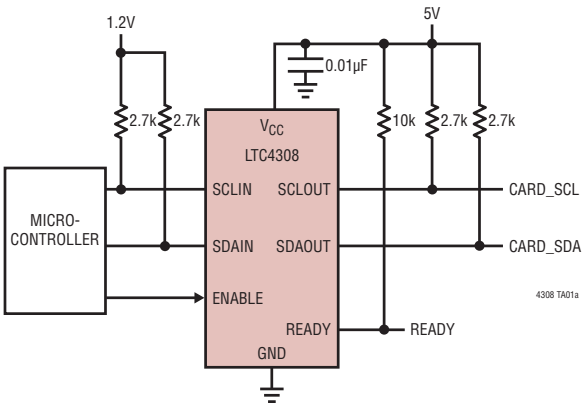
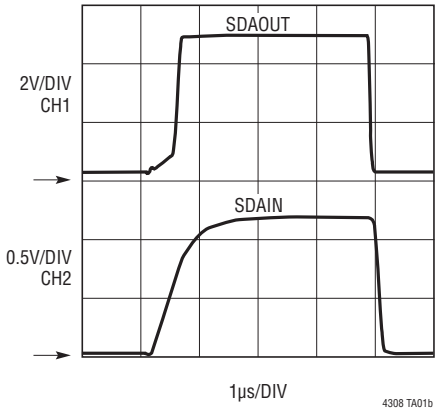
TYPICAL APPLICATION

The LTC4308 in a 1.2V Microcontroller Application



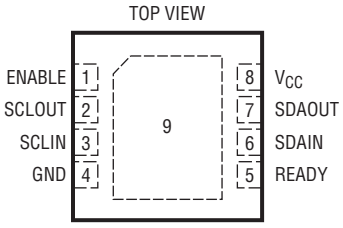
1.2V to 5V Level Shifting



ABSOLUTE MAXIMUM RATINGS (Notes 1, 7)

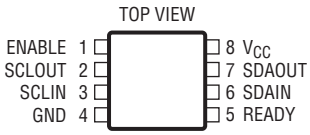
V_{CC} to GND ..... –0.3V to 6V
SDAIN, SCLIN, SDAOUT, SCLOUT,
READY, ENABLE..... –0.3V to 6V
Maximum Sink Current (SDAIN, SCLIN, SDAOUT,
SCLOUT, READY) 50mA
Operating Temperature Range
LTC4308C ..... 0°C to 70°C
LTC4308I.....–40°C to 85°C
Storage Temperature Range
DFN.....–65°C to 125°C
MSOP .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) CONNECTION TO GROUND IS OPTIONAL



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4308CDD#PBF	LTC4308CDD#TRPBF	LBTT	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4308IDD#PBF	LTC4308IDD#TRPBF	LBTT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4308CMS8#PBF	LTC4308CMS8#TRPBF	LTBTS	8-Lead Plastic MSOP	0°C to 70°C
LTC4308IMS8#PBF	LTC4308IMS8#TRPBF	LTBTS	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.3		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, V_{SCLOUT} = V_{SDAOUT} = 0V (Note 6)	●		7	11	mA
I_{SD}	Shutdown Supply Current	V_{CC} = 5.5V, ENABLE = 0V	●		900	1400	µA
V_{PRE}	Precharge Voltage	SDAOUT, SCLOUT Open	●	0.8	1	1.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{IDLE}	Bus Idle Time		●	55	95	175	µs
V_{THR_EN}	ENABLE Threshold Voltage	ENABLE Rising Edge	●	0.45	0.6	0.75	V
$V_{THR\_EN(HYST)}$	ENABLE Threshold Voltage Hysteresis	(Note 3)			35		mV
I_{ENABLE}	ENABLE Input Current	ENABLE from 0V to V_{CC}	●		0.1	±5	µA
t_{PLH_EN}	ENABLE Delay Off-On	(Figure 1)			95		µs
t_{PHL_EN}	ENABLE Delay On-Off	(Note 3), (Figure 1)			10		ns
t_{PLH_READY}	READY Delay Off-On	(Note 3), (Figure 1)			10		ns
t_{PHL_READY}	READY Delay On-Off	(Note 3), (Figure 1)			10		ns
V_{OL_READY}	READY Output Low Voltage	I_{READY} = 3mA, V_{CC} = 2.3V	●			0.4	V
I_{OFF_READY}	READY Off Leakage Current	V_{CC} = READY = 5.5V	●		0.1	±5	µA
Prop Delay and Rise-Time Accelerators							
t_{PHL}	SDA/SCL Propagation Delay High to Low	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, (Notes 2, 3), (Figure 1)			70		ns
t_{PLH}	SDA/SCL Propagation Delay Low to High	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, (Notes 2, 3), (Figure 1)			10		ns
t_{RISE}	SDA/SCL Transition Time Low to High	C_{LOAD} = 100pF, 10k to V_{CC} on SDA, SCL, (Notes 3, 4), (Figure 1)			30	300	ns
t_{FALL}	SDA/SCL Transition Time High to Low	C_{LOAD} = 100pF, 10k to V_{CC} on SDA, SCL, (Notes 3, 4), (Figure 1)			30	300	ns
$I_{PULLUPAC}$	Transient Boosted Pull-Up Current	Positive Transition > 0.8V/µs on SDAOUT, SCLOUT (Note 5)		5	8		mA
Input-Output Connection							
V_{OS}	Input to Output Offset Voltage (OUT – IN)	2.7k to V_{CC} on SDAOUT, SCLOUT, SDAIN = SCLIN = 0.2V	●	250	300	380	mV
		2.7k to V_{CC} on SDAOUT, SCLOUT, SDAIN = SCLIN = 0.4V, V_{CC} = 5.5V	●	250	350	450	mV
	Output to Input Offset Voltage (IN – OUT)	2.7k to V_{CC} on SDAIN, SCLIN, SDAOUT = SCLOUT = 0.4V	●	–150	–200	–300	mV
		2.7k to V_{CC} on SDAIN, SCLIN, SDAOUT = SCLOUT = 0.4V, V_{CC} = 5.5V	●	–150	–250	–350	mV
V_{THR}	SDAOUT, SCLOUT Logic Input Threshold Voltage	$V_{CC} \geq$ 2.9V V_{CC} < 2.9V		1.4 1.1	1.65 1.35	1.9 1.6	V V
	SDAIN, SCLIN Logic Input Threshold Voltage	SDAIN, SCLIN Rising Edge, V_{CC} = 2.3V, 5.5V		0.45	0.6	0.75	V
$V_{THR(HYST)}$	SDAOUT, SCLOUT Logic Input Threshold Voltage Hysteresis	(Note 3)			50		mV
	SDAIN, SCLIN Logic Input Threshold Voltage Hysteresis	(Note 3)			35		mV
C_{IN}	Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT	(Note 3)				10	pF
I_{LEAK}	Input Leakage Current	SDA, SCL Pins	●			±5	µA
V_{OL}	Output Low Voltage	SDAOUT, SCLOUT Pins, I_{SINK} = 4mA, SDAIN = SCLIN = 0V, V_{CC} = 2.7V	●	0		400	mV
		2.7k to V_{CC} on SDAOUT, SCLOUT, SDAIN = SCLIN = 0V	●	250	300	380	mV
V_{ILMAX}	Buffer Input Logic Low Voltage	SDAOUT, SCLOUT Pins	●			1.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bus Stuck Low Timeout							
$t_{TIMEOUT}$	Bus Stuck Low Timer	SDAOUT = SCLOUT = 0V	●	25	30	35	ms
Timing Characteristics							
$f_{I2C,MAX}$	I^2C Maximum Operating Frequency	(Note 3)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 3)				1.3	µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 3)				100	ns
$t_{SU,STA}$	Repeated Start Condition Set-Up Time	(Note 3)				0	ns
$t_{SU,STO}$	Stop Condition Set-Up Time	(Note 3)				0	ns
$t_{HD,DATI}$	Data Hold Time Input	(Note 3)				0	ns
$t_{SU,DAT}$	Data Set-Up Time	(Note 3)				100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See "Propagation Delays" in the Operations section for a discussion of t_{PHL} and t_{PLH} as a function of pull-up resistance and bus capacitance.

Note 3: Determined by design, not tested in production.

Note 4: Measure points are 0.3 • V_{CC} and 0.7 • V_{CC}.

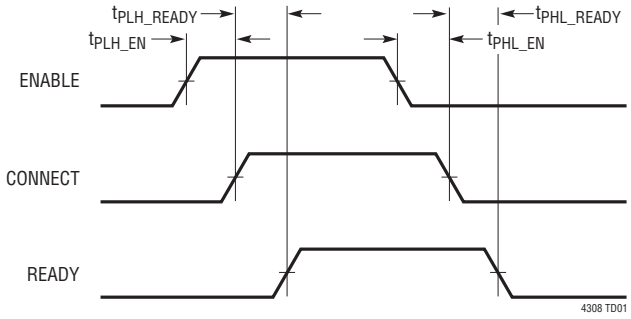
Note 5: $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage as shown in the Typical Performance Characteristics section.

Note 6: I_{CC} test performed with connection circuitry active.

Note 7: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

TIMING DIAGRAMS

ENABLE, CONNECT, READY Timing



Rising and Falling Propagation Delays and Rise and Fall Times for SDAIN, SDAOUT and SCLIN, SCLOUT

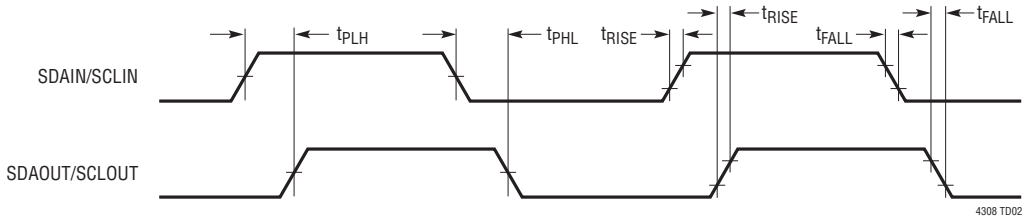
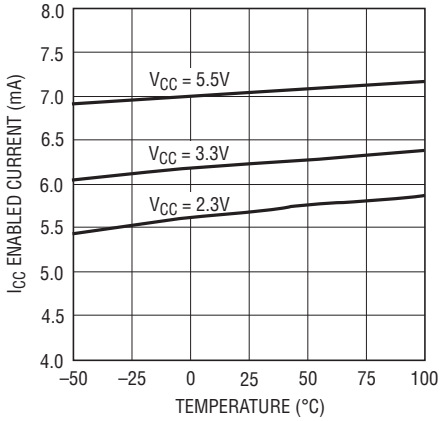


Figure 1. Timing Diagrams

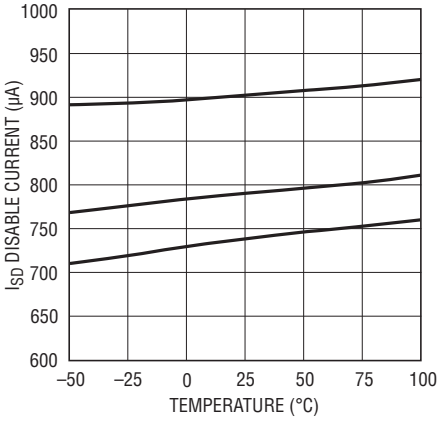
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, unless otherwise indicated.

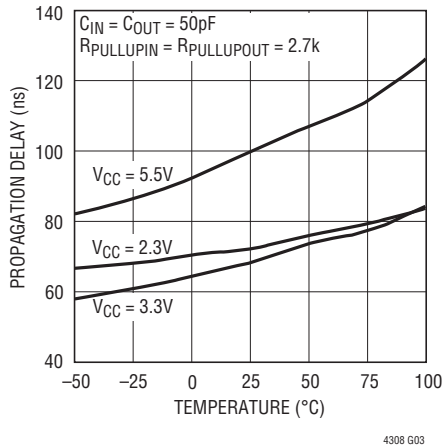
I_{CC} Enabled Current vs Temperature



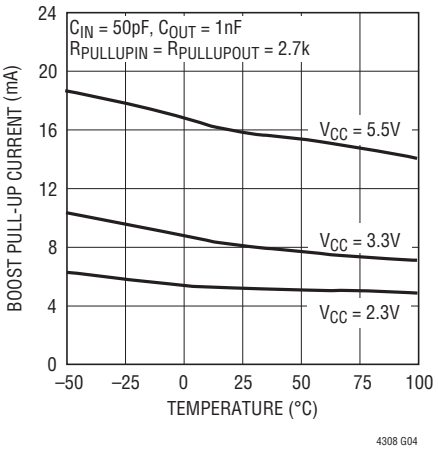
I_{SD} Disabled Current vs Temperature



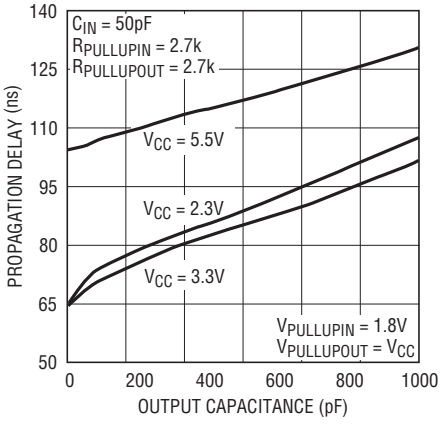
Input-Output High to Low Propagation Delay vs Temperature



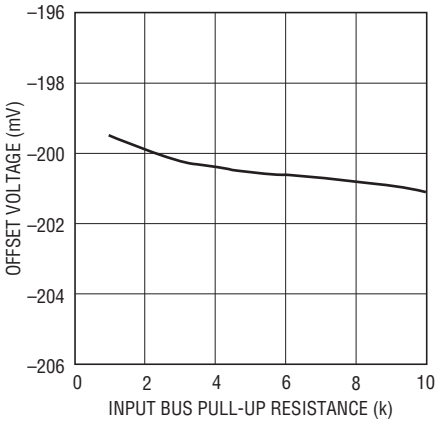
Boost Pull-Up Current vs Temperature



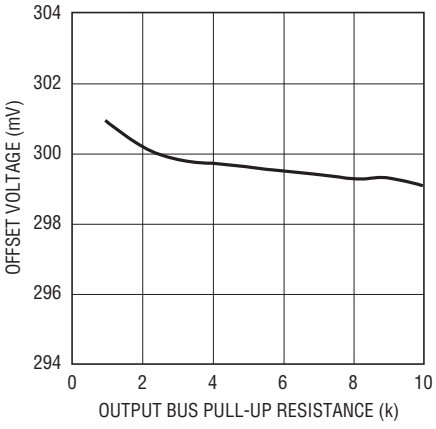
Input-Output High to Low Propagation Delay vs Output Capacitance



Input-Output Offset Voltage vs Pull-Up Resistance



Output-Input Offset Voltage vs Pull-Up Resistance



PIN FUNCTIONS

ENABLE (Pin 1): Connection Enable Input. This 0.6V nominal threshold input pin enables or disables the LTC4308. For normal operation, pull or connect ENABLE high. Driving ENABLE below the 0.45V threshold isolates SDAIN from SDAOUT, SCLIN from SCLOUT, asserts READY low, and prohibits automatic clock and stop bit generation during a fault condition. A rising edge on ENABLE after a fault has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT. Connect to V_{CC} if unused.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to a SCL bus segment where bus stuck low recovery is desired. A pull-up resistor should be connected between this pin and a bus pull-up supply greater than or equal to V_{CC}.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to a SCL bus segment where isolation from bus stuck low issues is desired. A pull-up resistor should be connected between this pin and a bus pull-up supply greater than 0.9V.

GND (Pin 4): Device Ground. Connect this pin to a ground plane for best results.

READY (Pin 5): Connection Ready Status Output. This open-drain N-channel MOSFET pin pulls low when ENABLE is low, when the startup and connection sequence described in the Operation section has not been completed, or when the LTC4308 disconnects the input and output pins due to a bus stuck low condition. READY goes high when ENABLE is high and connection is made between the input and output pins. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. This pin can be left open if unused.

SDAIN (Pin 6): Serial Data Input. Connect this pin to a SDA bus segment where isolation from bus stuck low issues is desired. A pull-up resistor should be connected between this pin and a bus pull-up supply greater than 0.9V.

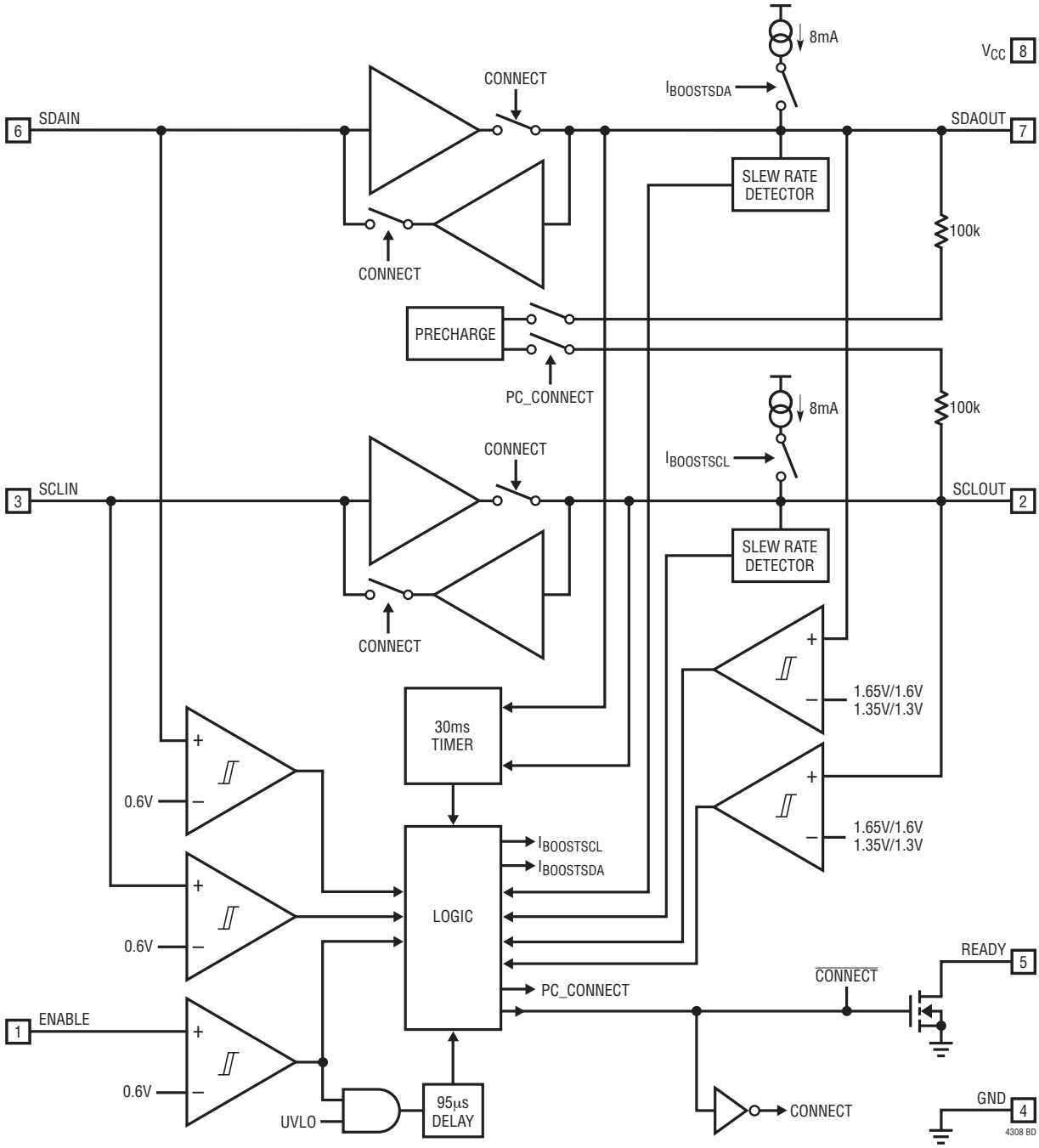
SDAOUT (Pin 7): Serial Data Output. Connect this pin to a SDA bus segment where bus stuck low recovery is desired. A pull-up resistor should be connected between this pin and a bus pull-up supply greater than or equal to V_{CC}.

V_{CC} (Pin 8): Supply Voltage Input. Place a bypass capacitor of at least 0.01µF close to V_{CC} for best results.

Exposed Pad (Pin 9, DFN Package Only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM

Low Voltage Level Shifting 2-Wire Bus Buffer with Stuck Bus Recovery



OPERATION

Start-Up

When the LTC4308 first receives power on its V_{CC} pin, either during power-up or live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2V (typical). This ensures the LTC4308 does not try to function until enough supply voltage is present.

During this time, the 1V precharge circuitry is actively forcing 1V through 100k nominal resistors to the SDAOUT and SCLOUT pins. Because SDAOUT and SCLOUT pins may be plugged into a live backplane, where the voltage on the backplane SDA and SCL busses can be anywhere between 0V and V_{CC}, precharging SCLOUT and SDAOUT to 1V minimizes the worst-case voltage differential these pins will see at the moment of contact, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4308 exits from UVLO, it monitors both the input and output pins for either a stop bit or a bus idle condition to indicate the completion of data transactions. When both sides are idle or one side has a stop bit while the other is idle, the connection circuitry is activated, joining the SDA and SCL pins on the input bus with those on the output bus. Because SDAIN and SCLIN are monitored for a stop bit or bus idle as a condition for connection, they may also be used for Hot-Swapping, but note that these pins are not precharged.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the input and output bus of the respective SDA or SCL pins is identical. A low forced on either output or input pin at any time results in both pin voltages forced low. The LTC4308 SCLOUT and SDAOUT busses are tolerant of I^2C bus DC logic low voltages up to the V_{IL} specification of $0.3 \cdot V_{CC}$, while the SCLIN and SDAIN busses are tolerant of bus logic low voltages up to 0.6V. A high occurs when all devices on the input and output pins release high.

When the LTC4308 senses a rising edge on either of the output busses, with a slew rate greater than 0.8V/µs, the internal pull-down device for the respective bus is deactivated at bus voltages as low as 0.48V. This methodology maximizes the effectiveness of the rise time accelerator circuitry and maintains compatibility with other devices in the LTC4300 bus buffer family. Care must be taken to ensure devices participating in clock stretching or arbitration is capable of forcing logic low voltages below 0.48V at the LTC4308's SCLOUT and SDAOUT pins.

These important features ensure the I^2C specification protocols such as clock stretching, clock synchronization, arbitration, and acknowledge function seamlessly in all cases as specified, regardless of how the devices in the system are connected to the LTC4308.

Another key feature provided by the connection circuitry is input and output bus capacitance isolation through bidirectional buffering. Because of this isolation, the waveforms on the input busses look slightly different than the corresponding output bus waveforms, as described in the next two sections.

Offset Voltages

When a logic low is driven on SDAIN or SCLIN, the LTC4308 regulates SDAOUT or SCLOUT, respectively, to a higher voltage, typically 300mV above the driven low voltage. When a logic low is driven on SCLOUT or SDAOUT, the LTC4308 regulates SCLIN or SDAIN, respectively, to a voltage that is typically 200mV below the driven low voltage. These offsets are nearly independent of pull-up current (see Typical Performance Characteristics).

OPERATION

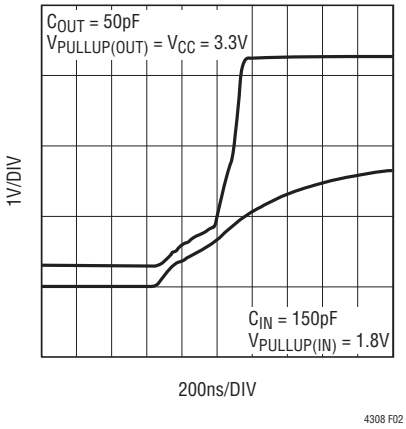


Figure 2. Input-Output Rising Edge Waveforms

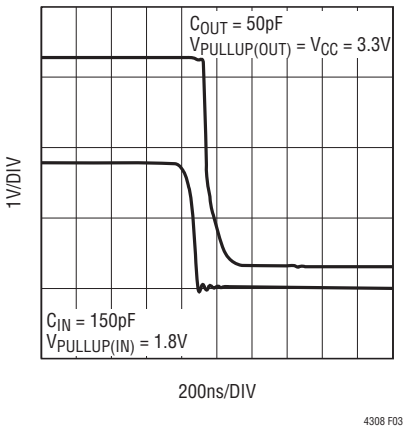


Figure 3. Input-Output Falling Edge Waveforms

Propagation Delays

During a rising edge, the rise time on each side is influenced by rise time acceleration, bus pull-up resistor, and the equivalent capacitance on the line. If the pull-up resistors are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance and the presence of rise time acceleration between the two sides. This effect is displayed in Figure 2 for V_{CC} = 3.3V and a 2.7k pull-up resistor on the input ($V_{PULLUP(IN)}$ = 1.8V, C_{IN} = 150pF) and output ($V_{PULLUP(OUT)}$ = 3.3V, C_{OUT} = 50pF). Since the output pin has rise time acceleration and less capacitance than the input, it rises faster and the effective propagation delay is negative.

There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 3 shows the falling edge waveforms for the same pull-up resistors and equivalent capacitance conditions as used in Figure 2. An external N-channel MOSFET device pulls down the voltage on the side with 150pF capacitance; the LTC4308 pulls down the voltage on the opposite side with a delay of 70ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus.

The Typical Performance Characteristics section shows propagation delay as a function of temperature and voltage for 2.7k pull-up resistors and 50pF equivalent capacitance on both sides of the part. Also, the Propagation Delay as a function of Output Capacitance curve shows that larger output capacitances translate to longer delays. Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

Bus Stuck Low Timeout

SDAOUT and SCLOUT are each connected to an internal timer. When SDAOUT or SCLOUT is low, its respective timer is started. Each timer is only reset when its pin goes high. If the bus stuck low does not go high within 30ms (typical), the connection circuitry is disabled, breaking the connection between the respective input and output pins. In addition, after at least 40µs, up to 16 clock pulses at 8.5kHz (typical) are generated on the SCLOUT pin by the LTC4308 in an attempt to free the stuck low bus. The clock pulses are halted if the bus recovers to a logic high condition before the completion of the full 16 pulses. A stop bit is always generated on the SCLOUT and SDAOUT pins to reset all devices on the bus.

If the stuck low SDAOUT or SCLOUT does not recover to a logic high condition after the automatic clocking and stop bit generation, the LTC4308 remains disconnected. Should the bus free, the LTC4308 will reconnect the input and output busses if a stop bit or bus idle condition is detected, as specified in the Start Up section. Alternatively, a rising edge on ENABLE forces the connection circuitry to reconnect the input and output busses and reset the 30ms timer if the bus remains in a stuck bus low condition.

OPERATION

When powering up into a bus stuck low condition, the connection circuitry connecting the SDA and SCL pins are not activated. 30ms after UVLO, automatic clocking and stop bit generation takes place as described above.

READY Digital Output

This pin provides a digital flag which is low when either ENABLE is low, the start-up sequence described earlier in this section has not been completed, or the LTC4308 has disconnected the input and output busses due to a bus stuck low condition. READY goes high when ENABLE is high and start-up is complete. The pin is driven by an open-drain pull-down device capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor to the bus pull-up supply to provide the pull-up.

ENABLE

When the ENABLE pin is driven below 0.45V with respect to the LTC4308's ground, the input pin is disconnected from the output pin and the READY pin is pulled low. When the pin is driven above 0.75V, the part waits for data transactions on both the input and output pins to be complete (as described in the Start-Up section) before connecting the two pins. At this time the internal pull-down on READY releases.

A rising edge on ENABLE after a bus stuck low condition has occurred forces a connection between SDAIN, SDAOUT, and SCLIN, SCLOUT even if the bus stuck low condition has not been cleared. At this time the 30ms timer is reset, but not disabled.

Rise Time Accelerators

Once connection has been established, rise time accelerator circuits on SDAOUT and SCLOUT are enabled. During positive bus transitions of at least 0.8V/µs, the rise time accelerators provide strong, slew-limited pull-up currents to force the bus voltage to rise at a rate of 100V/µs.

The rise time accelerators significantly improve reliability and performance in I^2C systems in several ways. First, due to the accelerator's significantly lower pull-up impedance, as compared to the bus pull-up resistance, the system is less susceptible to noise on rising edges, providing smooth, controlled transitions for both small and large systems. Second, the accelerators allow users to choose larger bus pull-up resistors, reducing power consumption and improving logic low noise margins or to design with bus capacitances beyond those specified in the I^2C specifications.

For these reasons, it is strongly recommended that users choose bus pull-up resistors that guarantee the output busses will rise on their own at a rate of at least 0.8 V/µs to ensure activation of the accelerators. See the Applications Information section for selecting pull-up resistor sizes.

It is important to connect SDAOUT and SCLOUT pins to a bus whose pull-up supply is equal to or greater than the LTC4308's supply to ensure the accelerators do not source current through the pull up resistors into the pull-up supply.

The rise time accelerators are internally disabled until the sequence of events described in the start-up section has been completed, as well as during automatic clocking and stop bit generation for a bus stuck low recovery event.

APPLICATIONS INFORMATION

Resistor Pull-Up Value Selection

To guarantee the SDAOUT and SCLOUT rise time accelerators are activated during a rising edge, the bus must rise on its own with a positive slew rate of at least 0.8V/µs. To achieve this, choose a maximum resistor value R_{PULLUP} using the formula:

$$R_{PULLUP} \leq \frac{(V_{BUS(MIN)} - 0.8V) \bullet 1250ns / V}{C_{BUS}}$$

Where R_{PULLUP} is the pull-up resistor value in kΩ, $V_{BUS(MIN)}$ is the minimum bus pull-up supply voltage and C_{BUS} is the equivalent bus capacitance in pF.

To estimate the value of C_{BUS}, use a general rule of 20pF of capacitance per device on the bus (10pF for the device and 10pF for interconnect).

In addition, R_{PULLUP} must be strong enough to overcome the precharge voltage and provide logic highs on SDAOUT and SCLOUT for the start-up and connection circuitry to connect the backplane to the card. To meet this requirement, always choose

$$R_{PULLUP} \leq 75k \frac{V_{BUS(MIN)} - V_{THR(MAX)}}{V_{THR(MAX)} - 1V}$$

where $V_{THR(MAX)}$ is the maximum specified Logic Input Threshold Voltage, V_{THR}.

Further, on SDAIN and SCLIN and for heavily loaded systems on SDAOUT and SCLOUT, where the selected R_{PULLUP} value causes the bus to rise at a rate slower than 0.8V/µs, users must also guarantee

$$R_{PULLUP} \leq \frac{V_{BUS(MIN)} - V_{THR(MAX)}}{100\mu A}$$

Live Insertion and Capacitance Buffering Application

Figure 4 and 5 illustrate applications of the LTC4308 that take advantage of the LTC4308's Hot Swap™, capacitance buffering and output pin precharge features. If the I/O cards were plugged directly into the backplane without the LTC4308 buffer, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing an LTC4308 on the edge of each card isolates the card capacitance from the backplane. For a given I/O card, the LTC4308 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4308, which is less than 10pF.

Figure 4 shows the LTC4308 used in the typical staggered connector application, where V_{CC} and GND are the longest "early power" pins. The "early power" pins ensure the LTC4308 is initially powered and forcing the 1V precharge voltage on the medium length SDA and SCL output pins before they contact with the backplane busses. Coupled with ENABLE as the shortest pin, passively pulled to ground by a resistor, the staggered approach provides additional time for transients associated with live insertion to settle before the LTC4308 can be enabled.

Figure 5 shows the LTC4308 in an application where all of the pins have the same length. In this application, a resistor is used to hold the ENABLE pin low during live insertion, until the backplane control circuitry can enable the device.

Level Shifting Applications

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4308 for bidirectional level shifting, as shown in Figures 4, 5, and 7. The LTC4308 can level shift between bus pull-up supplies as low as 0.9V to as high as 5.5V. Level shifting allows newer designs that require lower voltage supplies, such as EEPROMs and microcontrollers, the capability to interface with legacy backplanes which may be operating at higher supply voltages.

The LTC4308's negative offset voltage from output to input allow level shifting applications with high SDAOUT and SCLOUT V_{OL} to effectively translate to the low voltage SDAIN and SCLIN busses. Figure 7 shows an application where 200Ω resistors, used to provide additional ESD protection for the Temperature Sensor's internal low impedance pull-down device, generate high V_{OL} on the SDAOUT and SCLOUT busses.

APPLICATIONS INFORMATION

Systems with Supply Voltage Droop

In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is modeled by a series resistor in the V_{CC} line, as shown in Figure 6. For proper operation, make sure that the $V_{CC(LTC4308)}$ is ≥ 2.3V.

LTC4308 and LTC4301L Feature Comparison

Although both, the LTC4308 and LTC4301L are functionally similar Hot Swappable Bus Buffers designed for Low Voltage Level Translation in 2-wire bus systems, the LTC4308 provides greater features. These features include automatic bus stuck low detection and recovery; rise time accelerators on the output busses, and –200mV In-Out and 300mV Out-In offset voltages that are nearly independent of pull-up resistors. These and other differences are listed in Table 1 and must be accounted for if using the LTC4308 in LTC4301L applications.

Table 1: Differences Between LTC4301I and LTC4308

SPECIFICATION	LTC4301L	LTC4308	COMMENTS
$V_{CC(MIN)}$	2.7V	2.3V	Lower supply voltage allows greater compatibility with low voltage systems.
$V_{OS(TYP)}$	100mV	–200mV/300mV	Negative output-to-input offset voltage provide better noise margin on low voltage bus.
$I_{PULLUPAC(TYP)}$	N/A	8mA	Output bus rise time accelerators aid heavily loaded busses to meet rise time specifications.
$t_{TIMEOUT}$	N/A	30ms	Stuck Bus Recovery automatically isolates the input bus from the output bus and attempts to recover the output bus.
READY	–	–	READY functions identically. In addition, the LTC4308 will pull READY low to indicate when disconnection has occurred.
$\overline{CS}$/ENABLE	Active Low	Active High	When replacing an LTC4301L with an LTC4308, invert the $\overline{CS}$ signal.

APPLICATIONS INFORMATION

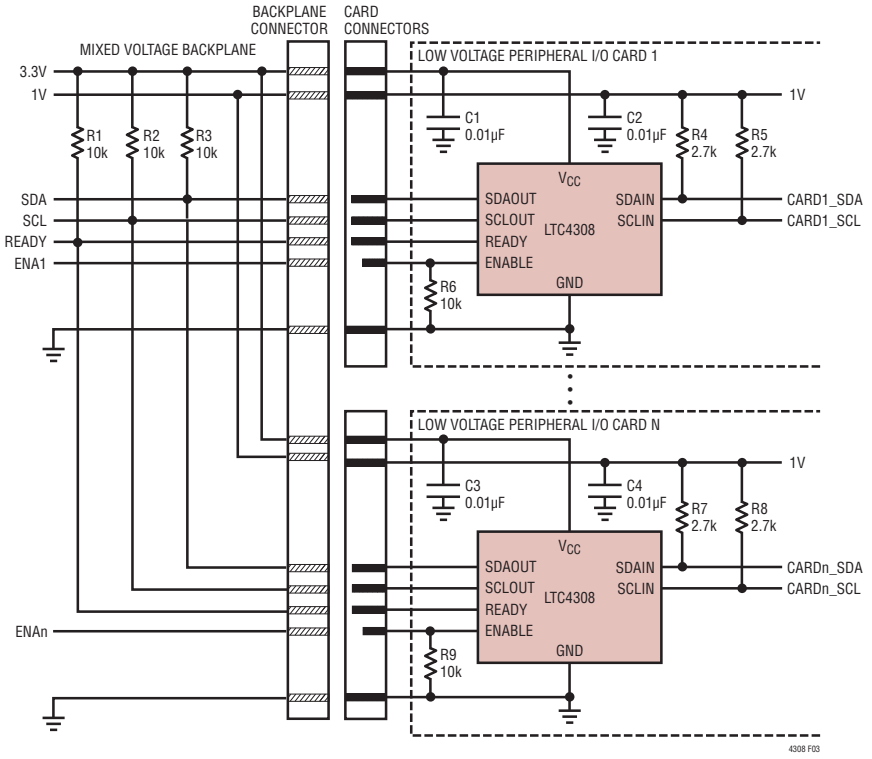


Figure 4. The LTC4308 in an Application with Staggered Connectors.

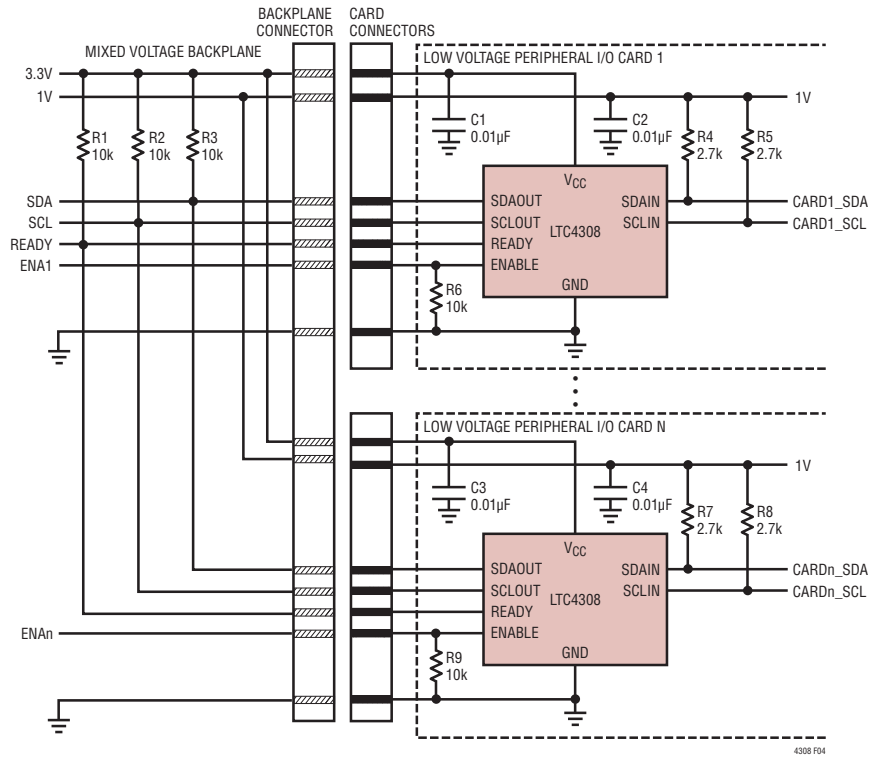


Figure 5. The LTC4308 in an Application Where All the Pins Have the Same Length.

TYPICAL APPLICATIONS

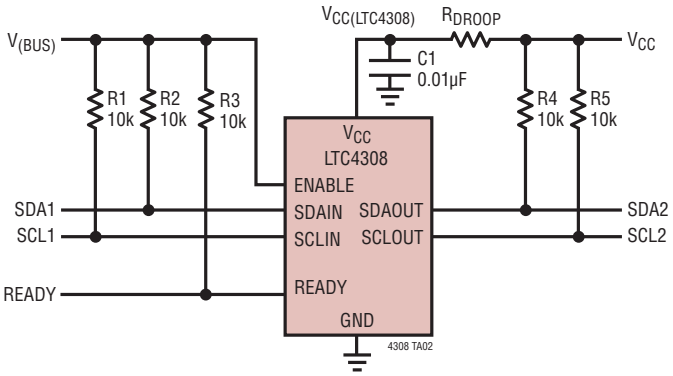


Figure 6. System with Voltage Droop

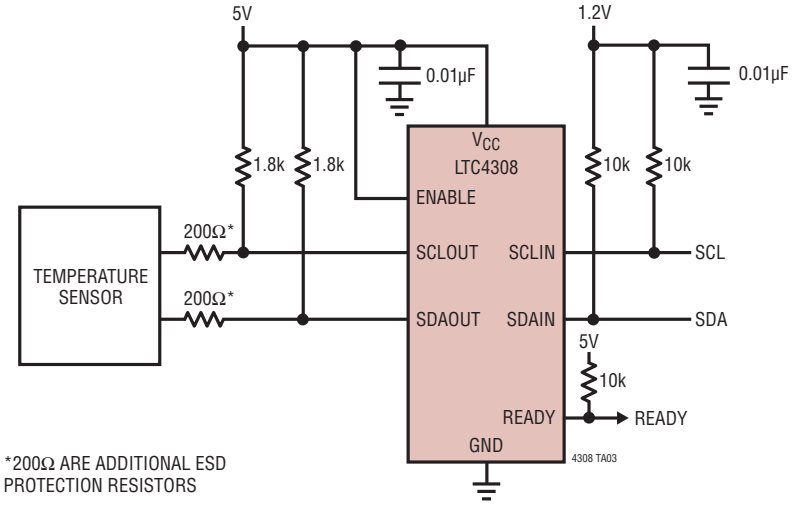
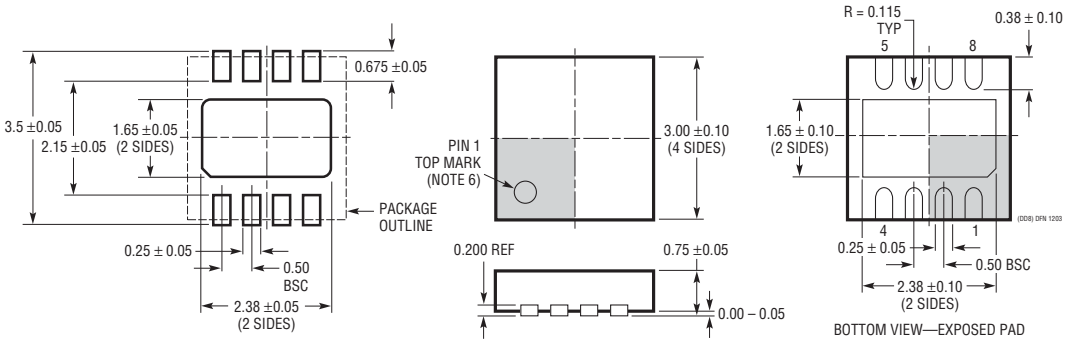


Figure 7. High V_{OL} Application

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

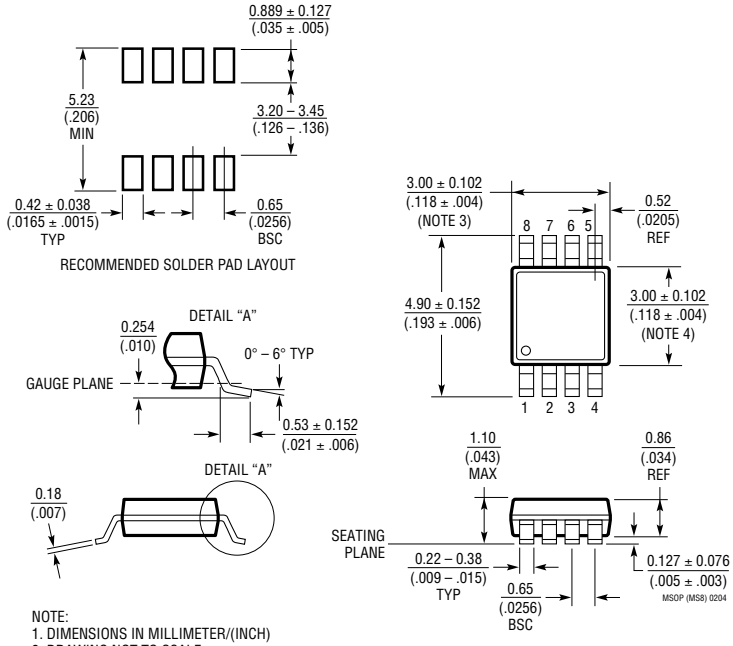


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)

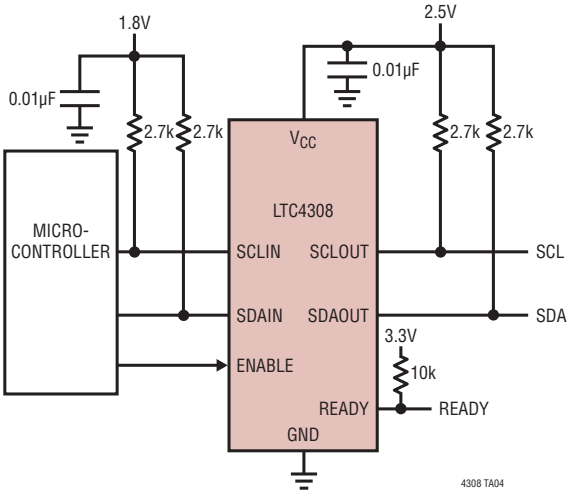


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

The LTC4308 in a Level Shifting Application.



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog MUX with SMBus Interface	Low R_{ON}: 35Ω Single Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA ±2.5% Tolerance Over Temperature, Four Selectable SMBus Addresses, DAC Powers Up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	Eight Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I^{2}C Rise Time, Ensures Data Integrity with Multiple SMBus/I^{2}C Devices
LTC1695	SMBus/I^{2}C Fan Speed Controller in ThinSOT™ Package	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz Floating or Grounded Lamp Configurations
LTC1840	Dual I^{2}C Fan Speed Controller	Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO
LTC4300A-1/ LTC4300A-2/ LTC4300A-3	Hot Swappable 2-Wire Bus Buffers	LTC4300A-1: Bus Buffer with READY, ACC and ENABLE LTC4300A-2: Dual Supply Bus Buffer with READY and ACC LTC4300A-3: Dual Supply Bus Buffer with READY and ENABLE
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Supply Independent
LTC4301L	Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation	Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN
LTC4302-1/LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled
LTC4303/LTC4304	Hot Swappable 2-Wire Bus Buffers with Stuck Bus Recovery	Provides Automatic Clocking to Free Stuck I^{2}C Busses
LTC4305/LTC4306	2-/4-Channel, 2-Wire Bus Multiplexers with Capacitance Buffering	2/4 Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD Tolerance
LTC4307	Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD Tolerance
LTC4307-1	High Definition Multimedia Interface (HDMI) Level Shifting 2-Wire Bus Buffer	60mV Buffer Offset, 3.3V to 5V Level Shifting, ±5kV HBM ESD Tolerance
LTC4309	Level Shifting Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, 1.8V to 5V Level Shifting, ±6kV HBM ESD Tolerance

ThinSOT is a trademark of Linear Technology Corporation

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