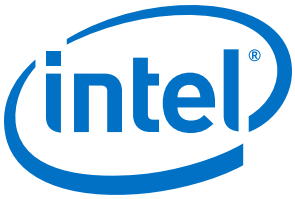

# 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.0**



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Latest document on the web: **PDF** | **HTML**

# Contents

# 1. About the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel® FPGA IP Core

The 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel® FPGA IP core for Intel Stratix® 10 devices (L- and H-Tiles) implements the Ethernet protocol as defined in the *IEEE 802.3 2005 Standard*. It consists of a physical coding sublayer (PCS) function and an embedded physical media attachment (PMA). You can dynamically switch the PHY operating speed.

*Note:* Intel FPGAs implement and support the required Media Access Control (MAC), PHY (PCS + PMA) IP to interface in a chip-to-chip or chip-to-module channel with external MGBASE-T and NBASE-T PHY standard devices. You are required to use an external PHY device to drive any copper media.

### Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Generating a Combined Simulator Setup Script
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

## 1.1. Features

**Table 1. 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core Features**

| Feature | Description |
|---|---|
| Operating speeds | 10M, 100M, 1G, 2.5G, 5G, and 10G. |
| MAC-side interface | 16-bit GMII for 10M/100M/1G/2.5G (MGBASE-T). |
| | 32-bit XGMII for 10M/100M/1G/2.5G/5G/10G (USXGMII/NBASE-T). |
| | 64-bit XGMII for 10G (MGBASE-T). |
| Network-side interface | 1.25 Gbps for 1G (MGBASE-T) and 10M/100M/1G (SGMII). |
| | 3.125 Gbps for 2.5G (MGBASE-T). |
| | 10.3125 Gbps for 10M/100M/1G/2.5G/5G/10G (USXGMII/NBASE-T) and 10G (MGBASE-T). |
| Avalon® Memory-Mapped (Avalon-MM) interface | Provides access to the configuration registers of the PHY. |
| Physical Coding Sublayer (PCS) function | 1000BASE-X for 1G and 2.5G. |

*continued...*

| Feature | Description |
|---|---|
| | 10GBASE-R for 10G. |
| | USXGMII PCS for 10M/100M/1G/2.5G/5G/10G (USXGMII). |
| | SGMII (10M/100M/1G) for 1G/2.5 and 1G/2.5/10G (MGBASE-T). |
| Auto-negotiation | Implements IEEE 802.3 clause 37. Supported in 1GbE only.<br>USXGMII Auto-negotiation supported in the 10M/100M/1G/2.5G/5G/10G (USXGMII/NBASE-T) configuration.<br>SGMII Auto-negotiation supported in the 10M/100M/1G (SGMII) configuration. |
| IEEE 1588v2 | Provides the required latency to the MAC if the MAC enables the IEEE 1588v2 feature.<br>Supported:<br>• 2.5G<br>• 1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII)<br>*Note:* For the 10M/100M/1G/2.5G/5G/10G (USXGMII) configuration, the provided latency is applicable only for 100M, 1G, 2.5G, 5G, and 10G modes.<br>Not Supported:<br>• 10M/100M/1G/2.5G<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |
| Sync-E | Provides the clock for Sync-E implementation. |

**Related Information**

IEEE website

For more information on IEEE 802.3.2005 and IEEE 1588 standards.

## 1.2. Device Family Support

**Table 2. Intel FPGA IP Core Device Support Levels**

| Device Support Level | Definition |
|---|---|
| **Advance** | The IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs). |
| **Preliminary** | The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution. |
| **Final** | The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs. |

**Table 3. Device Family Support for the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core**

| Device Family | Support Level |
|---|---|
| Intel Stratix 10 | Advance |

## 1.3. Device Speed Grade Support

**Table 4. Slowest Supported Device Speed Grades**

| Speed Mode | Supported Speed Grade | |
|---|---|---|
| | With 1588 Feature | Without 1588 Feature |
| 2.5G | E2, I2 | E3, I3 |
| 1G/2.5G | E2, I2 | E3, I3 |
| 10M/100M/1G/2.5G | - | E3, I3 |
| 1G/2.5G/10G (MGBASE-T) | E2, I2 | E3, I3 |
| 10M/100M/1G/2.5G/10G (MGBASE-T) | - | E3, I3 |
| 10M/100M/1G/2.5G/5G/10G (USXGMII) | E2, I2 | E3, I3 |

## 1.4. Resource Utilization

The following estimates are obtained by compiling the PHY IP core for Intel Stratix 10 devices using Intel Quartus® Prime software.

**Table 5. Resource Utilization**

| Speed | ALMs | ALUTs | Logic Registers | Memory Block (M20K) |
|---|---|---|---|---|
| 1G/2.5G | 790 | 940 | 1570 | 2 |
| 1G/2.5G with IEEE 1588v2 enabled | 1770 | 2390 | 3030 | 2 |
| 10M/100M/1G/2.5G | 810 | 980 | 1610 | 2 |
| 10M/100M/1G/2.5G/10G (MGBASE-T) | 1440 | 1790 | 2640 | 6 |
| 1G/2.5G/10G (MGBASE-T) | 1390 | 1740 | 2640 | 6 |
| 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 enabled | 3830 | 4630 | 5960 | 6 |
| 10M/100M/1G/2.5G/5G/10G (USXGMII) | 920 | 1120 | 1830 | 3 |
| 10M/100M/1G/2.5G/5G/10G (USXGMII) with IEEE 1588v2 enabled | 1760 | 2540 | 3510 | 4 |

## 1.5. Release Information

### Table 6. Release Information

| Item | Description |
|---|---|
| Version | Intel Quartus Prime Pro Edition 18.0 |
| Release Date | 2018.05.07 |
| Ordering Codes | IP-10GMRPHY |

# 2. Getting Started

The following section explains how to install, parameterize, simulate, and initialize the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core.

## 2.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

**Figure 1. IP Core Installation Path**

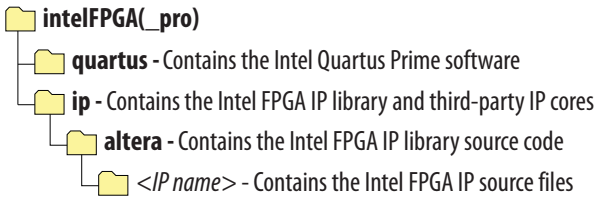



**Table 7. IP Core Installation Locations**

| Location | Software | Platform |
|---|---|---|
| *<drive>*:\intelFPGA_pro\quartus\ip\altera | Intel Quartus Prime Pro Edition | Windows* |
| *<home directory>*:/intelFPGA_pro/quartus/ip/altera | Intel Quartus Prime Pro Edition | Linux* |

### 2.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

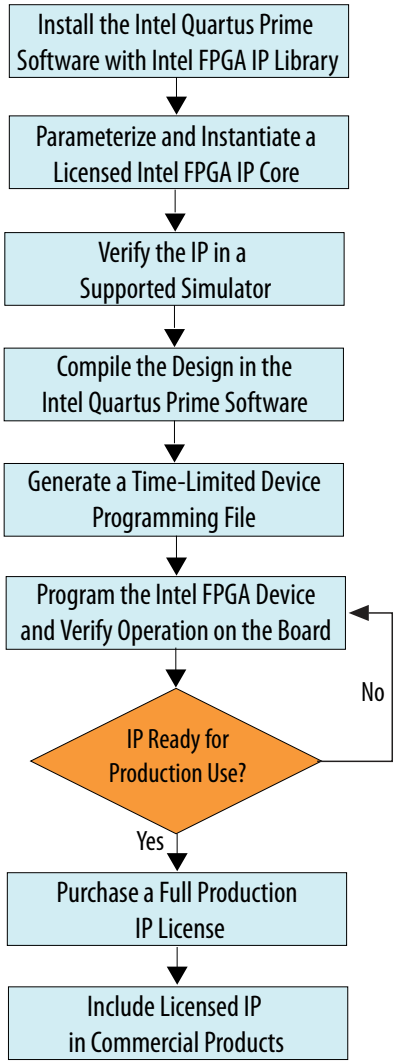
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (<*project name*>`_time_limited.sof`) that expires at the time limit.

**Figure 2. Intel FPGA IP Evaluation Mode Flow**




*Note:* Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

**Related Information**

- Intel Quartus Prime Licensing Site
- Intel FPGA Software Installation and Licensing

## 2.2. Specifying the IP Core Parameters and Options

The 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP parameter editor allows you to quickly configure your custom IP variation. Use the following steps to specify IP core options and parameters in the Intel Quartus Prime Pro Edition software:

1. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device.
2. In the IP Catalog (**Tools ➤ IP Catalog**), locate and double-click **1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP** core to customize. The **New IP Variant** window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named *<your_ip>*`.ip`.
4. Click **Create**. The parameter editor appears.
5. Specify the parameters for your IP core variation in the parameter editor. Refer to *Parameter Settings* for information about specific IP core parameters.
6. Optionally, to generate a MAC+PHY simulation testbench or compilation and hardware design example, follow the instructions in the *Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide*.
7. Click **Generate HDL**. The **Generation** dialog box appears.
8. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
9. Click **Finish**. The parameter editor adds the top-level `.ip` file to the current project automatically. If you are prompted to manually add the `.ip` file to the project, click **Project ➤ Add/Remove Files in Project** to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

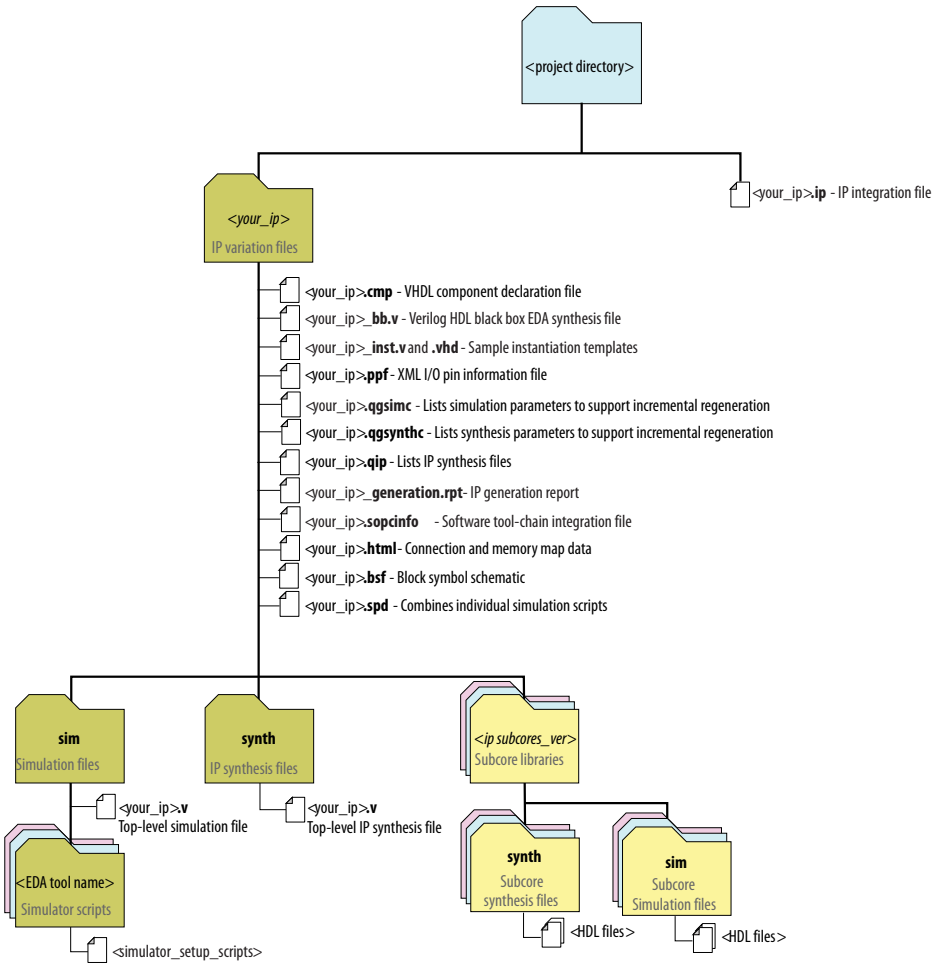
**Related Information**

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Parameter Settings on page 14

## 2.3. Generated File Structure

The Intel Quartus Prime Pro Edition software generates the following IP core output file structure.

## Figure 3. IP Core Generated Files




## Table 8. IP Core Generated Files

| File Name | Description |
|---|---|
| <*your_ip*>.ip | The Platform Designer system or top-level IP variation file. <*your_ip*> is the name that you give your IP variation. |
| <*your_ip*>.cmp | The VHDL Component Declaration (**.cmp**) file is a text file that contains local generic and port definitions that you can use in VHDL design files.<br>This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates this file. |
| <*your_ip*>.html | A report that contains connection information, a memory map showing the address of each slave with respect to each master to which it is connected, and parameter assignments. |
| <*your_ip*>_generation.rpt | IP or Platform Designer generation log file. A summary of the messages during IP generation. |
| <*your_ip*>.qgsimc | Lists simulation parameters to support incremental regeneration. |
| <*your_ip*>.qgsynthc | Lists synthesis parameters to support incremental regeneration. |

***continued...***

| File Name | Description |
|---|---|
| <*your_ip*>.qip | Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software. |
| <*your_ip*>.sopcinfo | Describes the connections and IP component parameterizations in your Platform Designer system. You can parse its contents to get requirements when you develop software drivers for IP components.<br>Downstream tools such as the Nios® II tool chain use this file. The .sopcinfo file and the system.h file generated for the Nios II tool chain include address map information for each slave relative to each master that accesses the slave. Different masters may have a different address map to access a particular slave component. |
| <*your_ip*>.csv | Contains information about the upgrade status of the IP component. |
| <*your_ip*>.bsf | A Block Symbol File (.**bsf**) representation of the IP variation for use in Intel Quartus Prime Block Diagram Files (**.bdf**). |
| <*your_ip*>.spd | Required input file for ip-make-simscript to generate simulation scripts for supported simulators. The **.spd** file contains a list of files generated for simulation, along with information about memories that you can initialize. |
| <*your_ip*>.ppf | The Pin Planner File (**.ppf**) stores the port and node assignments for IP components created for use with the Pin Planner. |
| <*your_ip*>_bb.v | You can use the Verilog black-box (**_bb.v**) file as an empty module declaration for use as a black box. |
| <*your_ip*>_inst.v or _inst.vhd | HDL example instantiation template. You can copy and paste the contents of this file into your HDL file to instantiate the IP variation.<br>This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates the _inst.vhd file. |
| <*your_ip*>.v | HDL files that instantiate each submodule or child IP core for synthesis or simulation. |
| mentor/ | Contains a ModelSim* script msim_setup.tcl to set up and run a simulation. |
| aldec/ | Contains a Riviera-PRO* script rivierapro_setup.tcl to setup and run a simulation.<br>ls |
| synopsys/vcs/<br>synopsys/vcsmx/ | Contains a shell script vcs_setup.sh to set up and run a VCS* simulation.<br>Contains a shell script vcsmx_setup.sh and synopsys_ sim.setup file to set up and run a VCS MX* simulation. |
| cadence/ | Contains a shell script ncsim_setup.sh and other setup files to set up and run an NCSim* simulation. |
| submodules/ | Contains HDL files for the IP core submodules. |
| <*child IP cores*>/ | For each generated child IP core directory, Platform Designer generates synth/ and sim/ sub-directories. |

## 2.4. Integrating Your IP Core in Your Design

### 2.4.1. Pin Assignments

When you integrate your 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core instance in your design, you must make appropriate pin assignments. While compiling the IP core alone, you can create virtual pins to avoid making specific pin assignments for top-level signals. When you are ready to map the design to hardware, you can change to the correct pin assignments.

## 2.4.2. Adding the Transceiver PLL

1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core requires an external PLL to drive TX serial clock, in order to compile and to function corrrectly in hardware. You must instantiate and connect ATX PLL/fPLL IP core to the 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP core.

You can create an external transceiver PLL from the IP Catalog. Select the **Intel Stratix 10 L-Tile/H-Tile Transceiver ATX PLL** core or **Intel Stratix 10 L-Tile/H-Tile fPLL** core.

**Table 9. Instantiate TX PLL**

| Speed | Reference Clock Frequency (MHz) | PLL Output Clock (MHz) |
|---|---|---|
| 1G | 125 | 625 |
| 2.5G | 125 | 1562.5 |
| 10G | 644.53125/322.265625 | 5156.25 |

### Related Information

PLLs and Clock Networks
Provides more information about the PLLs for the Intel Stratix 10 L- and H-Tile Transceiver PHY.

## 2.4.3. Adding the Intel Stratix 10 Transceiver PHY Reset Controller

You must add an Intel Stratix 10 Transceiver PHY Reset Controller IP core to your design, and connect it to the 1G/2.5/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core reset signals. This block implements a reset sequence that resets the device transceiver correctly.

You can use the IP Catalog to create a transceiver PHY reset controller.

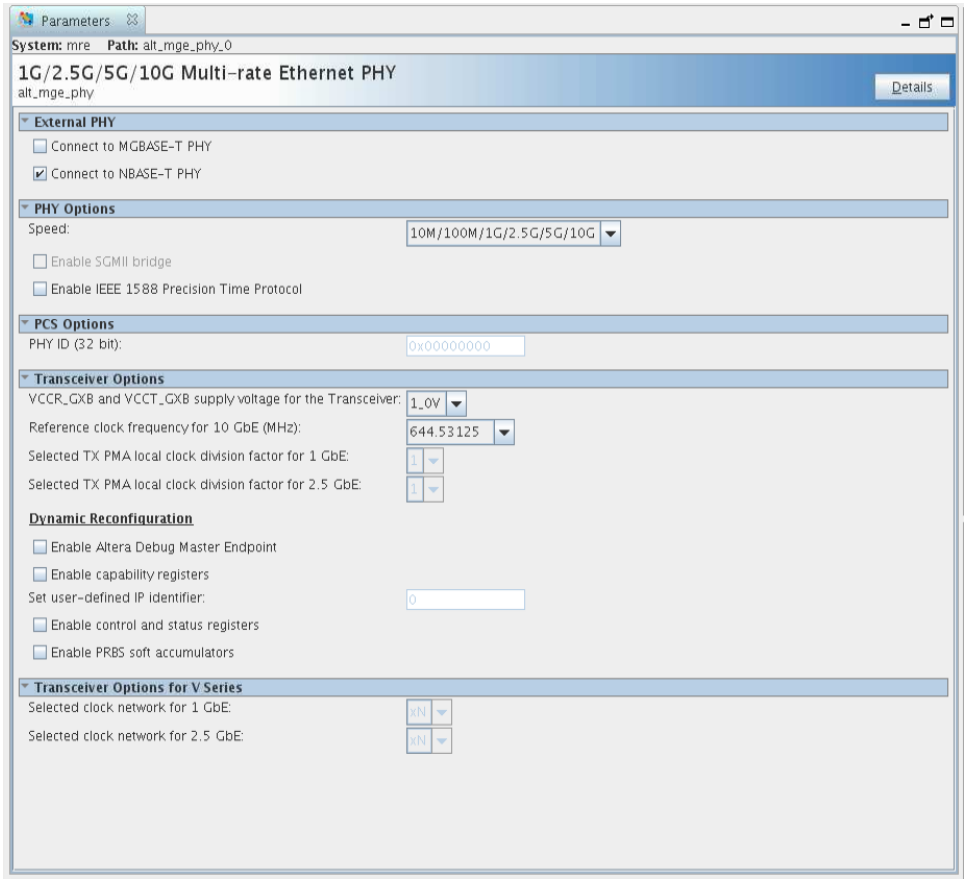
### Related Information

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Resetting Transceiver Channels
  Provides more information about resetting transceiver channels for the Intel Stratix 10 L- and H-Tile Transceiver PHY.

# 3. Parameter Settings

You can select the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core for Intel Stratix 10 devices from the Intel Quartus Prime Pro Edition IP catalog. To customize the PHY IP core, specify the parameters in the IP parameter editor. The parameter editor dynamically enables the parameter options that apply to the selected operating speed.

**Figure 4. IP Parameter Editor**



## Table 10. 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core Parameters

| Parameter | Options | Description |
|---|---|---|
| External PHY | | |
| **Connect to MGBASE-T PHY** | On, Off | Select this option when the external PHY is MGBASE-T compatible.<br>This parameter is enabled for 2.5G, 1G/2.5G, and 1G/2.5G/10G (MGBASE-T) modes. |
| **Connect to NBASE-T PHY** | On, Off | Select this option when the external PHY is NBASE-T compatible.<br>This parameter is enabled for 10M/100M/1G/2.5G/5G/10G (USXGMII) modes. |
| PHY Options | | |
| **Speed** | 2.5G<br>1G/2.5G<br>1G/2.5G/10G<br>10M/100M/1G/2.5G/5G/10G | The operating speed of the PHY. |
| **Enable SGMII bridge** | On, Off | Select this parameter to enable SGMII 10-Mbps/100-Mbps/1-Gbps.<br>You can enable this parameter for 1G/2.5G, and 1G/2.5G/10G (MGBASE-T) modes. |
| **Enable IEEE 1588 Precision Time Protocol** | On, Off | Select this parameter for the PHY to provide latency information to the MAC. The MAC requires this information if it enables the IEEE 1588v2 feature.<br>You can enable this parameter for 2.5G, 1G/2.5G, 1G/2.5G/10G (MGBASE-T), and 10M/100M/1G/2.5G/5G/10G (USXGMII) modes provided that the SGMII bridge is disabled in 1G/2.5G and 1G/2.5G/10G (MGBASE-T) modes. |
| PCS Options | | |
| **PHY ID (32 bit)** | 32-bit value | An optional 32-bit unique identifier:<br>• Bits 3 to 24 of the Organizationally Unique Identifier (OUI) assigned by the IEEE<br>• 6-bit model number<br>• 4-bit revision number<br>The default value is 0x00000000. |
| Transceiver Options | | |
| **VCCR_GXB and VCCT_GXB supply voltage for the transceivers** | 1.0 V, 1.1 V | This parameter specifies the VCCR_GXB and VCCT_GXB transceiver supply voltage. The default setting is 1.0 V.<br>Use 1.1 V setting if the bank contains transceivers running at 15 Gbps or faster. |
| **Reference clock frequency for 10 GbE (MHz)** | 322.265625, 644.53125 | Specify the frequency of the reference clock for 10GbE.<br>This option is only available for 1G/2.5G/10G and 10M/100M/1G/2.5G/5G/10G (USXGMII) speed modes. |
| **Selected TX PMA local clock division factor for 1 GbE** | 1, 2, 4, 8 | Select the TX local clock division factor for transceiver. The selection is used for 1G Ethernet. |
| **Selected TX PMA local clock division factor for 2.5 GbE** | 1, 2 | Select the TX local clock division factor for transceiver. The selection is used for 2.5G Ethernet. |
| Dynamic Reconfiguration | | |

***continued...***

| Parameter | Options | Description |
|---|---|---|
| **Enable Altera Debug Master Endpoint** | On, Off | When enabled, the Native PHY includes an embedded Altera Debug Master Endpoint (ADME) that connects internally Avalon-MM slave interface. The ADME can access the reconfiguration space of the transceiver. It can perform certain test and debug functions via JTAG using the System Console. |
| **Enable capability registers** | On, Off | Enables capability registers. These registers provide high-level information about the transceiver channel/PLL configuration. |
| **Set user-defined IP identifier** | User-specified | Sets a user-defined numeric identifier that can be read from the `user_identifier` offset when the capability registers are enabled. |
| **Enable control and status registers** | On, Off | Enables soft registers for reading status signals and writing control signals on the PHY /PLL interface through the ADME or reconfiguration interface. |
| **Enable PRBS soft accumulators** | On, Off | Enables soft logic to perform PRBS bit and error accumulation when using the hard PRBS generator and checker. |

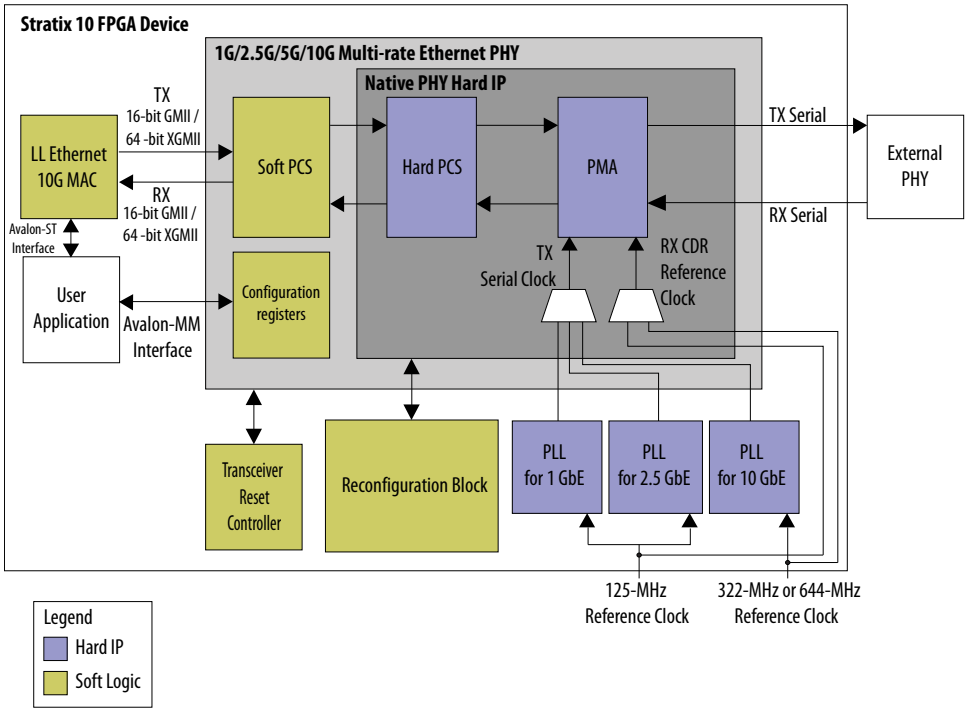
### Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
More information on Altera Debug Master Endpoint (ADME).

# 4. Functional Description

The 1G/2.5G/5G/10G Multi-rate PHY Intel FPGA IP core for Intel Stratix 10 devices implements the 10M to 10Gbps Ethernet PHY in accordance with the IEEE 802.3 Ethernet Standard. This IP core handles the frame encapsulation and flow of data between a client logic and Ethernet network via a 10M to 10GbE PCS and PMA (PHY). You can use the Native PHY IP core to configure the transceiver PHY for your protocol implementation. Refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide* for more information on using the Native PHY IP core.

**Figure 5. Architecture of 2.5G, 1G/2.5G, 10M/100M/1G/2.5G, 1G/2.5G/10G, 10M/100M/1G/2.5G/10G (MGBASE-T) Configuration**




In the transmit direction, the PHY encodes the Ethernet frame as required for reliable transmission over the media to the remote end. In the receive direction, the PHY passes frames to the MAC.

*Note:* You can generate the MAC and PHY design example using the Low Latency Ethernet 10G MAC Intel FPGA IP Parameter Editor.

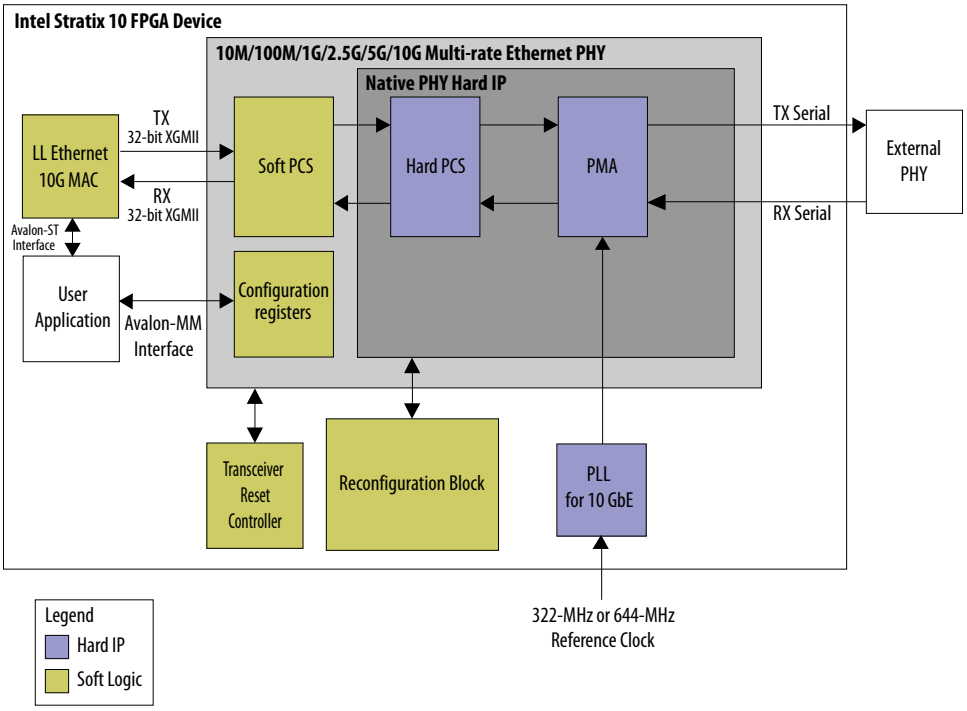
The IP core includes the following interfaces:

- Datapath client-interface:
  - 10GbE—XGMII, 64 bits
  - 10M/100M/1G/2.5GbE—GMII, 16 bit
  - 10M/100M/1G/2.5G/5G/10G (USXGMII)—XGMII, 32 bits

  For 1G/2.5/10G (MGBASE-T), select an interface based on the respective operating speed.
- Management interface—Avalon-MM host slave interface for PHY management.
- Datapath Ethernet interface with the following available options:
  - 10GbE—Single 10.3125 Gbps serial link
  - 2.5GbE—Single 3.125 Gbps serial link
  - 10M/100M/1GbE—Single 1.25 Gbps SGMII serial link
  - 10M/100M/1G/2.5G/5G/10G (USXGMII) —Single 10.3125 Gbps serial link

  For 1G/2.5/10G (MGBASE-T), select an ethernet interface based on the respective operating speed.
- Transceiver PHY dynamic reconfiguration interface—an Avalon-MM interface to read and write the Intel Stratix 10 Native PHY IP core registers. This interface supports dynamic reconfiguration of the transceiver. It is used to configure the transceiver operating modes to switch to desired Ethernet operating speeds.

**Figure 6. Architecture of 10M/100M/1G/2.5G/5G/10G (USXGMII) Configuration**




The 10M/100M/1G/2.5G/5G/10G (USXGMII) configuration supports the following features:

- USXGMII—10M/100M/1G/2.5G/5G/10G speeds
- Full duplex data transmission
- USXGMII Auto-Negotiation

**Related Information**

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

## 4.1. Clocking and Reset Sequence

Clocking Requirements:

- For 64-bit XGMII, the 156.25 MHz clock must have zero ppm difference with reference clock of 10G transceiver PLL. Therefore, the 156.25 MHz clock must derived from the transceiver 10G reference clock for 1G/2.5G/10G (MGBASE-T) variant.
- For 32-bit XGMII, the 312.5 MHz clock must have zero ppm difference with reference clock of 10G transceiver PLL. Therefore, the 312.5 MHz clock must derived from the transceiver 10G reference clock for 10M/100M/1G/2.5G/5G/10G (USXGMII) variant.

Reset sequence for all configurations is handled by the transceiver reset controller. For 1G/2.5G and 1G/2.5G/10G (MGBASE-T), transceiver reset sequence is automatically triggered after completion of speed switching/reconfiguration in the MAC+PHY example design.

The 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core for Intel Stratix 10 devices supports up to ±100 ppm clock frequency difference.

**Related Information**

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

## 4.2. Timing Constraints

Constrain the PHY based on the fastest speed. For example, if you configure the PHY as 1G/2.5G, constrain it based on 2.5G.

**Table 11. Timing Constraints**

| PHY Configuration | Constrain PHY for |
|---|---|
| 2.5G | 2.5G datapath |
| 1G/2.5G | 2.5G datapath |
| 1G/2.5G/10G (MGBASE-T) | 10G and 1G/2.5G datapath |
| 10M/100M/1G/2.5G/5G/10G (USXGMII) | 10G datapath |
| 10M/100M/1G/2.5G | 2.5G datapath |
| 10M/100M/1G/2.5G/10G (SGMII/MGBASE-T) | 10G and 1G/2.5G datapath |

When you configure the PHY in 1G/2.5G/10G (MGBASE-T) configuration, Intel recommends that you add the following constraints in the timing constraint file:

- Set false path for the clocks used for the different speed so that the Timing Analyzer ignores paths for clocks that are in different groups. For example:

```
set_clock_groups -physically_exclusive -group [get_clocks {DUT|
CHANNEL_GEN[0].u_channel|phy|alt_mge_phy_0|profile0|*}] \
                                          -group [get_clocks {DUT|
CHANNEL_GEN[0].u_channel|phy|alt_mge_phy_0|profile1|*}] \
                                          -group [get_clocks {DUT|
CHANNEL_GEN[0].u_channel|phy|alt_mge_phy_0|profile2|*}]
```

  where `profile0`, `profile1`, and `profile2` are created by the transceiver native PHY Synopsys Design Constraint (SDC) for 1G, 2.5G, and 10G clocks respectively.

- Set false path from native PHY 10G clock to 1G/2.5G PHY logic and vice versa. Since the 1G/2.5G PHY logic is not running native PHY 10G clock, you do not need to ensure timing closure for the 1G/2.5G data path at 10G clock. For example:

```
set_false_path -from [get_clocks {DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile2|*}] \
               -to [get_registers {*|alt_mge16_pcs_pma:*|*}]
set_false_path -from [get_registers {*|alt_mge16_pcs_pma:*|*}] \
               -to [get_clocks {DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile2|*}]
```

  where the path indicated by `profile2` is associated to the native PHY 10G clock, whereas the `alt_mge16_pcs_pma` path indicates the 1G/2.5G PHY logic.

- Set false path from native PHY 1G and 2.5G clock to 10G PHY logic and vice versa. Since the 10G PHY logic is not running the native PHY 1G and 2.5G clocks, you do not need to ensure timing closure for the 10G data path at the native PHY 1G and 2.5G clocks. For example:

```
set_false_path -from [get_clocks {DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile0|* \
                                    DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile1|*}] \
               -to [get_registers *|alt_mge_phy_xgmii_pcs:*|*]
set_false_path -from [get_registers *|alt_mge_phy_xgmii_pcs:*|*] \
               -to [get_clocks {DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile0|* \
                                  DUT|CHANNEL_GEN[*].u_channel|phy|
alt_mge_phy_0|profile1|*}]
```

  where the paths indicated by `profile0` and `profile1` are associated to the native PHY 1G and 2.5G clocks respectively, whereas the `alt_mge_phy_xgmii_pcs` path indicates the 10G PHY logic.

When you configure the PHY in 1G/2.5G configuration, Intel recommends that you add the following constraint in the timing constraint file:

- Set false path for the clocks used for the different speed so that the Timing Analyzer ignores paths for clocks that are in different groups. For example:

```
set_clock_groups -physically_exclusive -group [get_clocks {DUT|
CHANNEL_GEN[0].u_channel|phy|alt_mge_phy_0|profile0|*}] \
                                          -group [get_clocks {DUT|
CHANNEL_GEN[0].u_channel|phy|alt_mge_phy_0|profile1|*}]
```

  where `profile0` and `profile1` are created by the transceiver native PHY SDC for the 1G and 2.5G clocks respectively.

## 4.3. Switching Operation Speed

**Table 12. Supported Operating Speed**

| PHY Configurations | Features | 10M | 100M | 1G | 2.5G | 5G | 10G |
|---|---|---|---|---|---|---|---|
| 2.5G | Protocol | — | — | — | 1000BASE-X at 2.5x | — | — |
| | Transceiver Data Rate | — | — | — | 3.125 Gbps | — | — |
| | MAC Interface | — | — | — | 16-bit GMII @ 156.25 MHz | — | — |
| 10M/ 100M/1G/ 2.5G | Protocol | SGMII 100x data replication | SGMII 10x data replication | 1000BASE-X / SGMII | 1000BASE-X at 2.5x | — | — |
| | Transceiver Data Rate | 1.25 Gbps | 1.25 Gbps | 1.25 Gbps | 3.125 Gbps | — | — |
| | MAC Interface | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 156.25 MHz | — | — |
| 10M/ 100M/1G/ 2.5G/10G (MGBASE-T) | Protocol | SGMII | SGMII 10x data replication | 1000BASE-X / SGMII | 1000BASE-X at 2.5x | — | 10GBASE-R |
| | Transceiver Data Rate | 1.25 Gbps | 1.25 Gbps | 1.25 Gbps | 3.125 Gbps | — | 10.3125 Gbps |
| | MAC Interface | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 62.5 MHz | 16-bit GMII @ 156.25 MHz | — | 64-bit XGMII @ 156.25 MHz |
| 10M/ 100M/1G/ 2.5G/5G/10G (USXGMII) | Protocol | 10GBASE-R 1000x data replication | 10GBASE-R 100x data replication | 10GBASE-R 10x data replication | 10GBASE-R 4x data replication | 10GBASE-R 2x data replication | 10GBASE-R No data replication |
| | Transceiver Data Rate(1) | 10.3125 Gbps | 10.3125 Gbps | 10.3125 Gbps | 10.3125 Gbps | 10.3125 Gbps | 10.3125 Gbps |
| | MAC Interface | 32-bit XGMII @ 312.5 MHz | 32-bit XGMII @ 312.5 MHz | 32-bit XGMII @ 312.5 MHz | 32-bit XGMII @ 312.5 MHz | 32-bit XGMII @ 312.5 MHz | 32-bit XGMII @ 312.5 MHz |

You can change the PHY speed using the reconfiguration block in the MAC+PHY example design.

1. Initiates the speed change by writing to the corresponding register of the reconfiguration block.(2)
2. The reconfiguration block performs the following steps:

(1) With oversampling for lower data rates.

a. Sets the `xcvr_mode` signal of the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core to the requested speed.

b. Reads the generated `.mif` file for the configuration settings and configures the transceiver accordingly.

c. Selects the corresponding transceiver PLL.

d. Triggers the transceiver recalibration.

3. The reconfiguration block triggers the PHY reset through the transceiver reset controller.

### Related Information

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Register Definitions on page 23

(2) You can change the speed within SGMII (10M/100M/1G) and USXGMII (10M/100M/1G/2.5G/5G/10G) through CSR. It doesn't require reconfiguration block.

# 5. Configuration Registers

## 5.1. Register Map

You can access the 16-bit/32-bit configuration registers [3] via the Avalon-MM interface.

**Table 13. Register Map Overview**

| Address Range | Usage | Register Width | Configuration |
|---|---|---|---|
| 0x00–0x1F | 1000BASE-X/SGMII | 16 | 2.5G, 1G/2.5G, 10M/100M/1G/2.5G, 10M/100M/1G/2.5G/10G (MGBASE-T), 1G/2.5G/10G (MGBASE-T) |
| 0x400–0x41F | USXGMII | 32 | 10M/100M/1G/2.5G/5G/10G (USXGMII) |
| 0x461 | Serial Loopback | 32 | 10M/100M/1G/2.5G/5G/10G (USXGMII) |

## 5.2. Register Definitions

Observe the following guidelines when accessing the registers:

- Do not write to reserved or undefined registers.
- When writing to the registers, perform read-modify-write operation to ensure that reserved or undefined register bits are not overwritten.

**Table 14. Types of Register Access**

| Access | Definition |
|---|---|
| RO | Read only. |
| RW | Read and write. |
| RWC | Read, write and clear. The user application writes 1 to the register bit(s) to invoke a defined instruction. The IP core clears the bit(s) upon executing the instruction. |

[3] These registers are identical to the Intel Arria® 10 variation of 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core.

## Table 15. PHY Registers

| Address | Name | Description | Access | HW Reset Value |
|---|---|---|---|---|
| 0x00 | control | Bit [15]: RESET. Set this bit to 1 to trigger a soft reset.<br>The PHY clears the bit when the reset is completed. The register values remain intact during the reset. | RWC | 0 |
| | | Bit[14]: LOOPBACK. Set this bit to 1 to enable loopback on the serial interface. | RW | 0 |
| | | Bit [12]: AUTO_NEGOTIATION_ENABLE. Set this bit to 1 to enable auto-negotiation.<br>Auto-negotiation is supported only in 1GbE. Therefore, set this bit to 0 when you switch to a speed other than 1GbE. | RW | 0 |
| | | Bit [9]: RESTART_AUTO_NEGOTIATION. Set this bit to 1 to restart auto-negotiation.<br>The PHY clears the bit as soon as auto-negotiation is restarted. | RWC | 0 |
| | | All other bits are reserved. | — | — |
| 0x01 | status | Bit [5]: AUTO_NEGOTIATION_COMPLETE. A value of "1" indicates that the auto-negotiation is completed. | RO | 0 |
| | | Bit [3]: AUTO_NEGOTIATION_ABILITY. A value of "1" indicates that the PCS function supports auto-negotiation. | RO | 1 |
| | | Bit [2]: LINK_STATUS. A value of "0" indicates that the link is lost. A value of "1" indicates that the link is established. | RO | 0 |
| | | All other bits are reserved. | — | — |
| 0x02:0x03 | phy_identifier | The value set in the **PHY_IDENTIFIER** parameter. | RO | Value of PHY_IDENTIFIER parameter |
| 0x04 | dev_ability | Use this register to advertise the device abilities during auto-negotiation. | — | — |
| | | Bits [13:12]: RF. Specify the remote fault.<br>• 00: No error.<br>• 01: Link failure.<br>• 10: Off-line.<br>• 11: Auto-negotiation error. | RW | 00 |
| | | Bits [8:7]: PS. Specify the PAUSE support.<br>• 00: No PAUSE.<br>• 01: Symmetric PAUSE.<br>• 10: Asymmetric PAUSE towards the link partner.<br>• 11: Asymmetric and symmetric PAUSE towards the link device. | RW | 11 |
| | | Bit [5]: FD. Ensure that this bit is always set to 1. | RW | 1 |
| | | All other bits are reserved. | — | — |
| 0x05 (1000BASE-X mode) | partner_ability | The device abilities of the link partner during auto-negotiation. | — | — |

*continued...*

| Address | Name | Description | Access | HW Reset Value |
|---|---|---|---|---|
| | | Bit [14]: ACK. A value of "1" indicates that the link partner has received three consecutive matching ability values from the device. | RO | 0 |
| | | Bits [13:12]: RF. The remote fault.<br>• 00: No error.<br>• 01: Link failure.<br>• 10: Off-line.<br>• 11: Auto-negotiation error. | RO | 0 |
| | | Bits [8:7]: PS. The PAUSE support.<br>• 00: No PAUSE.<br>• 01: Symmetric PAUSE.<br>• 10: Asymmetric PAUSE towards the link partner.<br>• 11: Asymmetric and symmetric PAUSE towards the link device. | RO | 0 |
| | | Bit [6]: HD. A value of "1" indicates that half-duplex is supported. | RO | 0 |
| | | Bit [5]: FD. A value of "1" indicates that full-duplex is supported. | RO | 0 |
| | | All other bits are reserved. | — | — |
| 0x05 (SGMII mode) | `partner_ability` | The device abilities of the link partner during auto-negotiation. | — | — |
| | | Bit [11:10]: `COPPER_SPEED`<br>Link partner speed:<br>• 00: copper interface speed is 10 Mbps<br>• 01: copper interface speed is 100 Mbps<br>• 10: copper interface speed is 1 Gigabit<br>• 11: reserved | RO | 00 |
| | | Bit [12]: `COPPER_DUPLEX_STATUS`<br>Link partner capability:<br>• 1: copper interface is capable of full-duplex operation<br>• 0: copper interface is capable of half-duplex operation | RO | 0 |
| | | Bit [14]: ACK. Link partner acknowledge. A value of 1 indicates that the device received three consecutive matching ability values from its link partner. | RO | 0 |
| | | Bit [15]: `COPPER_LINK_STATUS`<br>Link partner status:<br>• 1: copper interface link is up<br>• 0: copper interface link is down | RO | 0 |
| | | All other bits are reserved. | — | — |
| 0x06 | `an_expansion` | The PCS capabilities and auto-negotiation status. | — | — |
| | | Bit [1]: `PAGE_RECEIVE`. A value of "1" indicates that the partner_ability register has been updated. This bit is automatically cleared once it is read. | RO | 0 |
| | | Bit [0]: `LINK_PARTNER_AUTO_NEGOTIATION_ABLE`. A value of "1" indicates that the link partner supports auto-negotiation. | RO | 0 |

***continued...***

| Address | Name | Description | Access | HW Reset Value |
|---|---|---|---|---|
| 0x07 | device_next_page | The PHY does not support the next page feature. These registers are always set to 0. | RO | 0 |
| 0x08 | partner_next_page | | RO | 0 |
| 0x09:0x0F | Reserved | — | — | — |
| 0x10 | scratch | Provides a memory location to test read and write operations. | RW | 0 |
| | | Bit [31:16]: Reserved | — | — |
| 0x11 | rev | The current version of the PHY IP core. | RO | Current version of the PHY |
| | | Bit [31:16]: Reserved | — | — |
| 0x12:0x13 | link_timer | 21-bit auto-negotiation link timer spans across two 16-bit registers, which have offset 0x12 and offset 0x13.<br>• Offset 0x12: link_timer[15:0]. Bits [8:0] are always be set to 0.<br>• Offset 0x13: link_timer[20:16] occupies the lower 5 bits. The remaining 11 bits are reserved and must always be set to 0. | RW | 0 |
| 0x14 | if_mode | Interface Mode Register | — | — |
| | | Bit [0]: SGMII_ENA<br>Determines the PCS function operating mode. Setting this bit to 1b'1 enables SGMII mode. Setting this bit to 1b'0 enables 1000BASE-X gigabit mode. | RW | 0 |
| | | Bit [1]: USE_SGMII_AN<br>In SGMII mode, setting this bit to 1b'1 configures the PCS with the link partner abilities advertised during auto-negotiation. If this bit is set to 1b'0, the PCS function should be configured with the SGMII_SPEED bits. | RW | 0 |
| | | Bit [3:2]: SGMII_SPEED<br>When the PCS operates in SGMII mode (SGMII_ENA = 1) and is not programmed for automatic configuration (USE_SGMII_AN = 0), the following encodings specify the speed:<br>• 2'b00: 10 Mbps<br>• 2'b01: 100 Mbps<br>• 2'b10: Gigabit<br>• 2'b11: Reserved<br>These bits are not used when SGMII_ENA = 0 or USE_SGMII_AN = 1. | RW | 0 |
| | | All other bits are reserved. | — | — |
| 0x15:0x1F | Reserved | — | — | — |
| 0x400 | usxgmii_control | Control Register | — | — |
| | | Bit [0]: USXGMII_ENA:<br>• 0: 10GBASE-R mode<br>• 1: USXGMII mode | RW | 0 |

continued...

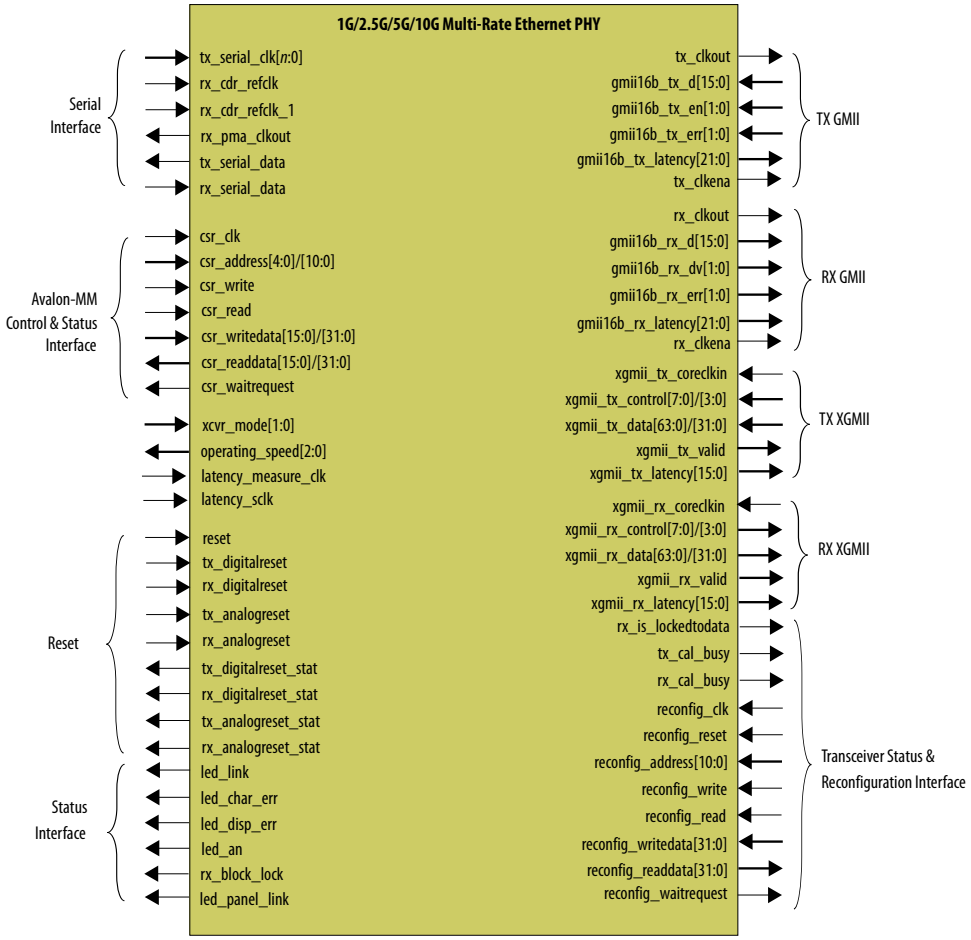
| Address | Name | Description | Access | HW Reset Value |
|---|---|---|---|---|
| | | Bit [1]: USXGMII_AN_ENA is used when USXGMII_ENA is set to 1:<br>• 0: Disables USXGMII Auto-Negotiation and manually configures the operating speed with the USXGMII_SPEED register.<br>• 1: Enables USXGMII Auto-Negotiation, and automatically configures operating speed with link partner ability advertised during USXGMII Auto-Negotiation. | RW | 1 |
| | | Bit [4:2]: USXGMII_SPEED is the operating speed of the PHY in USXGMII mode and USE_USXGMII_AN is set to 0.<br>• 3'b000: 10M<br>• 3'b001: 100M<br>• 3'b010: 1G<br>• 3'b011: 10G<br>• 3'b100: 2.5G<br>• 3'b101: 5G<br>• 3'b110: Reserved<br>• 3'b111: Reserved | RW | 0 |
| | | Bit [8:5]: Reserved | — | — |
| | | Bit [9]: RESTART_AUTO_NEGOTIATION<br>Write 1 to restart Auto-Negotiation sequence The bit is cleared by hardware when Auto-Negotiation is restarted. | RWC | 0 |
| | | Bit [31:10]: Reserved | — | — |
| 0x401 | usxgmii_status | Status Register | — | — |
| | | Bit [1:0]: Reserved | — | — |
| | | Bit [2]: LINK_STATUS indicates link status for USXGMII all speeds<br>• 1: Link is established<br>• 0: Link synchronization is lost, a 0 is latched | RO | 0 |
| | | Bit [4:3]: Reserved | — | — |
| | | Bit [5]: AUTO_NEGOTIATION_COMPLETE<br>A value of 1 indicates the Auto-Negotiation process is completed. | RO | 0 |
| | | Bit [31:6]: Reserved | — | — |
| 0x402:0x404 | Reserved | — | — | — |
| 0x405 | usxgmii_partner_ability | Device abilities advertised to the link partner during Auto-Negotiation | — | — |
| | | Bit [6:0]: Reserved | — | — |
| | | Bit [7]: EEE_CLOCK_STOP_CAPABILITY<br>Indicates whether or not energy efficient Ethernet (EEE) clock stop is supported.<br>• 0: Not supported<br>• 1: Supported | RO | 0 |
| | | Bit [8]: EEE_CAPABILITY<br>Indicates whether or not EEE is supported. | RO | 0 |

***continued...***

| Address | Name | Description | Access | HW Reset Value |
|---|---|---|---|---|
| | | • 0: Not supported<br>• 1: Supported | | |
| | | Bit [11:9]: SPEED<br>• 3'b000: 10M<br>• 3'b001: 100M<br>• 3'b010: 1G<br>• 3'b011: 10G<br>• 3'b100: 2.5G<br>• 3'b101: 5G<br>• 3'b110: Reserved<br>• 3'b111: Reserved | RO | 0 |
| | | Bit [12]: DUPLEX<br>Indicates the duplex mode.<br>• 0: Half duplex<br>• 1: Full duplex | RO | 0 |
| | | Bit [13]: Reserved | — | — |
| | | Bit [14]: ACKNOWLEDGE<br>A value of 1 indicates that the device has received three consecutive matching ability values from its link partner. | RO | 0 |
| | | Bit [15]: LINK<br>Indicates the link status.<br>• 0: Link down<br>• 1: Link up | RO | 0 |
| | | Bit [31:16]: Reserved | — | — |
| 0x406:0x411 | Reserved | — | — | — |
| 0x412 | usxgmii_link_timer | Auto-Negotiation link timer. Sets the link timer value in bit [19:14] from 0 to 2 ms in approximately 0.05-ms steps. You must program the link timer to ensure that it matches the link timer value of the external NBASE-T PHY IP Core.<br>The reset value sets the link timer to approximately 1.6 ms.<br>Bits [13:0] are reserved and always set to 0. | [19:14]: RW<br>[13:0]: RO | [19:14]: 1F<br>[13:0]: 0 |
| 0x413:0x41F | Reserved | — | — | — |
| 0x461 | phy_serial_loopback | Configures the transceiver serial loopback in the PMA from TX to RX. | — | — |
| | | Bit [0]<br>• 0: Disables the PHY serial loopback<br>• 1: Enables the PHY serial loopback | RW | 0 |
| | | Bit [31:1]: Reserved | — | — |

# 6. Interface Signals

**Figure 7. Interface Signals**




*n*: Number of serial clocks from transceiver PLL.

## 6.1. Clock and Reset Signals

### Table 16. Clock and Reset Signals

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| Clock signals | | | | |
| tx_clkout | Output | 1 | GMII TX clock, derived from tx_serial_clk[1:0]. Provides 156.25 MHz timing reference for 2.5GbE; 62.5 MHz for 1GbE; 6.25 MHz for 100M; 0.625 MHz for 10M. | • 2.5G<br>• 1G/2.5G<br>• 10M/100M/1G, 2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/10G (MGBASE-T) |
| rx_clkout | Output | 1 | GMII RX clock, derived from tx_serial_clk[1:0]. Provides 156.25 MHz timing reference for 2.5GbE; 62.5 MHz for 1GbE; 6.25 MHz for 100M; 0.625 MHz for 10M. | • 2.5G<br>• 1G/2.5G<br>• 10M/100M/1G/ 2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/10G (MGBASE-T) |
| csr_clk | Input | 1 | Clock for the Avalon-MM control and status interface. Intel recommends 125 – 156.25 MHz for this clock. | All |
| xgmii_tx_coreclkin | Input | 1 | XGMII TX clock. Provides 156.25 MHz timing reference for 10GbE and 312.5 MHz for 10M/100M/1G/2.5G/5G/10G (USXGMII) mode. Synchronous to tx_serial_clk with zero ppm. | • 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/5G/10G (USXGMII) |
| xgmii_rx_coreclkin | Input | 1 | XGMII RX clock. Provides 156.25 MHz timing reference for 10GbE and 312.5 MHz for 10M/100M/1G/2.5G/5G/10G (USXGMII) mode. | • 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/ 2.5G/5G/10G (USXGMII) |
| latency_measure_clk | Input | 1 | Sampling clock for measuring the latency of the 16-bit GMII datapath. This clock operates at 80 MHz and is available only when the IEEE 1588v2 feature is enabled. | • 2.5G<br>• 1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature |

*continued...*

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| latency_sclk | Input | 1 | Sampling clock for measuring the latency of the transceiver AIB datapath. The clock period is 6.5 ns. It is available only when the IEEE 1588v2 feature is enabled. | • 2.5G<br>• 1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) |
| Serial interface clock signals | | | | |
| tx_serial_clk | Input | 1-3 | Serial clock from transceiver PLLs.<br>• 2.5GbE: Connect bit [0] to the transceiver PLL. This clock operates at 1562.5 MHz.<br>• 1GbE: Connect bit [1] to the transceiver PLL. This clock operates at 625 MHz.<br>• 10GbE: Connect bit [2] to the transceiver PLL. This clock operates at 5156.25 MHz.<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) mode: Connect bit [0] to 5156.25 MHz. | All |
| rx_cdr_refclk | Input | 1 | 125-MHz RX CDR reference clock for 1GbE and 2.5GbE | • 2.5G<br>• 1G/2.5G, 10M/100M/1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |
| rx_cdr_refclk_1 | Input | 1 | RX CDR reference clock for 10G of 1G/2.5G/10G (MGBASE-T) and all speeds of USXGMII. The frequency of this clock can be either 322.265625 MHz or 644.53125 MHz, as specified by the **Reference clock frequency for 10 GbE (MHz)** parameter setting. | • 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) |
| rx_pma_clkout | Output | 1 | Recovered clock from CDR, operates at the following frequency:<br>• 1GbE: 125 MHz<br>• 2.5GbE: 312.5 MHz<br>• 10GbE: 322.265625 MHz | All |
| Reset signals | | | | |
| reset | Input | 1 | Active-high global reset. Assert this signal to trigger an asynchronous global reset. | All |
| tx_analogreset | Input | 1 | Connect this signal to the Transceiver PHY Reset Controller IP core. When asserted, triggers an asynchronous reset to the analog block on the TX path. | All |
| tx_analogreset_stat | Output | 1 | Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device. | All |

***continued...***

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| tx_digitalreset | Input | 1 | Connect this signal to the Transceiver PHY Reset Controller IP core. When asserted, triggers an asynchronous reset to the digital logic on the TX path. | All |
| tx_digitalreset_stat | Output | 1 | Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device. | All |
| rx_analogreset | Input | 1 | Connect this signal to the Transceiver PHY Reset Controller IP core. When asserted, triggers an asynchronous reset to the receiver CDR. | All |
| rx_analogreset_stat | Output | 1 | Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device. | All |
| rx_digitalreset | Input | 1 | Connect this signal to the Transceiver PHY Reset Controller IP core. When asserted, triggers an asynchronous reset to the digital logic on the RX path. | All |
| rx_digitalreset_stat | Output | 1 | Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device. | All |

## 6.2. Transceiver Mode and Operating Speed Signals

**Table 17. Transceiver Mode and Operating Speed Signals**

| Signal Name | Direction | Width | Description | PHY configurations |
|---|---|---|---|---|
| xcvr_mode | Input | 2 | Connect this signal to the reconfiguration block. Use the following values to set the speed:<br>• 0x0 = 1G<br>• 0x1 = 2.5G<br>• 0x3 = 10G | • 2.5G<br>• 1G/2.5G<br>• 10M/100M/1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |
| operating_speed | Output | 3 | Connect this signal to the MAC. This signal provides the current operating speed of the PHY:<br>• 0x0 = 10G<br>• 0x1 = 1G<br>• 0x2 = 100M<br>• 0x3 = 10M<br>• 0x4 = 2.5G<br>• 0x5 = 5G | All |

## 6.3. Serial Interface Signals

The serial interface connects to an external device.

**Table 18. Serial Interface Signals**

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| tx_serial_data | Output | 1 | Transmit data | All |
| rx_serial_data | Input | 1 | Receive data | All |

## 6.4. GMII Signals

The 16-bit TX and RX GMII supports 1GbE and 2.5GbE at 62.5 MHz and 156.25 MHz respectively.

**Table 19. GMII Signals**

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| **TX GMII signals** — synchronous to tx_clkout | | | | |
| gmii16b_tx_d | Input | 16 | TX data from the MAC. The MAC sends the lower byte first followed by the upper byte. | • 2.5G<br>• 1G/2.5G<br>• 10M/100M/1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |
| gmii16b_tx_en | Input | 2 | When asserted, indicates the start of a new frame from the MAC. Bit[0] corresponds to gmii16b_tx_d[7:0]; bit[1] corresponds to gmii16b_tx_d[15:8].<br>This signal remains asserted until the PHY receives the last byte of the data frame. | |
| gmii16b_tx_err | Input | 2 | When asserted, indicates an error. Bit[0] corresponds to gmii16b_tx_err[7:0]; bit[1] corresponds to gmii16b_tx_err[15:8].<br>The bits can be asserted at any time during a frame transfer to indicate an error in the current frame. | |
| gmii16b_tx_latency | Output | 22 | The latency of the PHY excluding the PMA block on the TX datapath:<br>• Bits [21:10]: The number of clock cycles.<br>• Bits [9:0]: The fractional number of clock cycles.<br>This signal is available when only the **Enable IEEE 1588 Precision Time Protocol** parameter is selected. | • 2.5G<br>• 1G/2.5G with IEEE 1588v2 feature<br>• 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature |
| tx_clkena | Output | 1 | TX clock enable for SGMII 10M/100M operating speeds. In 1 Gbps mode, this signal is always asserted; in 100 Mbps mode, this signal is asserted once every 10 clock cycles; in 10 Mbps mode, this signal is asserted once every 100 clock cycles.<br>For 100M mode, tx_clkout is divided to 6.25 MHz.<br>For 10M mode, tx_clkout is divided to 0.625 MHz.<br>This signal is available when only the **Enable SGMII bridge** parameter is selected. | • 10M/100M/1G/2.5G<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |

*continued...*

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| **RX GMII signals** — synchronous to `rx_clkout` | | | | |
| `gmii16b_rx_d` | Output | 16 | RX data to the MAC. The PHY sends the lower byte first followed by the upper byte. Rate matching is done by the PHY on the RX data from the RX recovered clock to `rx_clkout`. | • 2.5G<br>• 1G/2.5G<br>• 10M/100M/1G/2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G(MGBASE-T) |
| `gmii16b_rx_err` | Output | 2 | When asserted, indicates an error. Bit[0] corresponds to `gmii16b_rx_err[7:0]`; bit[1] corresponds to `gmii16b_rx_err[15:8]`.<br>The bits can be asserted at any time during a frame transfer to indicate an error in the current frame. | |
| `gmii16b_rx_dv` | Output | 2 | When asserted, indicates the start of a new frame. Bit[0] corresponds to `gmii16b_rx_d[7:0]`; bit[1] corresponds to `gmii16b_rx_d[15:8]`.<br>This signal remains asserted until the PHY sends the last byte of the data frame. | |
| `gmii16b_rx_latency` | Output | 22 | The latency of the PHY excluding the PMA block on the RX datapath:<br>• Bits [21:10]: The number of clock cycles.<br>• Bits [9:0]: The fractional number of clock cycles.<br>This signal is available only when the **Enable IEEE 1588 Precision Time Protocol** parameter is selected. | • 2.5G<br>• 1G/2.5G with IEEE 1588v2 feature<br>• 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature |
| `rx_clkena` | Output | 1 | RX clock enable for SGMII 10M/100M operating speeds. In 1 Gbps mode, this signal is always asserted; in 100Mbps mode, this signal is asserted once every 10 clock cycles; in 10 Mbps mode, this signal is asserted once every 100 clock cycles.<br>For 100M mode, `rx_clkout` is divided to 6.25 MHz.<br>For 10M mode, `rx_clkout` is divided to 0.625 MHz.<br>This signal is available when only the **Enable SGMII bridge** parameter is selected. | • 10M/100M/1G/2.5G<br>• 10M/100M/1G/2.5G/10G (MGBASE-T) |

## 6.5. XGMII Signals

The XGMII supports 10GbE at 156.25 MHz.

## Table 20. XGMII Signals

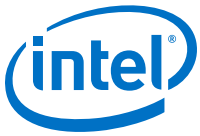
| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| **TX XGMII signals** — synchronous to `xgmii_tx_coreclkin` | | | | |
| `xgmii_tx_data` | Input | 64, 32 | TX data from the MAC. The MAC sends the data in the following order: bits [7:0], bits [15:8], bit [23:16], and so on.<br>The width is:<br>• 64 bits for 1G/2.5G/10G (MGBASE-T) configurations.<br>• 32 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations. | • 1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/10G (MGBASE-T)<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) |
| `xgmii_tx_control` | Input | 8, 4 | TX control from the MAC. The `xgmii_tx_control` bit corresponds to the `xgmii_tx_data` bits. For example, `xgmii_tx_control[0]` corresponds to `xgmii_tx_data[7:0]`, `xgmii_tx_control[1]` corresponds to `xgmii_tx_data[15:8]`, and so on.<br>The width is:<br>• 8 bits for 1G/2.5G/10G (MGBASE-T) configurations.<br>• 4 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations. | |
| `xgmii_tx_valid` | Input | 1 | Indicates valid data on `xgmii_tx_control` and `xgmii_tx_data` from the MAC.<br>Your logic/MAC must toggle the valid data as shown below: | 10M/100M/1G/2.5G/5G/10G (USXGMII) |

| Speed | Toggle Rate |
|---|---|
| 10M | Asserted once every 1000 clock cycles |
| 100M | Asserted once every 100 clock cycles |
| 1G | Asserted once every 10 clock cycles |
| 2.5G | Asserted once every 4 clock cycles |
| 5G | Asserted once every 2 clock cycles |
| 10G | Asserted on every clock cycle |

***continued...***

<table>
<tr><th>Signal Name</th><th>Direction</th><th>Width</th><th>Description</th><th>PHY Configurations</th></tr>
<tr><td>xgmii_tx_latency</td><td>Output</td><td>16, 24</td><td>The latency of the PHY excluding the PMA block on the TX datapath:<ul><li>Bits [15:10] and [23:10]: The number of clock cycles.</li><li>Bits [9:0]: The fractional number of clock cycles.</li></ul>The width is:<ul><li>16 bits for 1G/2.5G/10G (MGBASE-T) with IEEE 1588 configurations.</li><li>24 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations.</li></ul>This signal is available when only the Enable IEEE 1588 Precision Time Protocol parameter is selected.<br>Note: For USXGMII configuration, the latency value may be unstable for the first three transmitted packets times (at least 64 bytes). You should not use the latency value within this period.</td><td><ul><li>1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature</li><li>10M/100M/1G/2.5G/5G/10G (USXGMII)</li></ul></td></tr>
<tr><td colspan="5">RX XGMII signals — synchronous to xgmii_rx_coreclkin</td></tr>
<tr><td>xgmii_rx_data</td><td>Output</td><td>64, 32</td><td>RX data to the MAC. The PHY sends the data in the following order: bits [7:0], bits [15:8], bit [23:16], and so on.<br>The width is:<ul><li>64 bits for 1G/2.5G/10G (MGBASE-T) configurations.</li><li>32 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations.</li></ul></td><td rowspan="2"><ul><li>1G/2.5G/10G (MGBASE-T)</li><li>10M/100M/1G/2.5G/10G (MGBASE-T)</li><li>10M/100M/1G/2.5G/5G/10G (USXGMII)</li></ul></td></tr>
<tr><td>xgmii_rx_control</td><td>Output</td><td>8, 4</td><td>RX control to the MAC. The xgmii_rx_control bit corresponds to the xgmii_rx_data bits. For example, xgmii_rx_control[0] corresponds to xgmii_rx_data[7:0], xgmii_rx_control[1] corresponds to xgmii_rx_data[15:8], and so on.<br>The width is:<ul><li>8 bits for 1G/2.5G/10G (MGBASE-T) configurations.</li><li>4 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations.</li></ul></td></tr>
<tr><td>xgmii_rx_valid</td><td>Output</td><td>1</td><td>Indicates valid data on xgmii_rx_control and xgmii_rx_data from the MAC.<br>The toggle rate from the PHY is shown in the table below.<table><tr><th>Speed</th><th>Toggle Rate</th></tr><tr><td>10M</td><td>Asserted once every 1000 clock cycles</td></tr><tr><td>100M</td><td>Asserted once every 100 clock cycles</td></tr></table></td><td>10M/100M/1G/2.5G/5G/10G (USXGMII)</td></tr>
</table>

continued...



| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| | | | **Speed** / **Toggle Rate**<br>1G: Asserted once every 10 clock cycles<br>2.5G: Asserted once every 4 clock cycles<br>5G: Asserted once every 2 clock cycles<br>10G: Asserted on every clock cycle<br>*Note:* The toggle rate may vary when the start of a packet is received or when rate match occurs inside the PHY. You should not expect the valid data pattern to be fixed. | |
| `xgmii_rx_latency` | Output | 16, 24 | The latency of the PHY excluding the PMA block on the TX datapath:<br>• Bits [15:10]: The number of clock cycles.<br>• Bits [9:0]: The fractional number of clock cycles.<br>The width is:<br>• 16 bits for 1G/2.5G/10G (MGBASE-T) with IEEE 1588 configurations.<br>• 24 bits for 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations.<br>This signal is available when only the **Enable IEEE 1588 Precision Time Protocol** parameter is selected.<br>*Note:* For USXGMII configuration, the latency value may be unstable for the first three transmitted packets times (at least 64 bytes). You should not use the latency value within this period. | • 1G/2.5G/10G (MGBASE-T) with IEEE 1588v2 feature<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) |

## 6.6. Avalon-MM Interface Signals

The Avalon-MM interface is an Avalon-MM slave port. This interface uses word addressing and provides access to the 16-bit configuration registers of the PHY. The following signals are synchronous to `csr_clk`.

**Table 21. Avalon-MM Interface Signals**

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| `csr_address` | Input | 5, 11 | Use this bus to specify the register address to read from or write to. The width is: | All |

***continued...***

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| | | | • 5 bits for 2.5G and 1G/2.5G configurations.<br>• 11 bits for 1G/2.5G/10G (MGBASE-T) and 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations. | |
| csr_read | Input | 1 | Assert this signal to request a read operation. | |
| csr_readdata | Output | 16, 32 | Data read from the specified register. The data is valid only when the csr_waitrequest signal is deasserted. The width is:<br>• 16 bits for 2.5G and 1G/2.5G configurations.<br>• 32 bits for 1G/2.5G/10G (MGBASE-T) and 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations. The upper 16 bits are reserved. | |
| csr_write | Input | 1 | Assert this signal to request a write operation. | |
| csr_writedata | Input | 16, 32 | Data to be written to the specified register. The data is written only when the csr_waitrequest signal is deasserted. The width is:<br>• 16 bits for 2.5G and 1G/2.5G configurations.<br>• 32 bits for 1G/2.5G/10G (MGBASE-T) and 10M/100M/1G/2.5G/5G/10G (USXGMII) configurations. The upper 16 bits are reserved. | |
| csr_waitrequest | Output | 1 | When asserted, indicates that the PHY is busy and not ready to accept any read or write requests.<br>• When you have requested for a read or write, keep the control signals to the Avalon-MM interface constant while this signal is asserted. The request is complete when it is deasserted.<br>• This signal can be high or low during idle cycles and reset. Therefore, the user application must not make any assumption of its assertion state during these periods. | |

## 6.7. Transceiver Status and Reconfiguration Signals

### Table 22. Transceiver Status and Reconfiguration Signals

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| rx_is_lockedtodata | Output | 1 | Asserted when the CDR is locked to the RX data. | All |
| tx_cal_busy | Output | 1 | Asserted when TX calibration is in progress. | |

continued...

| Signal Name | Direction | Width | Description | PHY Configurations |
|---|---|---|---|---|
| rx_cal_busy | Output | 1 | Asserted when RX calibration is in progress. | |
| **Transceiver reconfiguration signals** | | | | |
| reconfig_clk | Input | 1 | Reconfiguration signals connected to the reconfiguration block. The reconfig_clk signal provides the timing reference for this interface. | All |
| reconfig_reset | Input | 1 | | |
| reconfig_address | Input | 11 | | |
| reconfig_write | Input | 1 | | |
| reconfig_read | Input | 1 | | |
| reconfig_writedata | Input | 32 | | |
| reconfig_readdata | Output | 32 | | |
| reconfig_waitrequest | Output | 1 | | |

**Related Information**

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

## 6.8. Status Signals

### Table 23. Status Signals

| Signal Name | Direction | Clock Domain | Width | Description | PHY Configurations |
|---|---|---|---|---|---|
| led_char_err | Output | Synchronous to rx_clkout | 1 | Asserted when a 10-bit character error is detected in the RX data. This signal is not applicable for 10GbE. | • 2.5G<br>• 1G/2.5G<br>• 10M/ 100M/1G/ 2.5G<br>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/ 100M/1G/ 2.5G/10G (MGBASE-T) |
| led_link | Output | Synchronous to tx_clkout | 1 | Asserted when the link synchronization for 1GbE or 2.5GbE is successful. This signal is not applicable for 10GbE. | |
| led_disp_err | Output | Synchronous to rx_clkout | 1 | Asserted when a 10-bit running disparity error is detected in the RX data. A running disparity error indicates that more than the previous and perhaps the current received group had an error. This signal is not applicable for 10GbE. | |
| led_an | Output | Synchronous to rx_clkout | 1 | Asserted when auto-negotiation is completed. This signal is not applicable for 10GbE. | All |
| led_panel_link | Output | Synchronous to rx_clkout | 1 | When asserted, this signal indicates the following behavior:<br>**Mode**: 1000 Base-X without Auto-negotiation — **Behavior**: When asserted, indicates successful link synchronization. | • 10M/ 100M/1G/ 2.5G<br>• 10M/ 100M/1G/ 2.5G/10G (MGBASE-T) |

***continued...***

<table>
<tr><th>Signal Name</th><th>Direction</th><th>Clock Domain</th><th>Width</th><th>Description</th><th>PHY Configurations</th></tr>
<tr><td></td><td></td><td></td><td></td><td><table><tr><th>Mode</th><th>Behavior</th></tr><tr><td>SGMII mode without Auto-negotiation</td><td>When asserted, indicates successful link synchronization.</td></tr><tr><td>1000 Base-X with Auto-negotiation</td><td>Clause 37 Auto-negotiation status. The PCS function asserts this signal when auto-negotiation completes.</td></tr><tr><td>SGMII mode with MAC mode Auto-negotiation</td><td>Clause 37 Auto-negotiation status. The PCS function asserts this signal when auto-negotiation completes.</td></tr></table>This signal is applicable only when SGMII 10M/100M mode is enabled.</td><td></td></tr>
<tr><td>rx_block_lock</td><td>Output</td><td>Synchronous to rx_clkout</td><td>1</td><td>Asserted when the link synchronization for 10GbE of MGBASE-T and all speeds of USXGMII is successful.</td><td>• 1G/2.5G/10G (MGBASE-T)<br>• 10M/ 100M/1G/ 2.5G/10G (MGBASE-T)<br>• 10M/ 100M/1G/ 2.5G/5G/10G (USXGMII)</td></tr>
</table>

The latency indicators are connected from PHY to MAC block, where the MAC block uses them to calculate timestamp of the transmitted or received packets. For more information, refer to *Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide*.

### Related Information

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide

# 7. 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide

If an IP core version is not listed, the user guide for the previous IP core version applies.

| IP Core Version | User Guide |
|---|---|
| 17.1 | Intel Stratix 10 1G/ 2.5G/5G/10G Multi-rate Ethernet PHY IP Core User Guide |

# A. Document Revision History for the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide

| Document Version | Intel Quartus Prime Version | Changes |
|---|---|---|
| 2018.09.24 | 18.0 | • Updated the note in *About the 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core* topic.<br>• Updated Table: *Status Signals* to include a Clock Domain column.<br>• Updated the *Functional Description* topic.<br>• Updated the *Timing Constraints* topic.<br>• Updated Table: *XGMII Signals*:<br>— Corrected the direction of `xgmii_tx_valid`.<br>— Updated the toggle rate of 10G speed for `xgmii_tx_valid` and `xgmii_rx_valid`.<br>• Renamed topic title *Register Access* to *Register Definitions*.<br>• Made minor editorial edits. |
| 2018.05.07 | 18.0 | • Renamed the document as *1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide*.<br>• Renamed "1G/2.5G/5G/10G Multi-rate Ethernet PHY" IP core to "1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP" as per Intel rebranding.<br>• Added support for the following variants:<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII)<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII) with IEEE 1588v2<br>• Updated topic title *Datasheet* to *About 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP*.<br>• Updated the *About 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP* topic.<br>• Updated Table: *1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core Features*.<br>• Updated Table: *Resource Utilization*:<br>— Updated the resource utilization for all configurations.<br>— Added resource utilization information for 10M/100M/1G/2.5G/5G/10G (USXGMII) with IEEE 1588v2 configuration.<br>• Removed a note from the *Specifying the IP Core Parameters and Options* topic.<br>• Updated Table: *Slowest Supported Device Speed Grades* with supported speed grade for 10M/100M/1G/2.5G/5G/10G (USXGMII) with 1588 feature.<br>• Updated Figure: *IP Parameter Editor*.<br>• Updated Table: *1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP Core Parameters*:<br>— Updated descriptions for **Connect to MGBASE-T PHY**, **Connect to NBASE-T PHY**, **Enable IEEE 1588 Precision Time Protocol**, **PHY ID (32 bit)**, and **Reference clock frequency for 10 GbE (MHz)** parameters.<br>— Updated options for **Speed** parameter.<br>• Updated the *Functional Description* topic. |

***continued...***

| Document Version | Intel Quartus Prime Version | Changes |
|---|---|---|
| | | • Updated the *Clocking and Reset Sequence* topic.<br>• Updated Table: *Timing Constraints* to include 10M/100M/1G/2.5G and 10M/100M/1G/2.5G/10G (SGMII/MGBASE-T) configurations.<br>• Renamed topic title *Register Definitions* to *Register Access*.<br>• Updated Table: *PHY Registers Definition*:<br>— Updated the description for Bit [4:2]: USXGMII_SPEED of the `usxgmii_control` signal.<br>— Updated the description for `link_timer` signal.<br>• Updated Figure: *Interface Signals*.<br>• Updated Tables: *Clock and Reset Signals*, *GMII Signals*, and *XGMII Signals*.<br>• Updated for latest Intel branding standards.<br>• Made editorial updates throughout the document. |

| Date | Version | Changes |
|---|---|---|
| November 2017 | 2017.11.06 | • Changed the document title from *Intel Stratix 10 Multi-rate Ethernet PHY IP Core User Guide* to *Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core User Guide*.<br>• Added support for the 1G/2.5G/5G/10G (USXGMII) variant.<br>• Added new Table: *Slowest Supported Device Speed Grades* to include speed grade support.<br>• Added resource utilization for 1G/2.5G/5G/10G (USXGMII) configuration.<br>• Added new chapter *Getting Started* explaining how to install, generate and integrate IP core in your design.<br>• Added information in *Clocking and Reset Sequence* to confirm that the Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP core can handle clock frequency difference up to ±100 ppm.<br>• Added the PHY configuration information in *Interface Signals* section. |
| June 2017 | 2017.06.05 | • Added the SGMII (10M/100M/1G) support for 1G/2.5G and 1G/2.5/10G (MGBASE-T).<br>• Added resource utilization for 1G/2.5G with IEEE 1588v2 enabled, 10M/100M/1G/2.5G, and 10M/100M/1G/2.5G/10G configurations.<br>• Added the **Enable SGMII bridge** parameter and removed the **Enable ODI acceleration logic** parameter in the *Table: 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core Parameters*.<br>• Updated the *Table: Supported Operating Speed* with SGMII mode information.<br>• Added registers for SGMII mode (see address 0x05 (SGMII mode) and 0x14).<br>• Added the following signals:<br>— `tx_clkena` and `rx_clkena` in *Table: GMII Signals*.<br>— `led_panel_link` in *Table: Status Signals*. |
| May 2017 | 2017.05.08 | Initial release. |