

## MOSFET

### 950V CoolMOS™ P7 SJ Power Device

The latest 950V CoolMOS™ P7 series sets a new benchmark in 950V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

#### Features

- Best-in-class FOM  $R_{DS(on)} * E_{oss}$ ; reduced  $Q_g$ ,  $C_{iss}$ , and  $C_{oss}$
- Best-in-class  $V_{GS(th)}$  of 3V and smallest  $V_{GS(th)}$  variation of  $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Best-in-class CoolMOS™ quality and reliability
- Fully optimized portfolio

#### Benefits

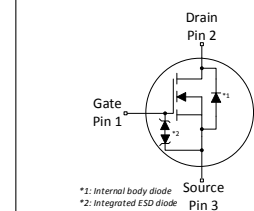
- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

#### Potential applications

Recommended for flyback topologies for LED Lighting, low power Chargers and Adapters, Smart Meter, AUX power and Industrial power. Also suitable for PFC stage in Consumer and Solar applications.

**Product Validation:** Fully qualified acc. JEDEC for Industrial Applications

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J=25^\circ C$	950	V
$R_{DS(on),max}$	0.75	$\Omega$
$Q_{g,typ}$	23	nC
$I_D$	9	A
$E_{oss} @ 500V$	1.9	$\mu J$
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPA95R750P7	PG-TO 220 FullPAK	95R750P7	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	9 5.5	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	27	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	18	mJ	$I_D=1.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.22	mJ	$I_D=1.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Application (Flyback) relevant avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	4.0	-	A	measured with standard leakage inductance of transformer of $10\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{Hz}$ )
Power dissipation	$P_{tot}$	-	-	28	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	3.8	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	27	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>4)</sup>	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 2.2\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	50	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 2.2\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.5$ ; IPAK equivalent.

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> For further explanation please read AN - CoolMOS™ 700V P7 & 950V P7

<sup>4)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.4	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	-
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	950	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	$V_{DS}=V_{GS}, I_D=0.22mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=950V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=950V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	1000	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.64 1.429	0.75	$\Omega$	$V_{GS}=10V, I_D=4.5A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=4.5A, T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	1	-	$\Omega$	$f=250\text{kHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	712	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	11	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	18	-	pF	$V_{GS}=0V, V_{DS}=0\dots400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	182	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots400V$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.5A,$ $R_G=10.2\Omega$ ; see table 9
Rise time	$t_r$	-	7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.5A,$ $R_G=10.2\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	46	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.5A,$ $R_G=10.2\Omega$ ; see table 9
Fall time	$t_f$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.5A,$ $R_G=10.2\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	3	-	nC	$V_{DD}=760V, I_D=4.5A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	7	-	nC	$V_{DD}=760V, I_D=4.5A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	23	-	nC	$V_{DD}=760V, I_D=4.5A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=760V, I_D=4.5A, V_{GS}=0$ to 10V

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=4.5A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	684	-	ns	$V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	5	-	$\mu C$	$V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	12	-	A	$V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

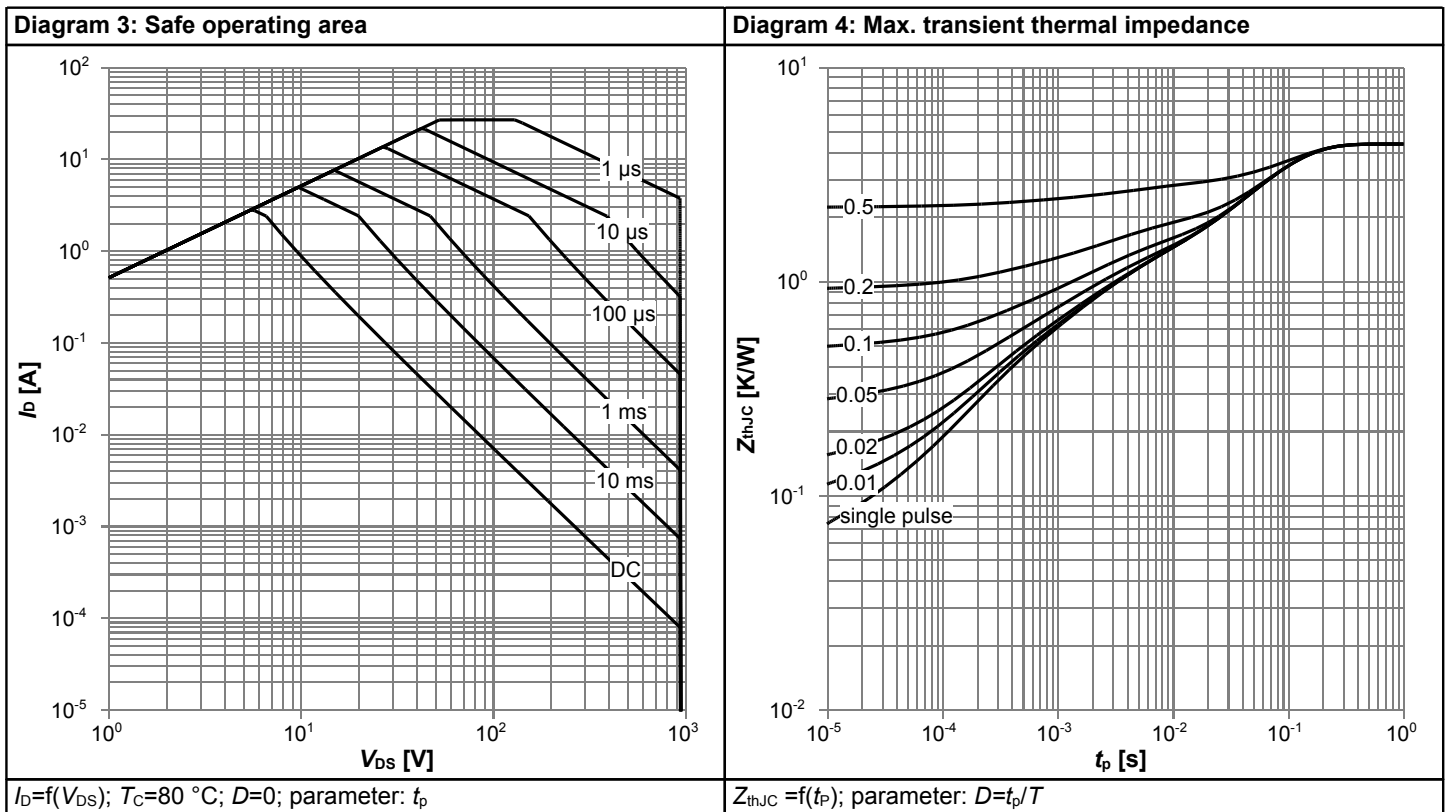
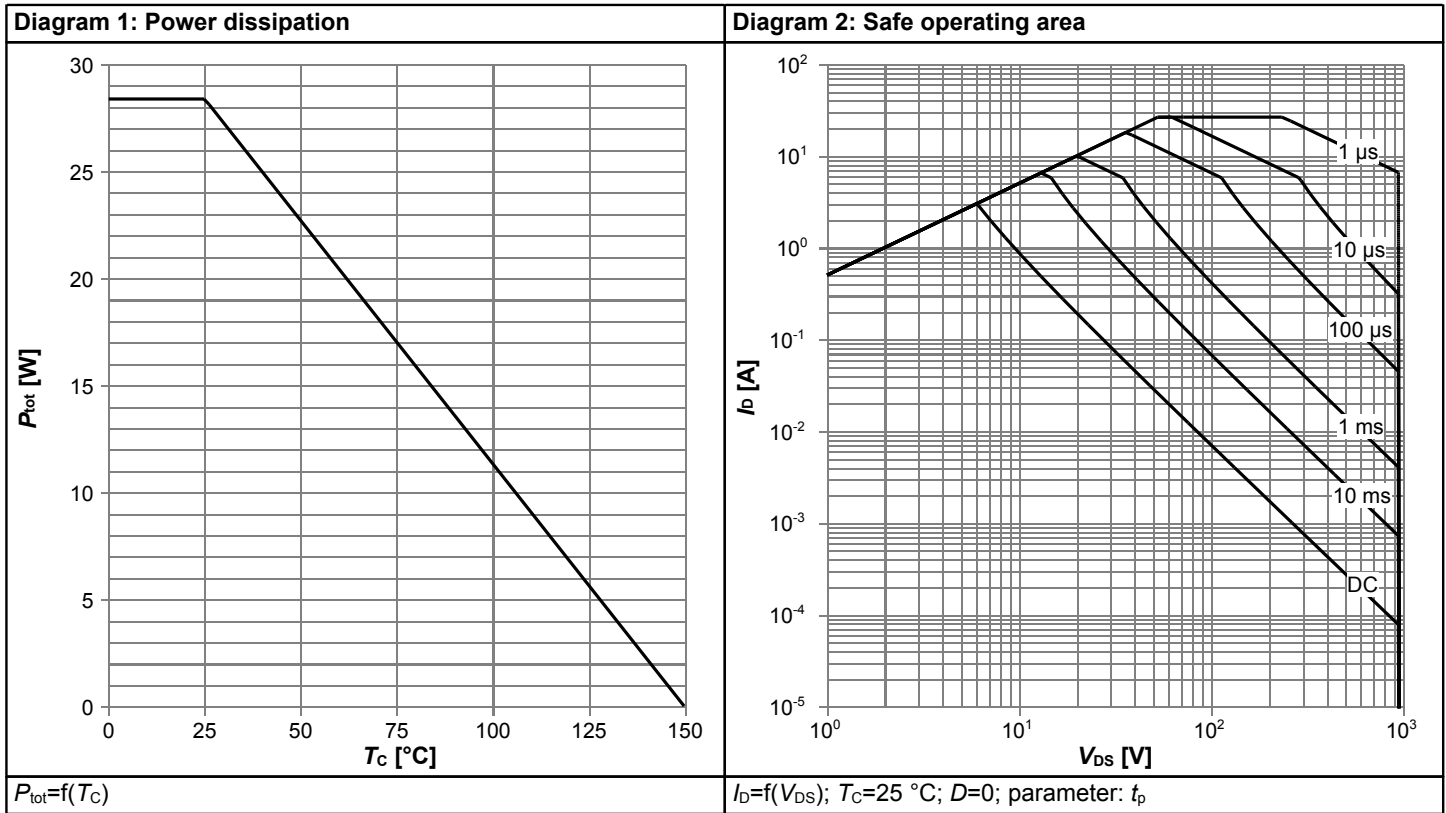
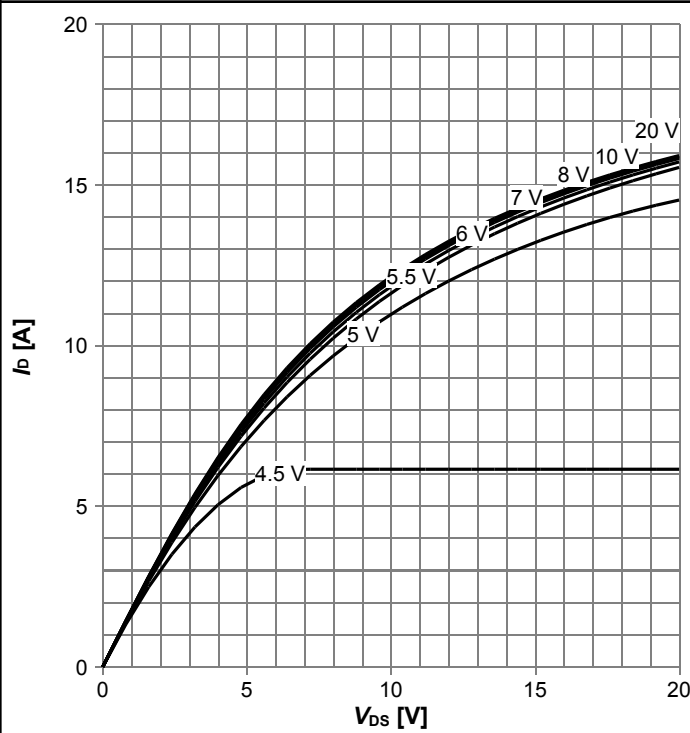
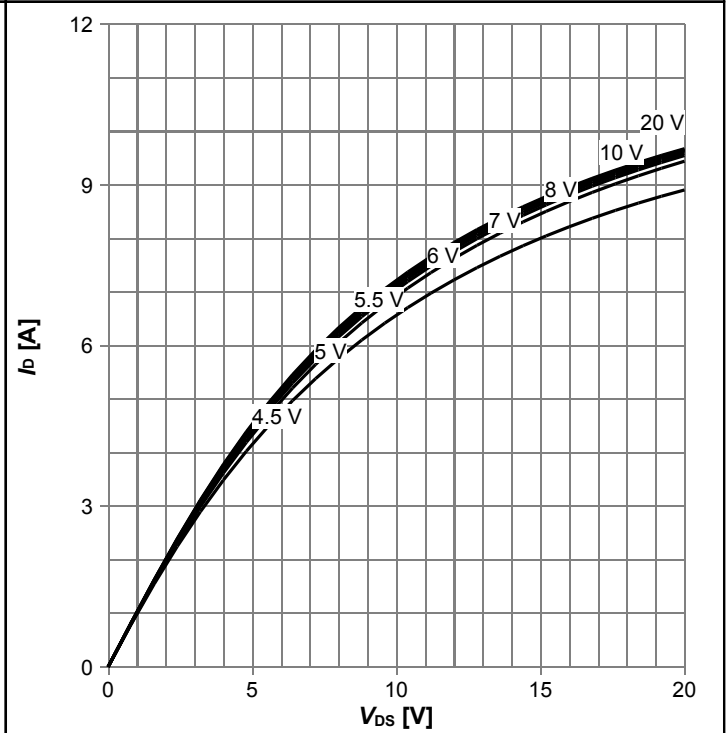


Diagram 5: Typ. output characteristics



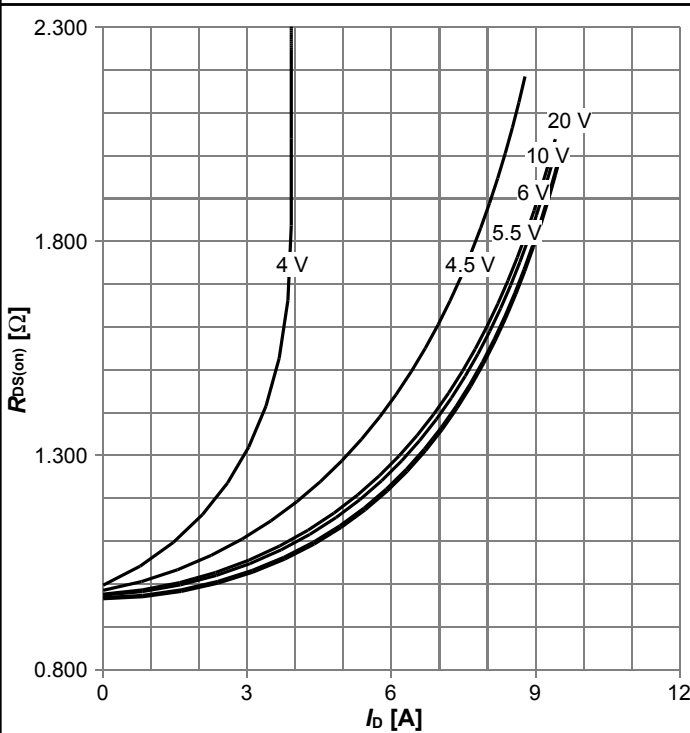
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



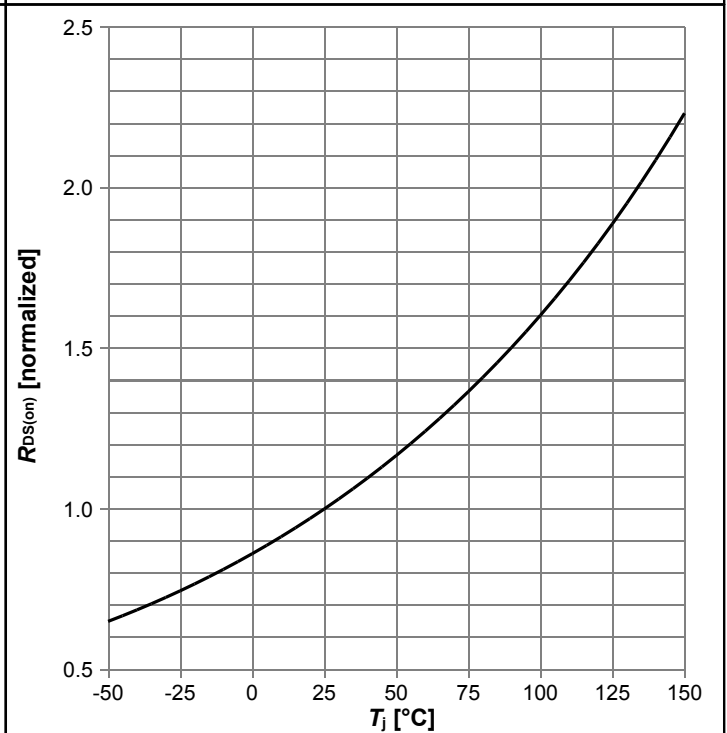
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

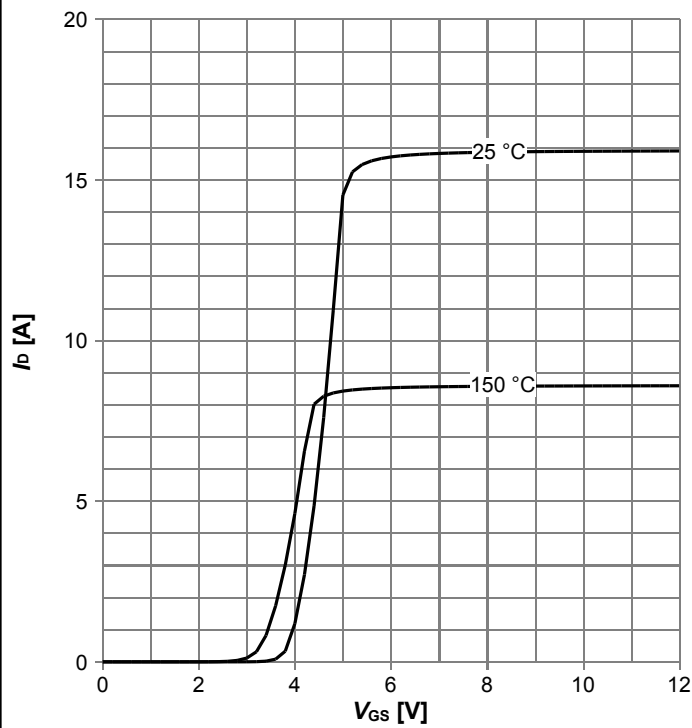
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$ ;  $I_D=4.5\text{ A}$ ;  $V_{GS}=10\text{ V}$

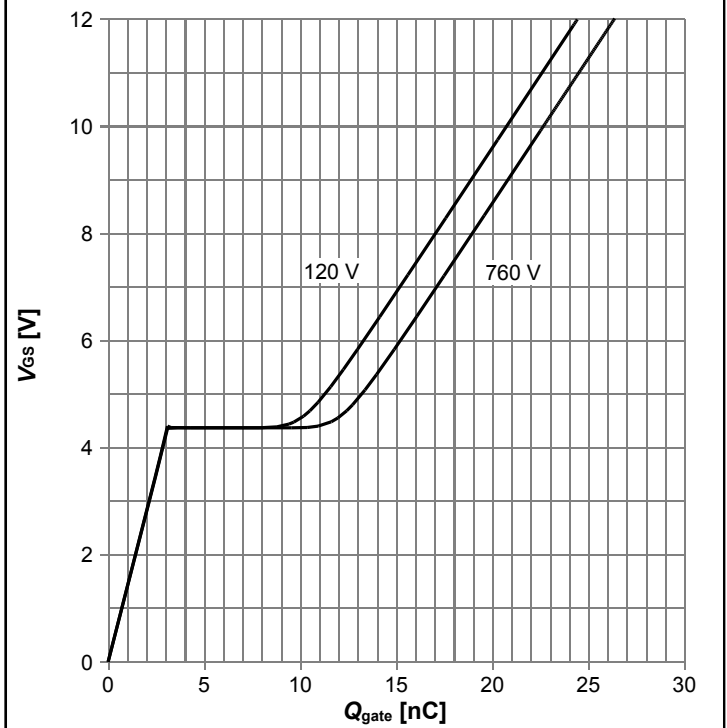


Diagram 9: Typ. transfer characteristics



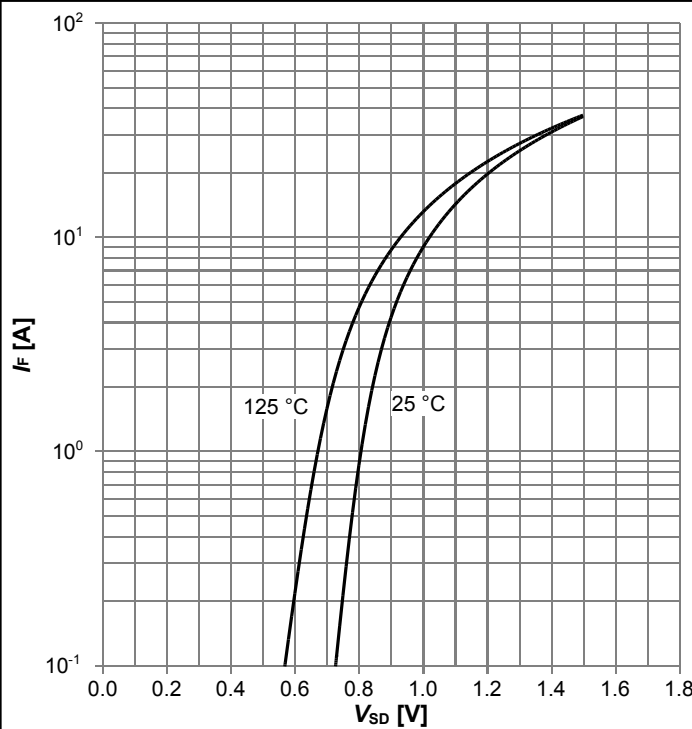
$I_D=f(V_{GS}); V_{DS}=20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



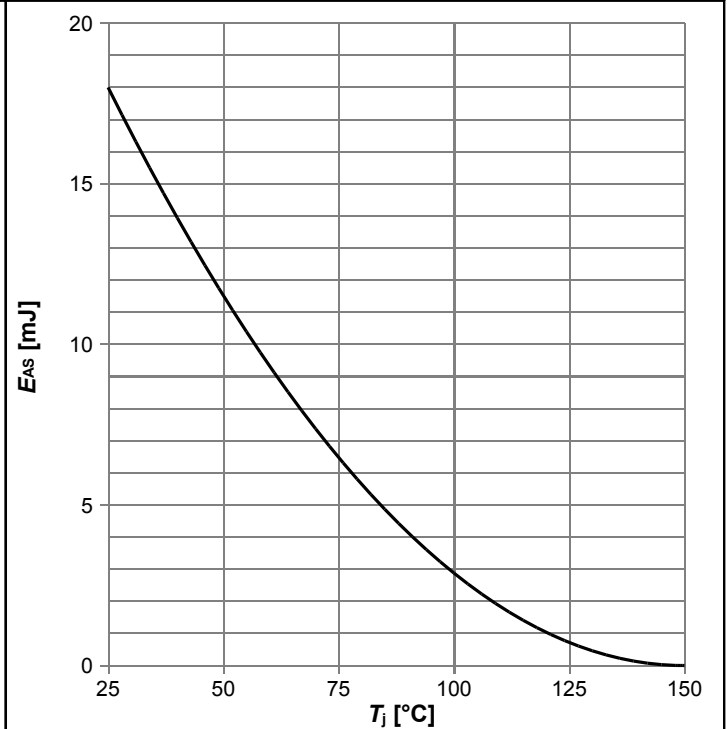
$V_{GS}=f(Q_{gate}); I_D=4.5 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



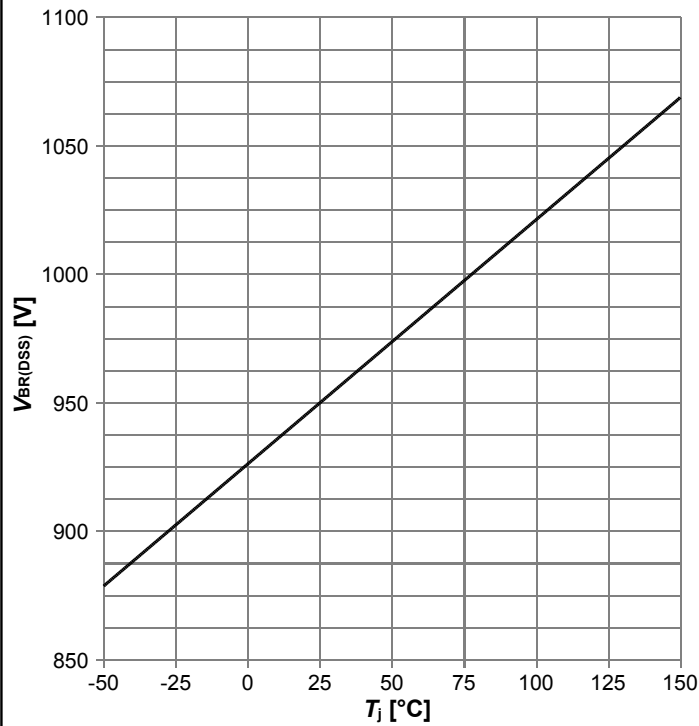
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy



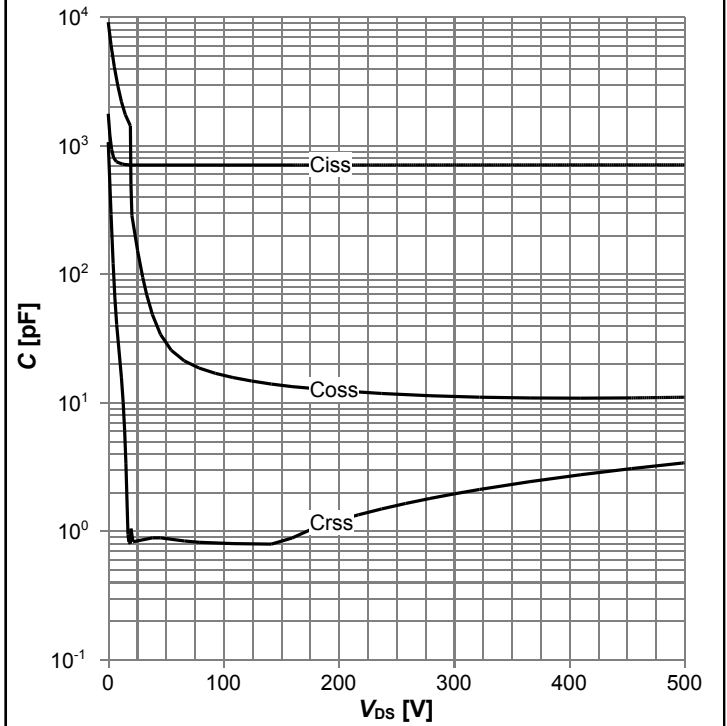
$E_{AS}=f(T_j); I_D=1.1 A; V_{DD}=50 V$

**Diagram 13: Drain-source breakdown voltage**



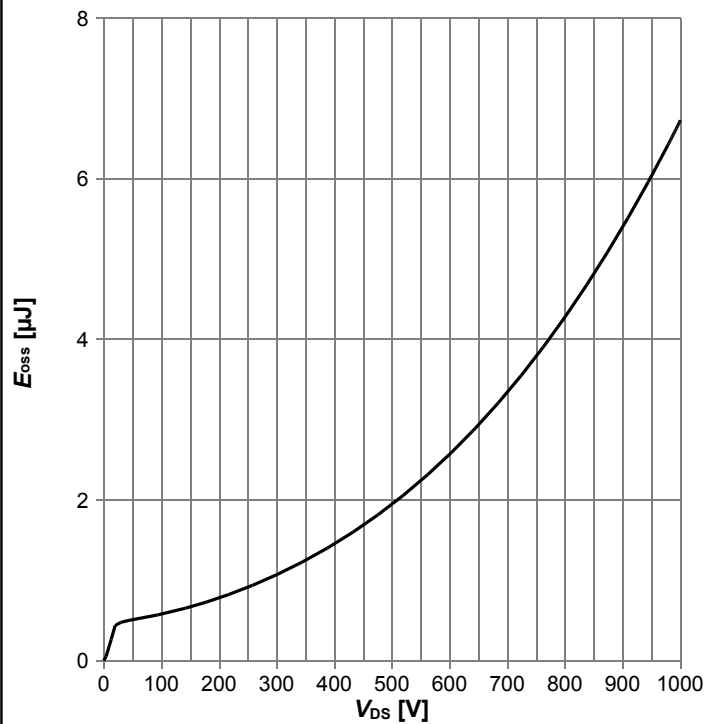
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

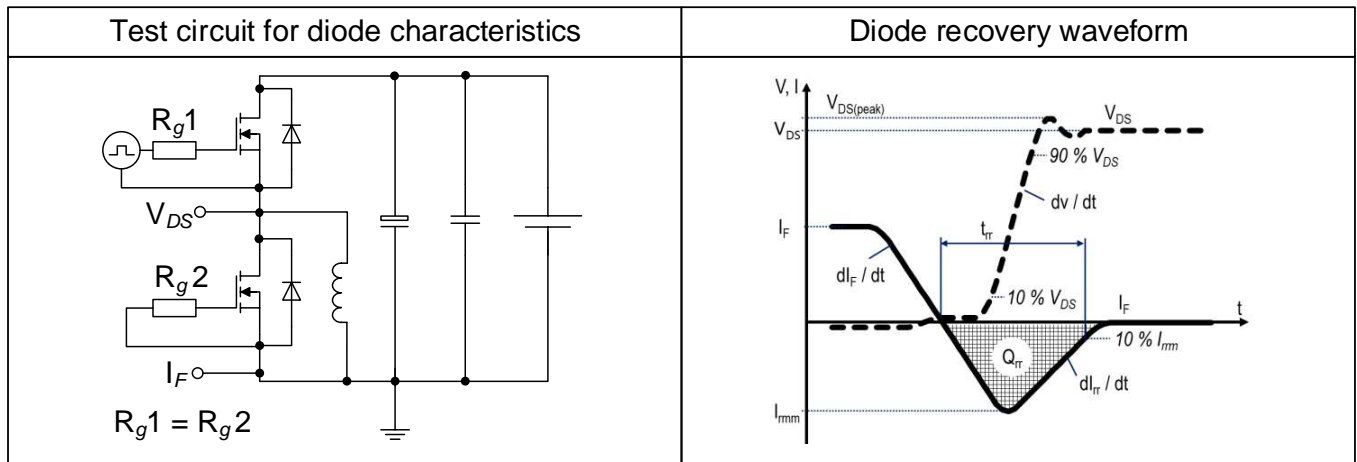
**Diagram 15: Typ. Coss stored energy**



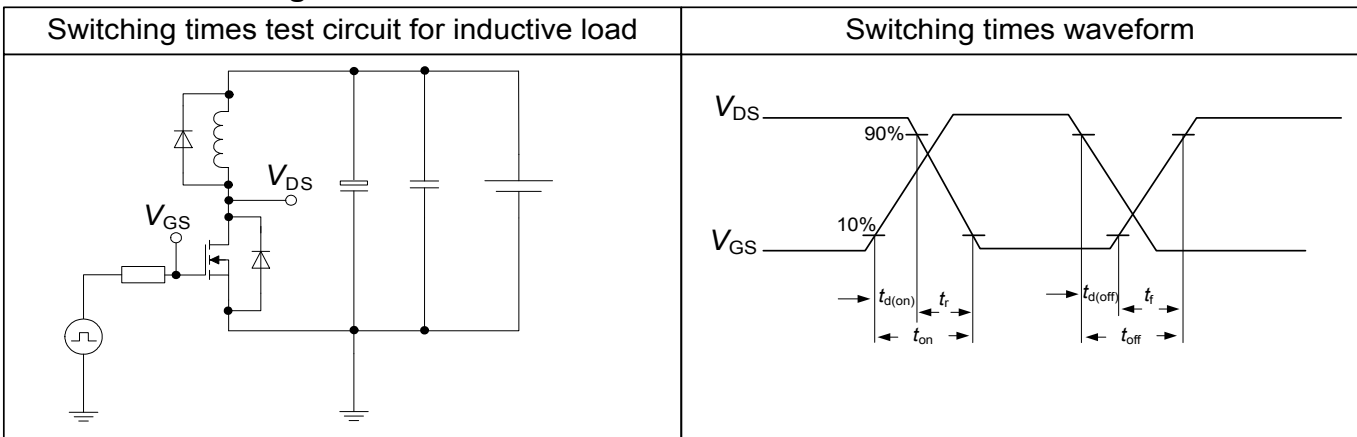
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

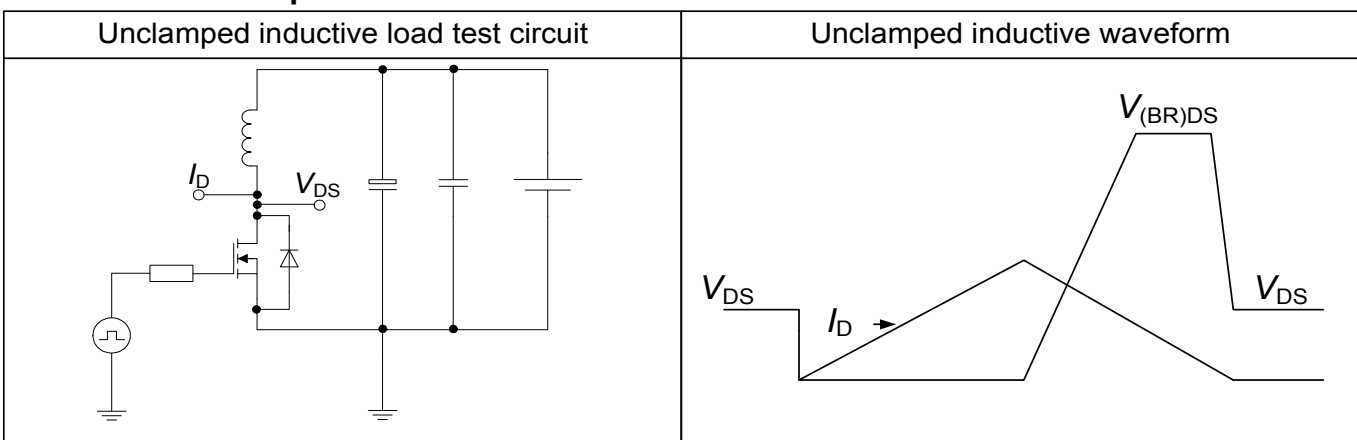
**Table 8 Diode characteristics**



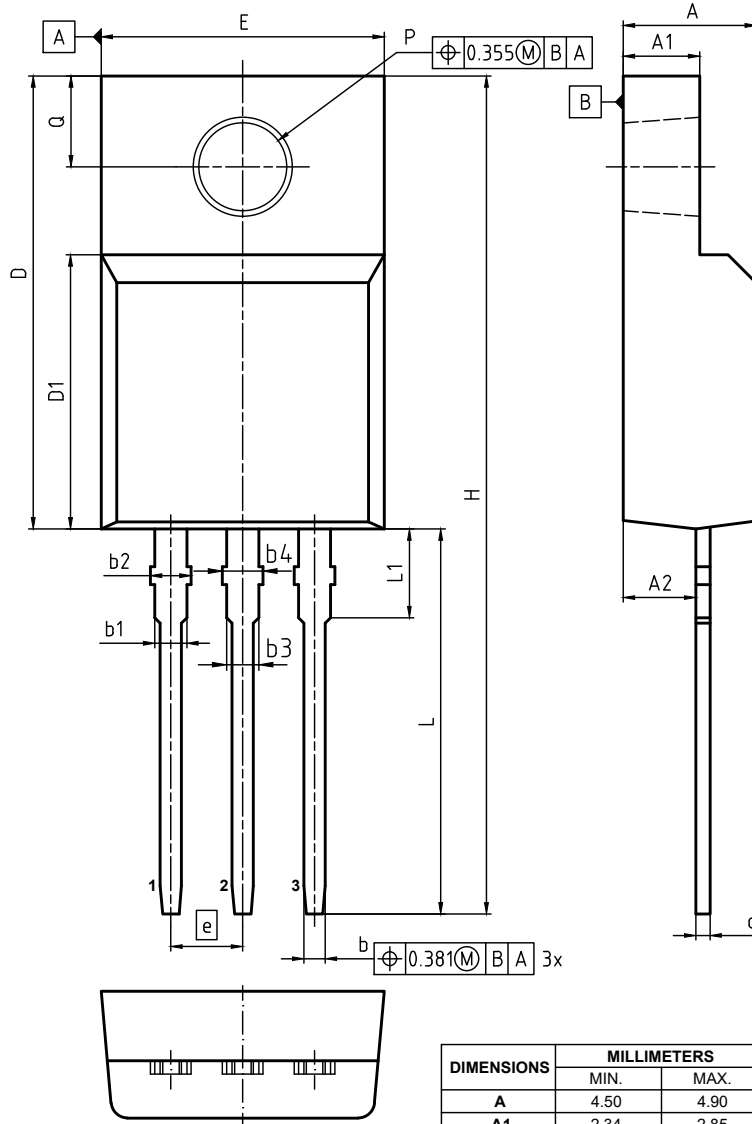
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



NOTES:  
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS  
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
$\phi P$	3.00	3.30
Q	3.15	3.50

DOCUMENT NO. Z8B00003319
REVISION 09
ISSUE DATE 23.07.2018
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION 

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS P7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS P7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS P7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA95R750P7

**Revision: 2018-07-24, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-05-30	Release of final version
2.1	2018-06-04	Final
2.2	2018-07-24	Corrected package drawing text

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### Published by

**Infineon Technologies AG**

**81726 München, Germany**

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