NXP Semiconductors
Advance Information

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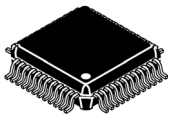
Power system basis chip with high speed can transceiver

FS6407
FS6408

POWER SYSTEM BASIS CHIP



AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

The FS6407/FS6408 SMARTMOS devices area multi-output, power supply, integrated circuit, including HSCAN transceiver, dedicated to the industrial market.

Multiple switching and linear voltage regulators, including low-power mode (32 μA) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over wide input voltages (down to 2.7 V) and wide output current ranges (up to 1.5 A).

The FS6407/FS6408 include enhanced safety features, with multiple fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level.

The built-in enhanced high-speed CAN interface fulfills the ISO11898-2 and -5 standards.

Features

- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.2 V to 3.3 V delivering up to 1.5 A
- Multiple wake-up sources in low-power mode: CAN and/or IOs
- Six configurable I/Os
- Linear voltage regulator dedicated to auxiliary functions, or to a sensor supply (V_{CCA} tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (V_{CCA}), 5.0 V or 3.3 V

Applications

- Automation (PLC, robotics)
- Building control (lift)
- Transportation (mobile machine, military)
- Medical (Infusion pump, stairs)

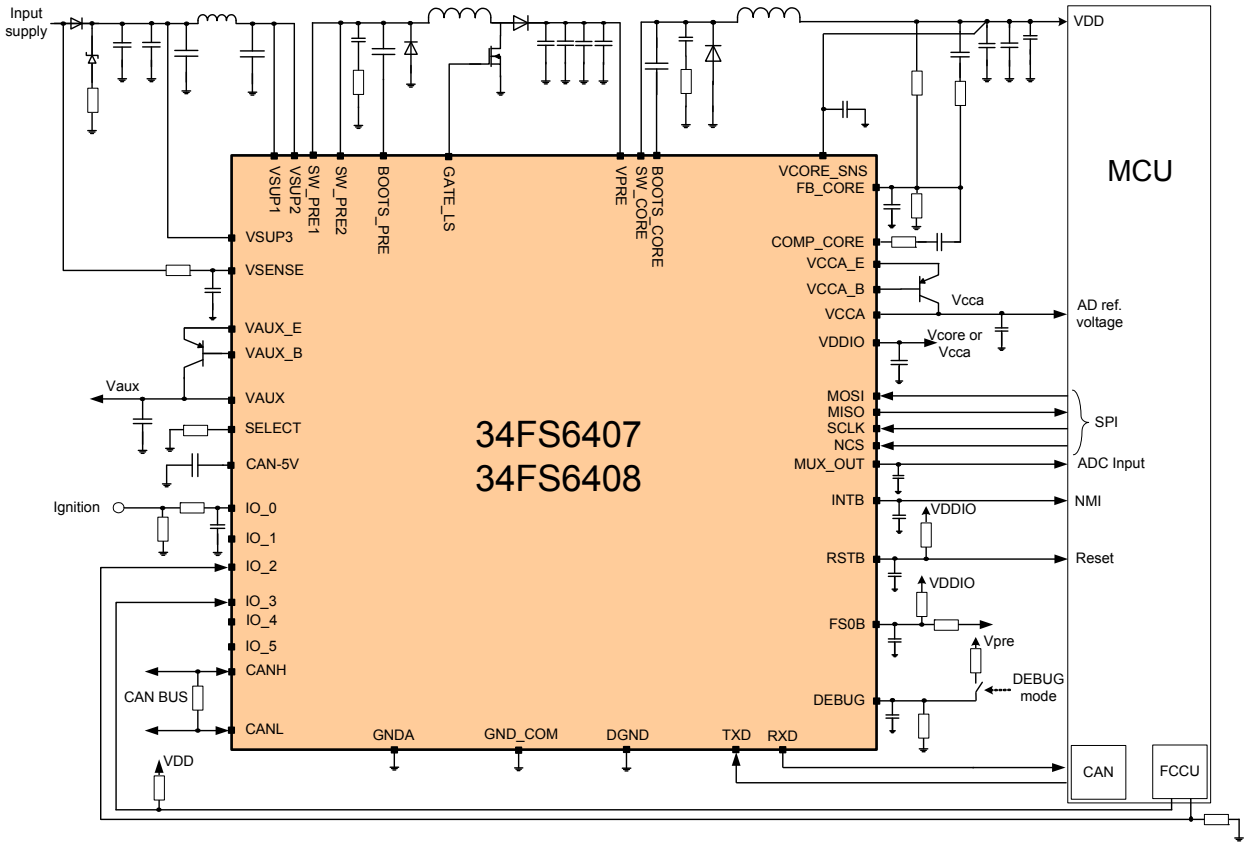


Figure 1. FS6407/FS6408 simplified application diagram - buck boost configuration

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

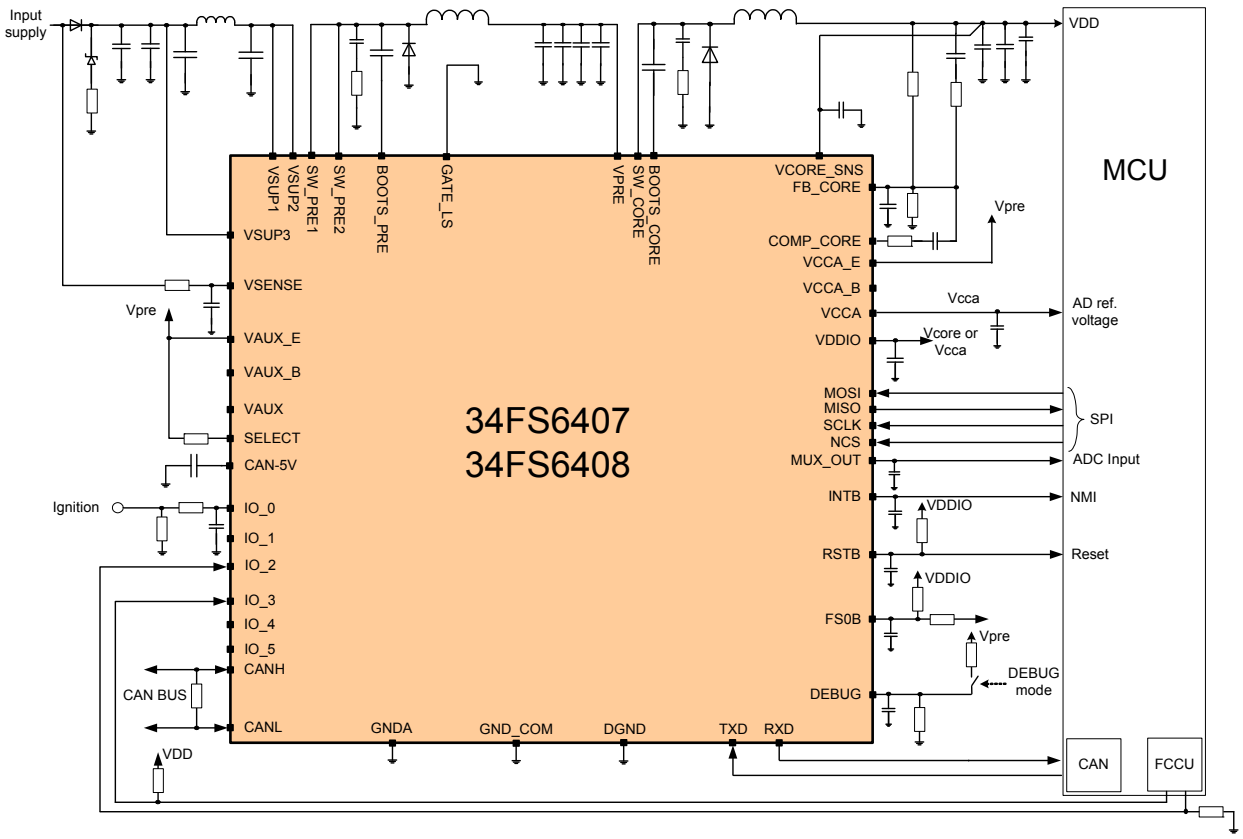


Figure 2. Simplified application diagram - buck configuration, V_{AUX} not used, V_{CCA} = 100 mA

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	CAN	Vcore	Notes
MC34FS6407NAE	-40 °C to 125 °C	48-pin LQFP exposed pad	1	0.8 A	(1)
MC34FS6408NAE				1.5 A	

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

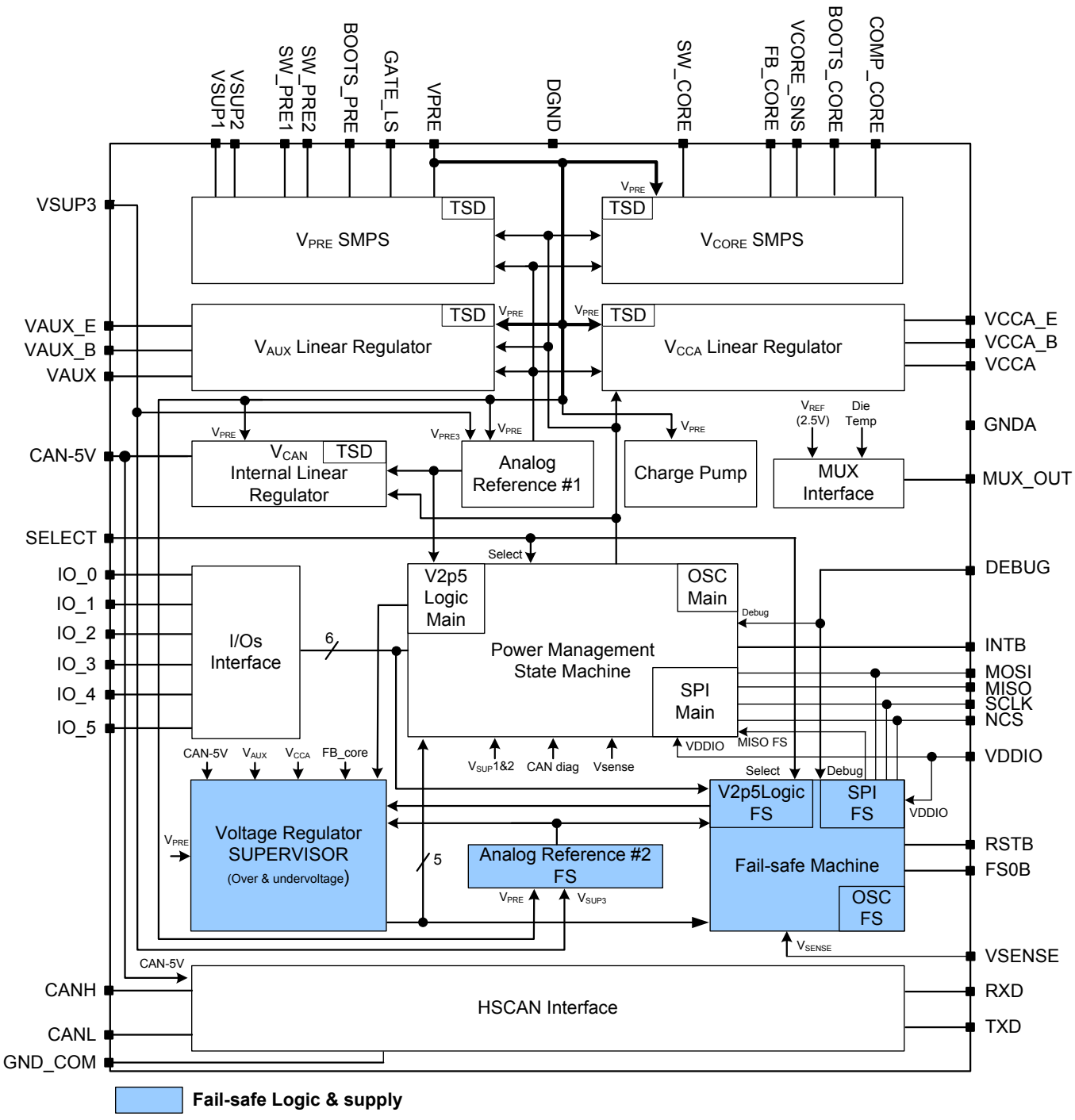


Figure 3. FS6407/FS6408 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram for FS6407/FS6408

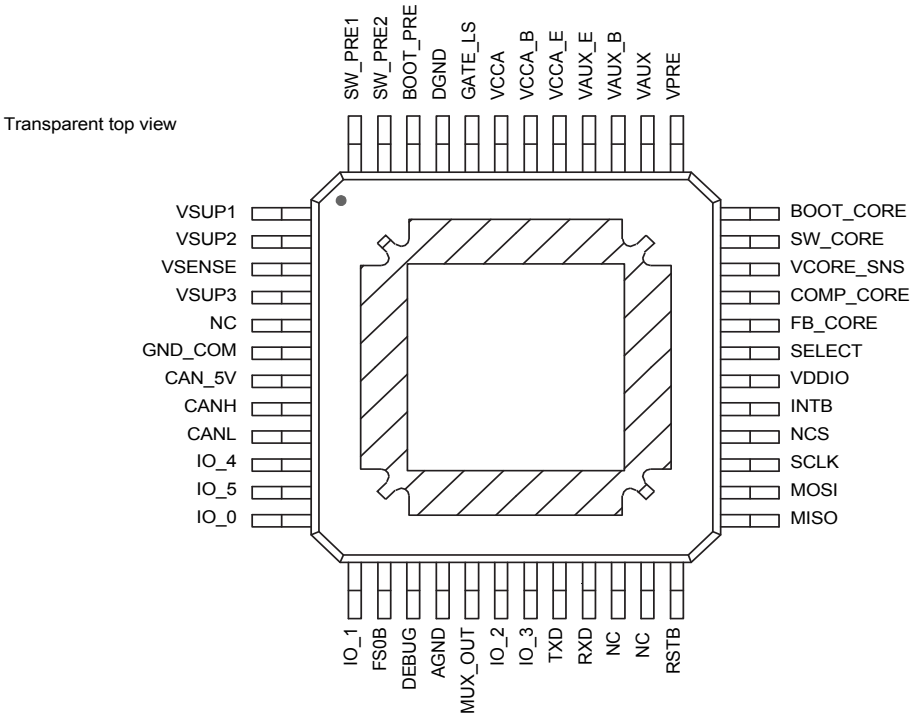


Figure 4. FS6407/FS6408 pinout

3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on page 22.

Table 2. FS6407/FS6408 pin definition

Pin Number	Pin Name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5, 22, 23	NC	N/A	Not connected. Pins must be left open.
6	GND_COM	GND	Dedicated ground for CAN
7	CAN_5V	A_OUT	Output voltage for the embedded CAN interface
8	CANH	A_IN/OUT	HSCAN output High
9	CANL	A_IN/OUT	HSCAN output Low

Table 2. FS6407/FS6408 pin definition (continued)

Pin Number	Pin Name	Type	Definition
10 11	IO_4:5	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Output gate driver:** Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
12 13	IO_0:1	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output pin **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Rk:** For safety purposes, IO_1 can also be used to monitor the middle point of a redundant resistor bridge connected on V_{CORE} (in parallel to the one used to set the Vcore voltage).
14	FS0B	D_OUT	Output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to an MCU ADC input. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital INPUT**: Pin status can be read through the SPI. Can be used to monitor error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the HSCAN bus. Internal pull-up to VDDIO. Internal pull-up to VDDIO.
21	RXD	D_OUT	Receiver output which reports the state of the HSCAN bus to the MCU
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master Input Slave Output
26	MOSI	D_IN	SPI bus. Master Output Slave Input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	No Chip Select (Active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_IN	Compensation network. Output of the error amplifier.
34	VCORE_SNS	A_IN	VCORE output voltage sense
35	SW_CORE	A_IN	VCORE switching point
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive
37	VPRE	A_OUT	VPRE output voltage
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection

Table 2. FS6407/FS6408 pin definition (continued)

Pin Number	Pin Name	Type	Definition
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for “Non-inverting Buck-boost” configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_IN	Second pre-regulator switching point
48	SW_PRE1	A_IN	First pre-regulator switching point

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP1/2/3}$	DC Voltage at Power Supply Pins	-1.0 to 40	V	(2)
V_{SENSE}	DC Voltage at Battery Sense Pin	-14 to 40	V	
$V_{SW1,2}$	DC Voltage at SW_PRE1 and SW_PRE2 Pins	-1.0 to 40	V	
V_{PRE}	DC Voltage at VPRE Pin	-0.3 to 8	V	
V_{GATE_LS}	DC Voltage at Gate_LS pin	-0.3 to 8	V	
V_{BOOT_PRE}	DC Voltage at BOOT_PRE pin	-1.0 to 50	V	
V_{SW_CORE}	DC Voltage at SW_CORE pin	-1.0 to 8.0	V	
V_{CORE_SNS}	DC Voltage at VCORE_SNS pin	0.0 to 8.0	V	
V_{BOOT_CORE}	DC Voltage at BOOT_CORE pin	0.0 to 15	V	
V_{FB_CORE}	DC Voltage at FB_CORE pin	-0.3 to 2.5	V	
V_{COMP_CORE}	DC Voltage at COMP_CORE pin	-0.3 to 2.5	V	
$V_{AUX\_E,B}$	DC Voltage at VAUX_E, VAUX_B pin	-0.3 to 40	V	
V_{AUX}	DC Voltage at VAUX pin	-2.0 to 40	V	
$V_{CCA\_B,E}$	DC Voltage at VCCA_B, VCCA_E pin	-0.3 to 8.0	V	
V_{CCA}	DC Voltage at VCCA pin	-0.3 to 8.0	V	
V_{DDIO}	DC Voltage at VDDIO	-0.3 to 8.0	V	
V_{FS0}	DC Voltage at FS0B (with ext R mandatory)	-0.3 to 40	V	
V_{DEBUG}	DC Voltage at DEBUG	-0.3 to 40	V	
$V_{IO\_0,1,4,5}$	DC Voltage at IO_0:1; 4:5 (with ext R = 5.1 kΩ in series mandatory)	-0.3 to 40	V	
V_{DIG}	DC Voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3	-0.3 to V_{DDIO}+0.3	V	
V_{SELECT}	DC Voltage at SELECT	-0.3 to 8.0	V	
V_{BUS_CAN}	DC Voltage on CANL, CANH	-27 to 40	V	
V_{CAN_5V}	DC Voltage on CAN_5 V	-0.3 to 8.0	V	
$I\_IO_{0,\ 1,\ 4,\ 5}$	IOs Maximum Current Capability(IO_0, IO_1, IO_4, IO_5)	-5.0 to 5.0	mA	

Notes

2. All V_{SUPS} ($V_{SUP1/2/3}$) must be connected to the same supply (Figure 49)

Table 3. Maximum ratings (continued)

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
	ESD Voltage			
	Human Body Model (JESD22/A114) - 100 pF, 1.5 kΩ			
$V_{ESD-HBM1}$	• All pins (ESD Class 2)	±2.0	kV	
$V_{ESD-HBM2}$	• VSUP1,VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5,FS0B, DEBUG (ESD Class 3A)	±4.0	kV	
$V_{ESD-HBM3}$	• CANH, CANL (ESD Class 3A)	±6.0	kV	
	Charge Device Model (JESD22/C101):			
$V_{ESD-CDM1}$	• All Pins (ESD Class 2)	±500	V	
$V_{ESD-CDM2}$	• Corner Pins (ESD Class 2)	±750	V	
	System level ESD (Gun Test)			(3)
	• VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B			
$V_{ESD-GUN1}$	330 Ω / 150 pF Unpowered According to IEC61000-4-2:	±8.0	kV	
$V_{ESD-GUN2}$	330 Ω / 150 pF Unpowered According to OEM CAN, FLexray Conformance	±8.0	kV	
$V_{ESD-GUN3}$	2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	±8.0	kV	
$V_{ESD-GUN4}$	2.0 kΩ / 330 pF Powered According to ISO10605.2008	±8.0	kV	
	• CANH, CANL			
$V_{ESD-GUN5}$	330 Ω / 150 pF Unpowered According to IEC61000-4-2:	±15.0	kV	
$V_{ESD-GUN6}$	330 Ω / 150 pF Unpowered According to OEM CAN, FLexray Conformance	±12.0	kV	
$V_{ESD-GUN7}$	2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	±15.0	kV	
$V_{ESD-GUN8}$	2.0 kΩ / 330 pF Powered According to ISO10605.2008	±15.0	kV	
Thermal ratings				
T_A	Ambient Temperature	-40 to 125	°C	
T_J	Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	30	°C/W	(4)
$R_{\theta JCTOP}$	Thermal Resistance Junction to Case Top	24.2	°C/W	(5)
$R_{\theta JCBOTTOM}$	Thermal Resistance Junction to Case Bottom	0.9	°C/W	(6)

Notes

3. Compared to AGND.
4. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
6. Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

4.2 Static electrical characteristics

Table 4. Operating range

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Power supply						
I_{SUP123}	Power Supply Current in Normal Mode (V_{SUP} > $V_{SUP\_UV\_7}$)	2.0	–	13.0	mA	
I_{SUP3}	Power Supply Current for VSUP3 in Normal Mode (V_{SUP} > $V_{SUP\_UV\_7}$)	–	3.5	5.0	mA	
I_{SUP_LPOFF1}	Power Supply Current in LPOFF (V_{SUP} = 14 V at T_A = 25 °C)	–	32	–	µA	
I_{SUP_LPOFF2}	Power Supply Current in LPOFF (V_{SUP} = 18 V at T_A = 80 °C)	–	42	60	µA	
V_{SNS_UV}	Power Supply Undervoltage Warning	–	8.5	–	V	
$V_{SNS\_UV\_HYST}$	Power Supply Undervoltage Warning Hysteresis	0.1	–	–	V	
$V_{SUP\_UV\_7}$	Power Supply Undervoltage Lockout (power-up)	7.0	–	8.0	V	
$V_{SUP\_UV\_5}$	Power Supply Undervoltage Lockout (power-up)	–	–	5.6	V	
$V_{SUP\_UV\_L}$	Power Supply Undervoltage Lockout (falling - Boost config.)	–	–	2.7	V	
$V_{SUP\_UV\_L\_B}$	Power Supply Undervoltage Lockout (falling - Buck config.)	–	–	4.6	V	(7)
$V_{SUP\_UV\_HYST}$	Power Supply Undervoltage Lockout Hysteresis	–	0.1	–	V	(8)
V_{PRE} voltage pre-regulator						
V_{PRE}	V_{PRE} Output Voltage • Buck mode (V_{SUP} > $V_{SUP\_UV\_7}$) • Buck mode ($V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V) • Boost mode (V_{SUP} ≥ 2.7 V)	6.25 $V_{PRE\_UV\_4P3}$ 6.0	– V_{SUP} - R_{DSON_PRE} * I_{PRE} –	6.75 – 7.0	V	
I_{PRE}	V_{PRE} Maximum Output Current Capability • Buck or Boost with V_{SUP} > $V_{SUP\_UV\_7}$ • Buck with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V • Boost with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 6.0 V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 – 0.5 – 1.0 0.3	 – – – – –	 1.7 1.7 1.7 – –	A	(8)
I_{PRE_LPOFF}	V_{PRE} Maximum Output Current Capability in LPOFF at low V_{SUP} voltage • Buck with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V • Boost with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 6.0 V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 0.05 1.7 1.0 0.3	 – – – –	 – – – –	A	(8)
I_{PRE_LIM}	V_{PRE} Output Current Limitation	3.5	–	–	A	
I_{PRE_OC}	V_{PRE} Overcurrent Detection Threshold (in buck mode only)	5.0	–	–	A	
V_{PRE_UV}	V_{PRE} Undervoltage Detection Threshold (Falling)	5.5	–	6.0	V	

Notes

7. $V_{SUP\_UV\_L\_B}$ = $V_{PRE\_UV\_4P3}$ + R_{DSON_PRE} * I_{PRE}
8. Guaranteed by design

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{PRE} voltage pre-regulator (continued)						
$V_{PRE\_UV\_HYST}$	V_{PRE} Undervoltage Hysteresis	0.05	–	0.15	V	(9)
$V_{PRE\_UV\_4P3}$	V_{PRE} Shut-off Threshold (Falling - buck and buck/boost)	4.2	–	4.5	V	
$V_{PRE\_UV\_4P3\_HYST}$	V_{PRE} Shut-off Hysteresis	0.05	–	0.15	V	(9)
R_{DSON_PRE}	V_{PRE} Pass Transistor On Resistance	–	–	200	mΩ	
L_{IR_VPRE}	V_{PRE} Line Regulation	–	20	–	mV	(9)
LOR_{VPRE_BUCK}	V_{PRE} Load Regulation for C_{OUT} = 57 µF • I_{PRE} from 50 mA to 2.0 A - Buck mode	–	100	–	mV	(9)
LOR_{VPRE_BOOST}	V_{PRE} Load Regulation for C_{OUT} = 57 µF • I_{PRE} from 50 mA to 2.0 A - Boost mode	–	500	–	mV	(9)
$V_{PRE\_LL\_H}$ $V_{PRE\_LL\_L}$	V_{PRE} Pulse Skipping Thresholds	– –	200 180	– –	mV	
T_{WARN_PRE}	V_{PRE} Thermal Warning Threshold	–	105	–	°C	
T_{SD_PRE}	V_{PRE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_PRE\_HYST}$	V_{PRE} Thermal Shutdown Hysteresis	–	10	–	°C	(9)
$V_{G\_LS\_OH}$	LS Gate Driver High Output Voltage (I_{OUT} = 50 mA)	V_{PRE}-1	–	V_{PRE}	V	
$V_{G\_LS\_OL}$	LS Gate driver Low Level (I_{OUT} = 50 mA)	–	–	0.5	V	
V_{core} voltage regulator						
V_{CORE_FB}	V_{CORE} Feedback Input Voltage	0.784	0.8	0.816	V	
I_{CORE}	V_{CORE} Output Current Capability in Normal Mode • FS6407N • FS6408N	 – –	 – –	 0.8 1.5	A	
I_{CORE_LIM}	V_{CORE} Output Current Limitation • FS6407N • FS6408N	 1 1.8	 – –	 2 3.5	A	
R_{DSON_CORE}	V_{CORE} Pass Transistor On Resistance	–	–	200	mΩ	
$LOR_{VCORE\_1.2}$	V_{CORE} Transient Load regulation - 1.2 V range	-60	–	60	mV	(9), (10)
$LOR_{VCORE\_3.3}$	V_{CORE} Transient Load regulation - 3.3 V range	-100	–	100	mV	(9), (10)
$V_{CORE\_LL\_H}$ $V_{CORE\_LL\_L}$	V_{CORE} Pulse Skipping Thresholds	– –	180 160	– –	mV	
T_{WARN_CORE}	V_{CORE} Thermal Warning Threshold	–	105	–	°C	
T_{SD_CORE}	V_{CORE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_CORE\_HYST}$	V_{CORE} Thermal Shutdown Hysteresis	–	10	–	°C	(9)

Notes

9. Guaranteed by design
10. C_{OUT} = 40 µF, I_{CORE} = 10 mA to 1.5 A, $dI_{CORE}/dt \leq 2.0$ A/µs

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CCA} voltage regulator						
V_{CCA}	V_{CCA} Output Voltage • 5.0 V config. with Internal ballast at 100 mA • 5.0 V config with external ballast at 200 mA • 5.0 V config with external ballast at 300 mA • 3.3 V config with Internal ballast at 100 mA • 3.3 V config with external ballast at 200 mA • 3.3 V config with external ballast at 300 mA	 4.95 4.9 4.85 3.2505 3.234 3.201	 5.0 5.0 5.0 3.3 3.3 3.3	 5.05 5.1 5.15 3.3495 3.366 3.399	V	(11)
I_{CCA_IN}	V_{CCA} Output Current (int. MOSFET)	–	–	100	mA	
I_{CCA_OUT}	V_{CCA} Output Current (external PNP)	–	–	300	mA	
$I_{CCA\_LIM\_INT}$	V_{CCA} Output Current Limitation (int. MOSFET)	100	–	675	mA	
$I_{CCA\_LIM\_OUT}$	V_{CCA} Output Current Limitation (external PNP)	300	–	675	mA	
$I_{CCA\_LIM\_FB}$	V_{CCA} Output Current Limitation Foldback	80	–	200	mA	
$V_{CCA\_LIM\_FB}$	V_{CCA} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{CCA\_LIM\_HYST}$	V_{CCA} Output Voltage Foldback Hysteresis	0.03	–	0.3	V	
$I_{CCA\_BASE\_SC}$ $I_{CCA\_BASE\_SK}$	V_{CCA} Base Current Capability	– 20	– –	30 –	mA	
T_{WARN_CCA}	V_{CCA} Thermal Warning Threshold (int. MOSFET only)	–	105	–	°C	
TSD_{CCA}	V_{CCA} Thermal Shutdown Threshold (int. MOSFET only)	160	–	–	°C	
TSD_{CCA_HYST}	V_{CCA} Thermal Shutdown Hysteresis	–	10	–	°C	(12)
$LORT_{VCCA}$	V_{CCA} Transient Load Regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	–	–	1.0	%	(12)

Notes

11. External PNP gain within 150 to 450
12. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Vaux voltage regulator						
V_{AUX_5}	V_{AUX} Output Voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V_{AUX_33}	V_{AUX} Output Voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V_{AUX_TRK}	V_{AUX} Tracking Error (V_{AUX_5} and V_{AUX_33})	-15	–	+15	mV	
I_{AUX_OUT}	V_{AUX} Output Current	–	–	300	mA	
I_{AUX_LIM}	V_{AUX} Output Current Limitation	300	–	700	mA	
$I_{AUX\_LIM\_FB}$	V_{AUX} Output Current Limitation Foldback	100	–	530	mA	
$V_{AUX\_LIM\_FB}$	V_{AUX} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{AUX\_LIM\_HYST}$	V_{AUX} Output Voltage Foldback Hysteresis	0.03	–	0.3	V	
$I_{AUX\_BASE\_SC}$ $I_{AUX\_BASE\_SK}$	V_{AUX} Base Current Capability	– 7.0	– –	-7.0 –	mA	
TSD_{AUX}	V_{AUX} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{AUX_HYST}	V_{AUX} Thermal Shutdown Hysteresis	–	10	–	°C	(13)
LOR_{VAUX}	V_{AUX} Static Load Regulation (I_{AUX_OUT} = 10 mA to 300 mA)	–	15	–	mV	(13)
$LORT_{VAUX}$	V_{AUX} Transient Load Regulation • I_{AUX_OUT} = 10 mA to 300 mA	–	–	1.0	%	(13)
CAN_5V voltage regulator						
V_{CAN}	V_{CAN} Output Voltage V_{SUP} > 6.0 V in Buck mode V_{SUP} > $V_{SUP\_UV\_L}$ in Boost mode	4.8	5.0	5.2	V	
I_{CAN_OUT}	V_{CAN} Output Current	–	–	100	mA	
I_{CAN_LIM}	V_{CAN} Output Current Limitation	100	–	250	mA	
TSD_{CAN}	V_{CAN} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{CAN_HYST}	V_{CAN} Thermal Shutdown Hysteresis	–	10	–	°C	(13)
V_{CAN_UV}	V_{CAN} Undervoltage Detection Threshold	4.25	–	4.8	V	
$V_{CAN\_UV\_HYST}$	V_{CAN} Undervoltage Hysteresis	0.07	–	0.22	V	
V_{CAN_OV}	V_{CAN} Overvoltage Detection Threshold	5.2	–	5.55	V	
$V_{CAN\_OV\_HYST}$	V_{CAN} Overvoltage Hysteresis	0.07	–	0.22	V	
LOR_{VCAN}	V_{CAN} Load Regulation (from 0 to 50 mA)	–	100	–	mV	(13)

Notes
13. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fail-safe machine voltage supervisor						
V_{PRE_OV}	V_{PRE} Overvoltage Detection Threshold	7.2	–	8.0	V	
$V_{PRE\_OV\_HYST}$	V_{PRE} Overvoltage Hysteresis	–	0.1	–	V	(14)
$V_{CORE\_FB\_UV}$	V_{CORE} FB Undervoltage Detection Threshold	0.67	–	0.773	V	
$V_{CORE\_FB\_UV\_D}$	V_{CORE} FB Undervoltage Detection Threshold - Degraded mode	0.45	–	0.58	V	
$V_{CORE\_FB\_UV\_HYST}$	V_{CORE} FB Undervoltage Hysteresis	10	–	27	mV	(14)
$V_{CORE\_FB\_OV}$	V_{CORE} FB Overvoltage Detection Threshold	0.84	–	0.905	V	
$V_{CORE\_FB\_OV\_HYST}$	V_{CORE} FB Overvoltage Hysteresis	10	–	30	mV	(14)
$V_{CORE\_FB\_DRIFT}$	V_{CORE_FB} Drift versus IO_1	50	100	150	mV	
I_{PD_CORE}	V_{CORE} Internal Pull-down Current (active when $V_{COR\ E}$ is enabled)	5.0	12	25	mA	
$V_{CCA\_UV\_5}$	V_{CCA} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{CCA\_UV\_5D}$	V_{CCA} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{CCA\_UV\_33}$	V_{CCA} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{CCA\_UV\_HYST}$	V_{CCA} Undervoltage Hysteresis	–	0.07	–	V	(14)
$V_{CCA\_OV\_5}$	V_{CCA} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{CCA\_OV\_33}$	V_{CCA} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{CCA\_OV\_HYST}$	V_{CCA} Overvoltage Hysteresis	–	0.15	–	V	(14)
R_{PD_CCA}	V_{CCA} Internal Pull-down Resistor (active when V_{CCA} is disabled)	50	–	160	Ω	
$V_{AUX\_UV\_5}$	V_{AUX} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{AUX\_UV\_5D}$	V_{AUX} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{AUX\_UV\_33}$	V_{AUX} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{AUX\_UV\_HYST}$	V_{AUX} Undervoltage Hysteresis	–	0.07	–	V	(14)
$V_{AUX\_OV\_5}$	V_{AUX} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{AUX\_OV\_33}$	V_{AUX} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{AUX\_OV\_HYST}$	V_{AUX} Overvoltage Hysteresis	–	0.07	–	V	(14)
R_{PD_AUX}	V_{AUX} Internal Pull-down Resistor (active when V_{AUX} is disabled)	50	–	170	Ω	

Notes

14. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fail-safe outputs						
V_{RSTB_OL}	Reset Low Output Level (I_RSTB = 2.0 mA and 2.0 V < V_{SUP} < 40 V)	–	–	0.5	V	(15)
I_{RSTB_LIM}	Reset Output Current Limitation	12	–	25	mA	
V_{RSTB_IL}	External Reset Detection Threshold (falling)	1.0	–	–	V	
V_{RSTB_IH}	External Reset Detection Threshold (rising)	–	–	2.0	V	
$V_{RSTB\_IN\_HYST}$	External Reset Input Hysteresis	0.2	–	–	V	
V_{FS0B_OL}	FS0B Low Output Level (I_FS0b = 2.0 mA)	–	–	0.5	V	
I_{FS0B_LK}	FS0B Input Current Leakage (V_{FS0B} = 28 V)	–	–	1.0	µA	
I_{FS0B_LIM}	FS0B Output Current Limitation	6.0	–	12	mA	
Digital input						
V_{IO_IH}	Digital High Input voltage level (IO_0:1, IO_4:5) • Min Limit = 2.7 V at V_{SUP} = 40 V	2.6	–	–	V	
V_{IO23_IH}	Digital High Input voltage level (IO_2, IO_3)	2.0	–	–	V	
V_{IO_IL}	Digital Low Input voltage Level (IO_0:1; IO_4:5)	–	–	2.1	V	
V_{IO_HYST}	Input Voltage Hysteresis (IO_0:1, IO_4:5)	50	120	500	mV	(16)
V_{IO23_IL}	Digital Low Input voltage Level (IO_2, IO_3)	–	–	0.9	V	
V_{IO23_HYST}	Input Voltage Hysteresis (IO_2, IO_3)	200	450	700	mV	(16)
$I_{IO\_IN\_0:1}$	Input Current for IO_0:1	-5.0	–	100	µA	
$I_{IO\_IN\_1}$	Input Current for IO_1 when used for FB_Core monitoring	-1.0	–	1.0	µA	
$I_{IO\_IN\_2:5}$	Input Current for IO_2:5	-5.0	–	5.0	µA	
$I_{IO\_IN\_LPOFF}$	Input Current for IO_0:5 in LPOFF	-1.0	–	1.0	µA	
Output gate driver						
V_{IO_OH}	High Output Level at I_{IO_OUT} = -2.5 mA	V_{PRE} - 1.5	–	V_{PRE}	V	
V_{IO_OL}	Low Output Level at I_{IO_OUT} = +2.5 mA	0.0	–	1.0	V	
$V_{IO\_OUT\_SK}$ $V_{IO\_OUT\_SC}$	Output Current Capability	2.5 –	– –	– -2.5	mA	
Analog multiplexer						
V_{AMUX_REF1}	Internal Voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V	
V_{AMUX_REF2}	Internal Voltage Reference with $V_{SUP} \leq$ 6.0 V or $V_{SUP} \geq$ 19 V	2.468	2.5	2.532	V	
$V_{AMUX\_TP\_CO}$	Internal Temperature sensor coefficient	–	9.9	–	mV/°C	(16)
V_{AMUX_TP}	Temperature Sensor MUX_OUT output voltage (at T_J=165°C)	2.08	2.15	2.22	V	

Notes

15. For V_{SUP} < 2.0 V, all supplies are already off and external pull-up on RSTB (e.g V_{CORE} or V_{CCA}) pulls the line down.
16. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Interrupt						
V_{INTB_OL}	Low Output Level (I_{INT} = 2.5 mA)	–	–	0.5	V	
R_{PU_INT}	Internal Pull-up Resistor (connected to VDDIO)	–	10	–	KΩ	
I_{INT_LK}	Input Leakage Current	–	–	1	µA	
CAN transceiver						
CAN logic input pin (TXD)						
V_{TXD_IH}	TXD High Input Threshold	0.7 x V_{DDIO}	–	–	V	
V_{TXD_IL}	TXD Low Input Threshold	–	–	0.3 x V_{DDIO}	V	
$TXD_{PULL-UP}$	TXD Main Device Pull-up	20	33	50	KΩ	
TXD_{LK}	TXD Input Leakage Current, V_{TXD} = V_{DDIO}	-1.0	–	1.0	µA	
CAN logic output pin (RXD)						
V_{RXD_OL1}	Low Level Output Voltage (I_{RXD} = 250 µA)	–	–	0.4	V	
V_{RXD_OL2}	Low Level Output Voltage (I_{RXD} = 1.5 mA)	–	–	0.9	V	
$VOUT_{HIGH}$	High Level Output Voltage (I_{RXD} = -250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} - 0.4V	–	–	V	
CAN Output pins (CANH, CANL)						
$V_{DIFF\_COM\_MODE}$	Differential Input Comparator Common Mode Range	-12	–	12	V	
$V_{IN\_DIFF\_SLEEP}$	Differential Input Voltage Threshold in Sleep Mode	0.5	–	0.9	V	
V_{IN_HYST}	Differential Input Hysteresis (in TX, RX mode)	50	–	–	mV	
R_{IN_CHCL}	CANH, CANL Input Resistance	5.0	–	50	kΩ	
R_{IN_DIFF}	CAN Differential Input Resistance	10	–	100	kΩ	
R_{IN_MATCH}	Input Resistance Matching	-3.0	–	3.0	%	
V_{CANH}	CANH Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 – 2.5	 4.5 3.0	V	
V_{CANL}	CANL Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 – 2.5	 2.25 3.0	V	
V_{CAN_SYM}	CAN dominant voltage symmetry (V_{CANL} + V_{CANH})	4.5	5	5.5	V	
V_{OH}-V_{OL}	Differential Output Voltage • TX dominant state (45 Ω < R_{BUS} < 65 Ω) • TX recessive state	 1.5 -50	 2.0 0.0	 3.0 50	 V mV	
$I_{CANL-SK}$	CANL Sink Current Under Short-circuit Condition (V_{CANL} ≤ 12 V, CANL driver ON, TXD low)	40	–	100	mA	
$I_{CANH-SC}$	CANH Source Current Under Short-circuit Condition (V_{CANH} = -2.0 V, CANH driver ON, TXD low)	-100	–	-40	mA	
$R_{INSLEEP}$	CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode	5.0	–	50	kΩ	

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CAN output pins (CANH, CANL) (continued)						
V_{CANLP}	CANL, CANH Output Voltage in Sleep Modes. No termination load.	-0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL Input Current, Device Unsupplied, (V_{CANH}, V_{CANL} =5.0V) • V_{SUP} and V_{CAN} connected to GND • V_{SUP} and V_{CAN} connected to GND via 47k resistor	 -10 -10	 – –	 10 10	 µA µA	(17)
T_{OT}	Overtemperature Detection	160	–	–	°C	
T_{HYST}	Overtemperature Hysteresis	–	–	20	°C	
Digital interface						
$MISO_H$	High Output Level on MISO (I_{MISO} = 1.5 mA)	V_{DDIO} - 0.4	–	–	V	
$MISO_L$	Low Output Level on MISO (I_{MISO} = 2.0 mA)	–	–	0.4	V	
I_{MISO}	Tri-state Leakage Current (V_{DDIO} = 5.0 V)	-5.0	–	5.0	µA	
V_{DDIO}	Supply Voltage for MISO Output Buffer	3.0	–	5.5	V	
IV_{DDIO}	Current consumption on VDDIO	–	1.0	3.0	mA	
SPI_{LK}	SCLK, NCS, MOSI Input Current	-1.0	–	1.0	µA	
V_{SPI_IH}	SCLK, NCS, MOSI High Input Threshold	2.0	–	–	V	
R_{SPI}	NCS, MOSI Internal Pull-up (pull-up to VDDIO)	200	400	800	KΩ	
V_{SPI_IL}	SCLK, NCS, MOSI Low Input Threshold	–	–	0.8	V	
Debug						
V_{DEBUG_IL}	Low Input Voltage Threshold	2.1	2.35	2.6	V	
V_{DEBUG_IH}	High Input Voltage Threshold	4.35	4.6	4.97	V	
I_{DEBUG_LK}	Input Leakage Current	-10	–	10	µA	

Notes

17. Guaranteed by design and characterization.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Digital interface timing						
f_{SPI}	SPI Operation Frequency (50% DC)	0.5	–	8.0	MHz	
t_{MISO_TRANS}	MISO Transition Speed, 20 - 80% • V_{DDIO} = 5.0 V, C_{LOAD} = 50 pF • V_{DDIO} = 5.0 V, C_{LOAD} = 150 pF	 5.0 5.0	 – –	 30 50	ns	
t_{CLH}	Minimum Time SCLK = HIGH	62	–	–	ns	
t_{CLL}	Minimum Time SCLK = LOW	62	–	–	ns	
t_{PCLD}	Propagation Delay (SCLK to data at 10% of MISO rising edge)	–	–	30	ns	
t_{CSDV}	NCS = LOW to Data at MISO Active	–	–	75	ns	
t_{SCLCH}	SCLK Low Before NCS Low (setup time SCLK to NCS change H/L)	75	–	–	ns	
t_{HCLCL}	SCLK Change L/H after NCS = low	75	–	–	ns	
t_{SCLD}	SDI Input Setup Time (SCLK change H/L after MOSI data valid)	40	–	–	ns	
t_{HCLD}	SDI Input Hold Time (MOSI data hold after SCLK change H/L)	40	–	–	ns	
t_{SCLCL}	SCLK Low Before NCS High	100	–	–	ns	
t_{HCLCH}	SCLK High After NCS High	100	–	–	ns	
t_{PCHD}	NCS L/H to MISO at High-impedance	–	–	75	ns	
t_{ONNCS}	NCS Min. High Time	500	–	–	ns	
t_{NCS_MIN}	NCS Filter Time	10	–	40	ns	

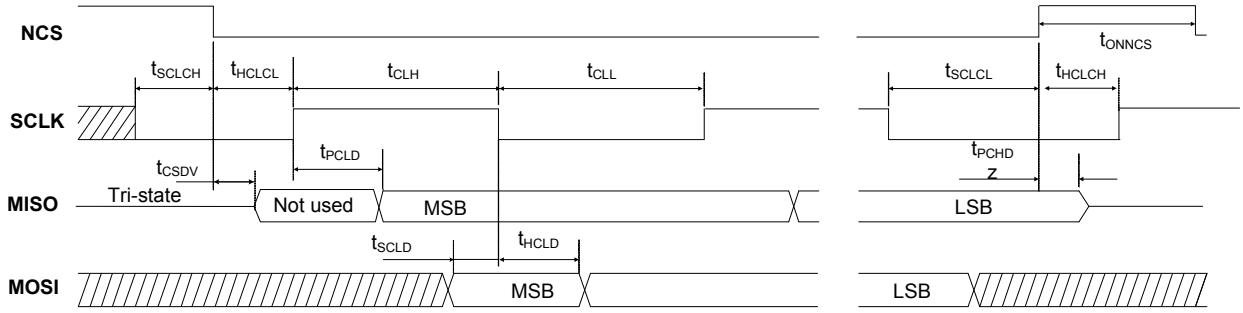


Figure 5. SPI timing diagram

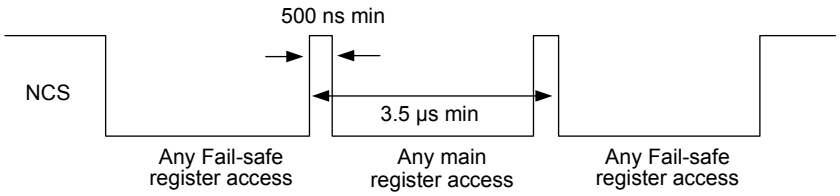


Figure 6. Register access restriction

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CAN dynamic characteristics						
t_{DOUT}	TXD Dominant State Timeout	0.8	–	5.0	ms	
t_{DOM}	Bus Dominant Clamping Detection	0.8	–	5.0	ms	
t_{LOOP}	Propagation Loop Delay TXD to RXD • R_{LOAD} = 120 Ω, C between CANH and CANL = 100 pF, C at RxD < 15 pF	–	–	255	ns	
t_{1PWU}	Single Pulse Wake-up Time	0.5	–	5.0	µs	
t_{3PWU}	Multiple Pulse Wake-up Time	0.5	–	1.0	µs	
t_{3PTO1}	Multiple Pulse Wake-up Timeout (120 µs bit selection)	100	120	–	µs	
t_{3PTO2}	Multiple Pulse Wake-up Timeout (360 µs bit selection)	330	360	–	µs	
t_{CAN_READY}	Delay to Enable CAN by SPI Command (NCS rising edge) to CAN to Transmit (device in normal mode and CAN interface in TX/RX mode)	–	–	100	µs	(18)
Fail-safe state machine						
OSC_{FSSM}	Oscillator	405	–	495	kHz	
CLK_{FS_MIN}	Fail-safe Oscillator Monitoring	150	–	–	kHz	
t_{IC_ERR}	IO_0:5 Filter Time	4.0	–	20	µs	
t_{ACK_FS}	Acknowledgement Counter (used for IC error handling IO_1 and IO_5)	7.0	–	9.7	ms	
$t_{\_DFS\_RECOVERY}$	IO_0 Filter Time to Recover from Deep Reset and Fail State	0.8	–	1.3	ms	
$t_{IO1\_DRIFT\_MON}$	IO_1 filter time	1.0	–	2.0	ms	
Fail-safe output						
t_{RSTB_FB}	RSTB Feedback Filter Time	8.0	–	15	µs	
t_{FSOB_FB}	FS0B Feedback Filter Time	8.0	–	15	µs	
t_{RSTB_BLK}	RSTB Feedback Blanking Time	180	–	320	µs	
t_{FSOB_BLK}	FS0B Feedback Blanking Time	180	–	320	µs	
t_{RSTB_POR}	Reset Delay Time (after a Power On Reset or from LPOFF)	12	15.9	23.6	ms	(19)
t_{RSTB_LG}	Reset Duration (long pulse)	8.0	–	10	ms	
t_{RSTB_ST}	Reset duration (short pulse)	1.0	–	1.3	ms	
t_{RSTB_IN}	External Reset Delay time	8.0	–	15	µs	
t_{DIAG_SC}	Fail-safe Output Diagnostic Counter (FS0B)	550	–	800	µs	
VSUP voltage supply						
C_{SUP}	Minimum capacitor on Vsup	44	–	–	µF	

Notes

18. For proper CAN operation, TXD must be set to high level before CAN enable by SPI, and must remain high for at least T_{CAN_READY}.
19. This timing is not guaranteed in case of fault during startup phase (after Power On Reset of from LPOFF)

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{PRE} voltage pre-regulator						
f_{SW_PRE}	V_{PRE} Switching Frequency	412	437.5	465	kHz	
t_{SW_PRE}	V_{SW_PRE} On and Off Switching Time	–	–	30	ns	(20)
t_{PRE_SOFT}	V_{PRE} Soft Start Duration ($C_{OUT} \leq$ 100 µF)	500	–	700	µs	
$t_{PRE\_BLK\_LIM}$	V_{PRE} Current Limitation Blanking Time	200	–	600	ns	
t_{IPRE_OC}	V_{PRE} Overcurrent Filtering Time	30	–	120	ns	(20)
t_{PRE_UV}	V_{PRE} Undervoltage Filtering Time	20	–	40	µs	
$t_{PRE\_UV\_4p3}$	Vpre Shut-off Filtering Time	3.0	–	7.0	µs	
$d_{IPRE/DT}$	V_{PRE} Load Regulation Variation	–	–	25	A/ms	(20)
t_{PRE_WARN}	V_{PRE} Thermal Warning Filtering Time	30	–	40	µs	
t_{PRE_TSD}	V_{PRE} Thermal Detection Filtering Time	1.0	–	3.0	µs	
$t_{LS\_RISE/FALL}$	LS Gate Voltage Switching Time (I_{OUT} = 300 mA)	–	–	50	ns	
V_{sense} voltage regulator						
t_{VSNS_UV}	V_{SNS} Undervoltage Filtering Time	1.0	–	3.0	µs	
V_{core} voltage regulator						
$t_{CORE\_BLK\_LIM}$	V_{CORE} Current Limitation Blanking Time	20	–	40	ns	
f_{SW_CORE}	V_{CORE} Switching Frequency	2.20	2.34	2.49	MHz	
t_{SW_CORE}	V_{SW_CORE} On and Off Switching Time	6.0	–	12	ns	
V_{CORE_SOFT}	V_{CORE} Soft Start (C_{OUT} = 100 µF max)	–	–	10	V/ms	
t_{CORE_WARN}	V_{CORE} Thermal Warning Filtering Time	30	–	40	µs	
t_{CORE_TSD}	V_{CORE} Thermal Detection Filtering Time	1.0	–	3.0	µs	
V_{cca} voltage regulator						
t_{CCA_LIM}	V_{CCA} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{CCA\_LIM\_OFF1}$ $t_{CCA\_LIM\_OFF2}$	V_{CCA} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{CCA_WARN}	V_{CCA} Thermal Warning Filtering Time	30	–	40	µs	
t_{CCA_TSD}	V_{CCA} Thermal Detection Filter Time (int. MOSFET)	1.0	–	3.0	µs	
dI_{LOAD}/dt	V_{CCA} Load Transient	–	2.0	–	A/ms	(20)
V_{CCA_SOFT}	V_{CCA} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	

Notes

20. Guaranteed by characterization.

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{aux} voltage regulator						
t_{AUX_LIM}	V_{AUX} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{AUX\_LIM\_OFF1}$ $t_{AUX\_LIM\_OFF2}$	V_{AUX} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{AUX_TSD}	V_{AUX} Thermal Detection Filter Time	1.0	–	3.0	µs	
dI_{AUX}/dt	V_{AUX} Load Transient	–	2.0	–	A/ms	(21)
V_{AUX_SOFT}	V_{AUX} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	
CAN_5V voltage regulator						
t_{CAN_LIM}	Output Current Limitation Filter Time	2.0	–	4.0	µs	
t_{CAN_TSD}	V_{CAN} Thermal Detection Filter Time	1.0	–	3.0	µs	
t_{CAN_UV}	V_{CAN} Undervoltage Filtering Time	4.0	–	7.0	µs	
t_{CAN_OV}	V_{CAN} Overvoltage Filtering Time	100	–	200	µs	
dI_{CAN}/dt	V_{CAN} Load Transient	–	100	–	A/ms	(21)
Fail-safe machine voltage supervisor						
t_{PRE_OV}	V_{PRE} Overvoltage Filtering Time	128	–	234	µs	
t_{CORE_UV}	V_{CORE} FB Undervoltage Filtering Time	4.0	–	10	µs	
t_{CORE_OV}	V_{CORE} FB Overvoltage Filtering Time	128	–	234	µs	
t_{CCA_UV}	V_{CCA} Undervoltage Filtering Time	4.0	–	10	µs	
t_{CCA_OV}	V_{CCA} Overvoltage Filtering Time	128	–	234	µs	
t_{AUX_UV}	V_{AUX} Undervoltage Filtering Time	4.0	–	10	µs	
t_{AUX_OV}	V_{AUX} Overvoltage Filtering Time	128	–	234	µs	
Digital input - multi-purpose IOS						
F_{IO_IN}	Digital Input Frequency Range	0.0	–	100	kHz	
Analog multiplexer						
t_{MUX_READY}	SPI Selection to Data Ready to be Sampled on Mux_out • V_{DDIO} = 5.0 V, C_{MUX_OUT} = 1.0 nF	–	–	10	µs	
Interrupt						
t_{INTB_LG}	INTB Pulse Duration (long)	90	100	–	µs	
t_{INTB_ST}	INTB Pulse Duration (short)	20	25	–	µs	
Functional sate machine						
t_{WU_GEN}	General Wake-up Signal Deglitch Time (for any wu signal on IOs)	60	70	80	µs	

Notes

21. Guaranteed by characterization.

5 Functional pin description

5.1 Introduction

The FS6407/FS6408 is the third generation of the System Basis Chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN interface, external ICs such as sensors, and accurate reference voltage for A to D converters.
- Built-in enhanced high-speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, protection, and Fail-safe operation mode.
- Low-power mode, with ultra low-current consumption.
- Various wake-up capabilities.
- Enhanced safety features with multiple fail-safe outputs and scheme to support SIL applications.

5.2 Power supplies (VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the inputs pins for internal supply dedicated to SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO7637 pulses. VSUP1,2, and 3 must be connected to the same supply (Figure 49).

5.3 VSENSE input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX-OUT pin. VSENSE pin is robust against ISO7637 pulses.

5.4 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the FS6407/FS6408. It can be configured as a “non-inverting buck-boost converter” (Figure 24) or “standard buck converter” (Figure 23), depending on the external configuration (connection of pin GATE_LS). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high-side switching MOSFET is also integrated to make the current control easier. The pre-regulator delivers a typical output voltage of 6.5 V, which is used internally. Current limitation, overcurrent, overvoltage, and undervoltage detectors are provided. VPRE is enabled by default.

5.5 VCORE output (from 1.2 V to 3.3 V range)

The VCORE block is an SMPS regulator. The voltage regulator is a step down DC-DC converter operating in voltage control mode. The output voltage is configurable from 1.2 V to 3.3 V range thanks to an external resistor divider connected between VCORE and the feedback pin (FB_CORE) (as example in Figure 1, Figure 2, and Figure 49).

The stability of the converter is done externally, by using the COMP_CORE pin. Current limitation, overvoltage, and undervoltage detectors are provided. VCORE can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCORE by SPI when VCORE is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCORE overvoltage information disables VCORE. Diagnostics are reported in the dedicated register and generate an Interrupt. VCORE is enabled by default.

5.6 VCCA output, 5.0 V or 3.3 V selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal transistor delivering very good accuracy (±1.0% for 5.0 V configuration and ±1.5% for 3.3 V configuration), with a limited current capability (100 mA) for an analog to digital converter, or with an external PNP transistor, giving higher current capability (up to 300 mA) with lower output voltage accuracy (±3.0% for 300 mA) when using a local supply.

Current limitation, overvoltage, and undervoltage detectors are provided. VCCA can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCCA by SPI when VCCA is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCCA overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt. VCCA is enabled by default.

5.7 VAUX output, 5.0 V or 3.3 V selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints. The VAUX output voltage regulator can be used as “auxiliary supply” (local supply) or “sensor supply” (external supply) with the possibility to be configured as a tracking regulator following VCCA.

Current limitation, overvoltage, and undervoltage detectors are provided. VAUX can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VAUX by the SPI when VAUX is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VAUX overcurrent and overvoltage information disables V_{AUX}, reported in the dedicated register, and generates an Interrupt. V_{AUX} is enabled by default.

5.8 SELECT input (VCCA, VAUX voltage configuration)

VCCA and VAUX output voltage configurations are set by connecting an external resistor between the SELECT pin and Ground. According to the value of this resistor, the voltage of VCCA and VAUX are configured after each Power On Reset, and after a wake-up event when device is in LPOFF. Information latches until the next hardware configuration read. Regulator voltage values can be read on the dedicated register via the SPI.

Table 6. V_{CCA}/V_{AUX} voltage selection (Figure 50)

V_{CCA}(V)	V_{AUX}(V)	R Select	Recommended value
3.3	3.3	<7.0 KΩ	5.1 KΩ ±5.0%
5.0	5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
3.3	5.0	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	3.3	45.9 << 56.1 KΩ	51 KΩ ±5.0%

When VAUX is not used, the output VCCA voltage configuration is set using an external resistor connected between the SELECT and the VPRE pin.

Table 7. V_{CCA} voltage selection (V_{AUX} not used, Figure 51, Figure 52)

V_{CCA}(V)	R Select	Recommended Value
3.3	<7.0 KΩ	5.1 KΩ ±5.0%
	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
	45.9 << 56.1 KΩ	51 KΩ ±5.0%

5.9 CAN_5V voltage regulator

The CAN_5V voltage regulator is a linear regulator dedicated to the internal HSCAN interface. An external capacitor is required. Current limitation, overvoltage, and undervoltage detectors are provided. If the internal CAN transceiver is not used, the CAN_5V regulator can supply an external load (CAN_5V voltage regulator). CAN_5V is enabled by default.

5.10 Interrupt (INTB)

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. INTB has an internal pull-up resistor connected to VDDIO.

5.11 CANH, CANL, TXD, RXD

These are the pins of the high speed CAN physical interface. The CAN transceivers provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. The CAN interface is connected to the MCU via the RXD and TXD pins.

5.11.1 TXD

TXD is the device input pin to control the CAN bus level. TXD is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In Normal mode, when TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus in a recessive state. When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection that disables the bus when TXD is dominant for more than T_{DOUT}. In LPOFF mode, VDDIO is OFF, pulling down this pin to GND.

5.11.2 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In Normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in high-impedance state.

5.11.3 CANH and CANL

These are the CAN bus pins. CANL is a low-side driver to GND, and CANH is a high-side driver to CAN_5V. In Normal mode and TXD high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is approximately 2.5 V, provided by the internal bus biasing circuitry. When TXD is low, CANL is pulled to GND and CANH to CAN_5V, creating a differential voltage on the CAN bus.

In LPOFF mode, the CANH and CANL drivers are OFF, and these pins are pulled down to GND via the device R_{IN_CHCL} resistors. CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

5.12 Multiplexer output MUX_OUT

The MUX_OUT pin (Figure 7) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX_OUT is selected via the SPI, from one of the following parameters:

- Internal 2.5 V reference
- Die temperature sensor T(°C) = (V_{AMUX} - V_{AMUX_TP}) / $V_{AMUX\_TP\_CO}$ + 165

Voltage range at MUX_OUT is from GND to VDDIO (3.3 V or 5.0 V)

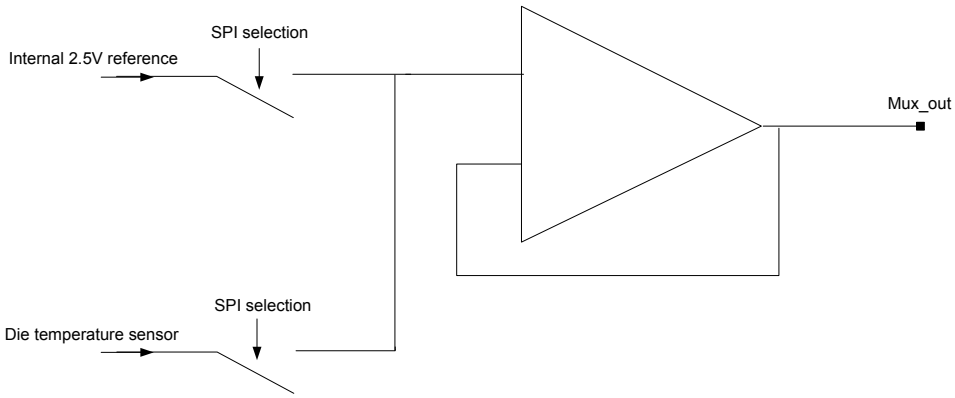


Figure 7. Simplified analog multiplexer block diagram

5.13 I/O pins (I/O_0:I/O_5)

The FS6407/FS6408 includes six multi-purpose I/Os (I/O_0 to I/O_5). I/O_0, I/O_1, I/O_4, and I/O_5 are robust against ISO7637 pulses. An external serial resistor must be connected to those pins to limit the current during ISO pulses.

Table 8. I/Os configuration

I/0 number	Digital input	Wake-up capability	Output gate driver
IO_0	X	X	
IO_1	X	X	
IO_2	X	X	
IO_3	X	X	
IO_4	X	X	X
IO_5	X	X	X

- IO_0:1 are selectable as follows:
  Analog input (load dump proof) sent to the MCU through the MUX_OUT pin. Wake-up input on the rising or falling edge or based on the previous state. Digital input (logic level) sent to the MCU through the SPI. **Safety purpose**: Digital input (logic level) to perform an IC error monitoring (both IO_0 AND IO_1 are used if configured as safety inputs, see Figure 9).
- IO_1 is also selectable as follow:
  Safety purpose: FB_Core using a second resistor bridge (R3/R4 duplicated) connected to IO_1, to detect external resistor drift and trigger when FB_Core - IO_1 > ±150 mV max.
- IO_2:3 are selectable as follows:
  Digital input (logic level) sent to the MCU through the SPI. Wake-up input (logic level) on the rising or falling edge or based on the previous state. **Safety purpose**: Digital input (logic level) to monitor MCU error signals (both IO_2 AND IO_3 are used if configured as safety inputs). Only bi-stable protocol is available.
  When IO_2:3 are used as safety inputs to monitor FCCU error outputs from the NXP MCU, the monitoring is active only when the Fail-safe sate machine is in “normal WD running” state (Figure 11) and all the phases except the “Normal Phase” are considered as an Error.

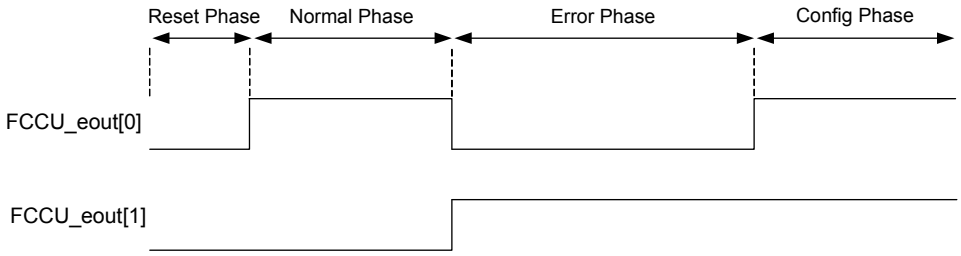


Figure 8. IO_2:3 MCU error monitoring: bi-stable protocol

- IO_4:5 are selectable as follows:
  Digital input (logic level) sent to the MCU through the SPI. Wake-up input (load dump proof) on rising or falling edge or based on previous state. Output gate driver (from V_{PRE}) for low-side logic level MOSFET. **Safety purpose**: Digital input (logic level) to perform an IC error monitoring (both IO_4 AND IO_5 are used if configured as safety inputs, see Figure 9).

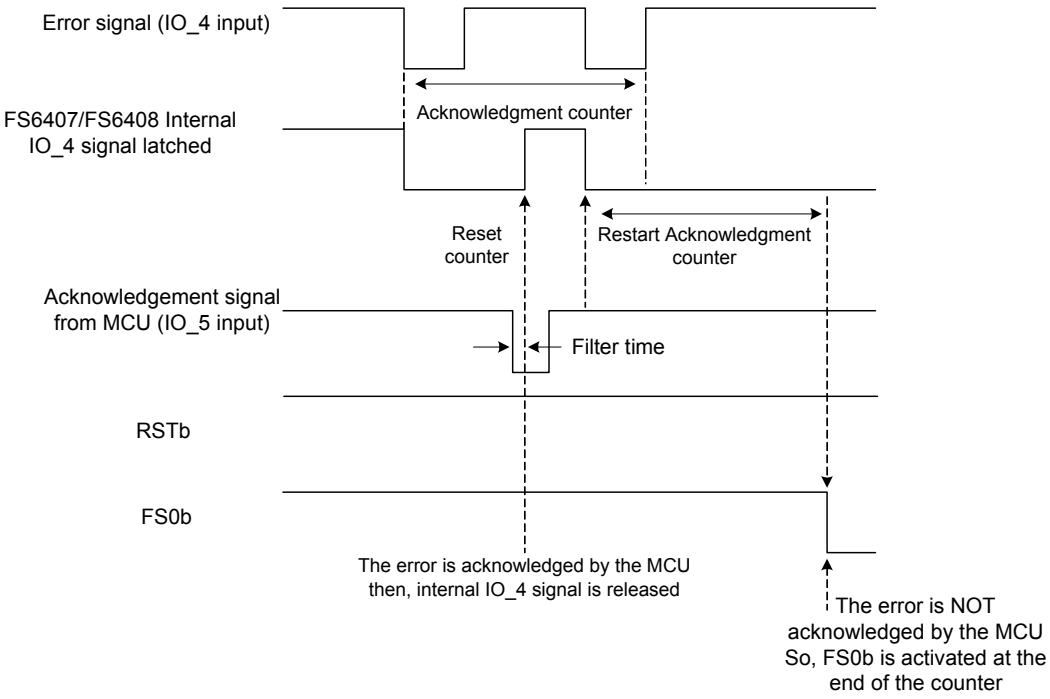


Figure 9. External error signal handling

5.14 SAFE output pins (FS0B, RSTB)

FS0B is asserted low when a fault event occurs (See Faults triggering FS0B activation on page 40). The objective of this pin is to drive an electrical safe circuitry independent from the MCU to deactivate the whole system and set the application in a protected and known state.

After each power on reset or after each wake-up event (LPOFF), the FS0B pin is asserted low. The MCU can then decide to release the FS0B pin, when the application is ready to start. An external pull-up circuitry is mandatory connected to VDDIO or VSUP3.

- If the pull-up is connected to VDDIO, the value recommended is 5.0 kΩ. There is no current in LPOFF since VDDIO is OFF in the LPOFF mode.
- If the pull-up is connected to VSUP3, the value must be above 10 kΩ. There is a current in the pull-up resistor to consider at the application level in LPOFF mode.

The RSTB pin must be connected to the MCU and is active low. An external pull-up resistor must be connected to VDDIO. In default configuration, the RST delay time has three possible values depending on the mode and product configuration:

- The longest one is used automatically following a Power On Reset or when resulting from LPOFF mode (Low Power Off).
- The two reset durations are then available in the INIT_FSSM1 register, which are 1.0 ms and 10 ms. The configured duration is used in the normal operation when a fault occurs leading to a reset activation. The INIT_FSSM1 register is available (writing) in the INIT FS phase.

5.15 DEBUG input (entering in debug mode)

The DEBUG pin allows the product to enter Debug mode. To activate Debug mode, the voltage applied to the DEBUG pin must be within the V_{DEBUG_IL} and V_{DEBUG_IH} range at start-up. If the voltage applied to DEBUG pin is out of these limits before V_{CORE} ramp-up, the device settles into Normal mode. When Debug mode is activated, the FS0B output is asserted low at start-up. As soon as the FS0B is released to “high” via SPI (Good WD answer and FS_OUT writing), this pin is never activated, whatever the fault is reported.

In Debug mode, any errors from the watchdog are ignored (No reset and No fail-safe), even if the whole functionality of the watchdog is kept ON (Seed, LFSR, Wd_refresh counter, WD error counter). This allows an easy debug of the hardware and software routines (i.e. SPI commands). When Debug mode is activated, the CAN transceiver is set to Normal operation mode. This allows communication with the MCU, in case SPI communication is not available (case of MCU not programmed). To exit Debug mode, the pin must be tied to ground through an external pull-down resistor or to VPRE through an external pull-up resistor and a Power On Reset occurs.

6 Functional device operation

6.1 Mode and state description of main state machine

The device has several operation modes. The transition and conditions to enter or leave each mode are illustrated in the functional state diagram (Figure 10). Two state machines are working in parallel. The Main state machine is in charge of the power management (VPRE, VCORE, VCCA, VAUX,...) and the fail-safe state machine is in charge of all the safety aspect (WD, RSTB, FS0B,...).

6.1.1 Buck or buck boost configuration

An external low-side logic level MOSFET (N-type) is required to operate in non-inverting buck-boost converter. The connection of the external MOSFET is detected automatically during the start-up phase (after a Power On Reset or From LPOFF).

- If the external low-side MOSFET is NOT connected (GATE_LS pin connected to PGND), the product is configured as a standard buck converter.
- If the external low-side MOSFET is connected (GATE_LS pin connected to external MOSFET gate), the product is configured as a non-inverting buck-boost converter.

The automatic detection is accomplished by pushing a 300 µA current on Gate_LS pin and monitoring the corresponding voltage generated. If a voltage >120 mV is detected before the 120 µs timeout, the non-inverting buck-boost configuration is locked. Otherwise, the standard buck configuration is locked. The boost driver has a current capability of ±300 mA.

6.1.2 VPRE on

Pre-regulator is an SMPS regulator. In this phase, the pre-regulator is switched ON and a softstart with a specified duration t_{PRE_SOFT} is started to control the VPRE output capacitor charge.

6.1.3 Select pin configuration

This phase is detecting the required voltage level on VAUX and VCCA, according to resistor value connected between the SELECT pin and ground. If the SELECT pin is connected to VPRE via the resistor, it disables the VAUX regulator at start-up.

6.1.4 VCORE/VAUX/VCCA on

In this stage, the three regulators VCORE, VAUX, and VCCA are switched ON at the same time with a specified soft start duration. The CAN_5V is also started at that time.

6.1.5 INIT main

This mode is automatically entered after the device is “Powered ON”. When RSTB is released, initialization phase starts where the device can be configured via the SPI. During INIT phase, some registers can only be configured in this mode (refer to Table 14 and Table 15). Other registers can be written in this mode, and also in Normal mode.

Once the INIT registers configurations are complete, a last register called “INIT INT” must be configured to switch to Normal mode. Writing data in this register (even same default values), automatically locks the INIT registers, and the product switches automatically to Normal mode in the Main state machine.

6.1.6 Normal

In this mode, all device functions are available. This mode is entered by a SPI command from the INIT phase by writing in the INIT INT register. While in Normal mode, the device can be set to Low Power mode (LPOFF) using secured SPI command.

6.1.7 Low-power mode off

The Main State Machine has 3 LPOFF modes with different conditions to enter and exit each LPOFF mode as described here after. After wake up from LPOFF, all the regulators are enabled by default. In LPOFF, all the regulators are switched OFF. The register configuration, the V_{PRE} behavior and the ISO pulse requirement are valid for the 3 LPOFF modes.

6.1.7.1 LPOFF - sleep

Entering in Low Power mode LPOFF - SLEEP is only available if the product is in Normal mode by sending a secured SPI command. In this mode, all the regulators are turned OFF and the MCU connected to the VCORE regulator is unsupplied.

Before entering in LPOFF Power mode OFF-sleep, the Reset Error Counter must go back to value “0” (“N” consecutive good watchdog refreshes decrease the reset error counter to 0). “N” = RSTb_err_2:0 x (WD_refresh_2:0 + 1). Once the FS6407/FS6408 is in LPOFF - SLEEP, the device monitors external events to wake-up and leave the Low Power mode. The wake-up events can occur and depending of the device configuration from:

- CAN
- I/O inputs

When a wake-up event is detected, the device starts the main state machine again by detecting the V_{PRE} configuration (BUCK or BUCK-BOOST), the wake-up source is reported to the dedicated SPI register, and the Fail-safe state machine is also restarted.

6.1.7.2 LPOFF - V_{PRE_UV}

LPOFF- V_{PRE_UV} is entered when the device is in the INIT or Normal mode, and if the VPRE voltage level is passing the $V_{PRE\_UV\_L\_4P3}$ threshold (typ 4.3 V). After 1.0 ms the device attempts to recover by switching ON the VPRE again.

6.1.7.3 LPOFF - deep FS

LPOFF - DEEP FS is entered when the device is in Deep Fail-safe and if the Key is OFF (IO_0 is low). To exit this mode, a transition to high level on IO_0 is required. IO_0 is usually connected to key ON key OFF signal.

6.1.7.4 Register configuration in LPOFF

In LPOFF, the register settings of the main state machine are kept because the internal 2.5 V main digital regulator is available for wake-up operation. However, the register settings of the fail-safe state machine are erased, because the 2.5 V fail safe digital regulator is not available in LPOFF. As a consequence, after a wake-up event, the configuration of the fail-safe registers must be done again during initialization phase (256 ms open window).

6.1.7.5 V_{PRE} behavior in LPOFF

When device is in LPOFF Sleep mode, and if the VSUP < $V_{SUP\_UV\_7}$, VPRE is switched on to maintain internal biasing and wake-up capabilities on IOs or CAN.

- If V_{PRE} is configured as a non-inverting buck-boost converter, VPRE is switched ON in SMPS mode with boost functionality.
- If V_{PRE} is configured as a standard buck converter, V_{PRE} is switched ON in Linear mode following V_{SUP}.

6.2 Mode and state description of fail-safe state machine

6.2.1 LBIST

Included in the fail-safe machine, the Logic Built-in Self Test (LBIST) verifies the correct functionality of the FSSM at start-up. The fail-safe state machine is fully checked and if an issue is reported, the RSTB stays low and after 8 s, the device enters in DEEP Fail-safe. LBIST is run at start-up and after each wake-up event when the device is in LPOFF mode.

6.2.2 Select pin configuration

This phase detects the required voltage level to apply on VAUX and VCCA, according to the resistor value connected between the SELECT pin and ground, (V_{AUX} used) or between the SELECT pin and VPRE (V_{AUX} not used). This mode is the equivalent mode seen in the main state machine. Difference is in the fail-safe machine, this detection is used to internally set the UV/OV threshold on VCCA and VAUX for the voltage supervision.

6.2.3 ABIST

Included in the fail-safe machine, the analog built-in self test (ABIST) verifies the correct functionality of the analog part of the device, like the overvoltage and undervoltage detections of the voltage supervisor and the RTSTB and FS0B fail-safe outputs feedback (Table 9). The ABIST is run at start-up and after each wake-up event when the device is in LPOFF mode.

Table 9. Regulators and fail-safe pins checked during ABIST

Parameters	Overvoltage	Undervoltage	OK/NOK
VPRE	X		
VCORE	X	X	
VCCA	X	X	
VAUX	X	X	
IO_1 FB_Core Delta			X
RSTB			X
FS0B			X

6.2.4 Release RSTB

In this state, the device releases the RSTB pin.

6.2.5 INIT FS

This mode is automatically entered after the device is “powered on” and only if built-in self tests (Logic and Analog) have been passed successfully. This INIT FS mode starts as soon as RSTB is released (means no “Activate RST” faults are present and no external reset is requested). Faults leading to an “Activate RST” are described in Reset error counter.

In this mode, the device can be configured via the SPI within a maximum time of 256 ms, including first watchdog refresh. Some registers can only be configured in this mode and is locked when leaving INIT FS mode (refer to Table 14 and Table 15). It is recommended, to configure first the device before sending the first WD refresh. As soon as the first good watchdog refresh is sent by the MCU, the device leaves this mode and goes into Normal WD mode.

6.2.6 Normal WD is running

In this mode, the device waits for a periodic watchdog refresh coming from the MCU, within a specific configured window timing. Configuration of the watchdog window period can be set during INIT FS phase or in this mode. This mode is exited if there are consecutive bad watchdog refreshes, if there is an external reset request, or if a fault occurs leading to an RSTB activation.

6.2.7 RST delay

When the reset pin is asserted low by the device, a delay runs, to release the RSTB, if there are no faults present. The reset low duration time is configurable via the SPI in the INIT_ FSSM1 register, which is accessible for writing only in the INIT FS phase.

6.3 Deep fail-safe state

The Fail-safe state machine monitors the RSTB pin of the device and count the number of reset(s) happening in case of fault detection (see Reset error counter). As soon as either the reset error counter reach its final value or the RESET pin remains asserted low for more than 8.0 s, the device moves to Deep Fail-safe state, identified by the “Wait Deep Fail-safe” state in the functional state diagram (Figure 10).

When the device is in Deep Fail-safe state, all the regulators are OFF. To exit this state, a Key OFF / Key ON action is needed. IO_0 is usually connected to key signal. Key OFF (IO_0 low) moves the device to LPOFF-Deep FS, and Key ON (IO_0 high) wakes up the device.

The final value of the reset error counter can be configured to 2 or 6 in the register INIT FSSM 2. During power up phase, the 8.0 s timer starts when the Fail-safe state machine enters in the “Select pin config detection” state and stop when the RSTB pin is released. During “INIT FS” state, the 8.0 s timer can be disabled in the register INIT SUPERVISOR 2. During “Normal WD running” state, the 8.0 s timer is activated at each RSTB pin assertion.

6.4 Functional state diagram

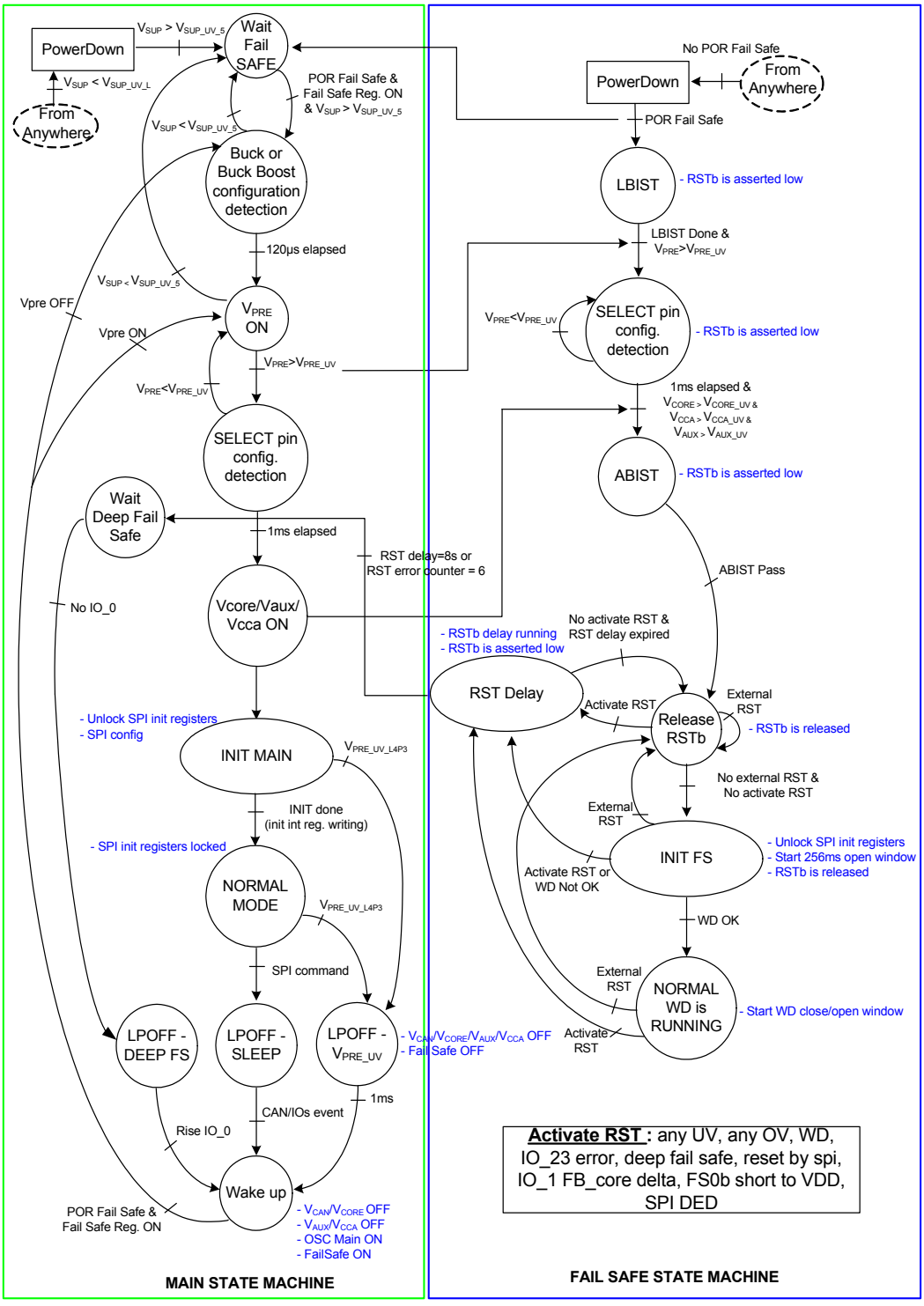


Figure 10. Simplified state diagram

6.5 Fail-safe machine

To fulfill safety critical applications, the FS6407/FS6408 integrates a dedicated fail-safe machine (FSM). The FSM is composed of three main sub-blocks: the voltage supervisor (VS), the Fail-safe state machine (FSSM), and the fail-safe output driver (FSO).The FSM is electrically independent from the rest of the circuitry, to avoid common cause failure.

For this reason, the FSM has its own voltage regulators (analog and digital), dedicated bandgap, and its own oscillator. Three power supply pins (VSUP 1, 2, & 3) are used to overtake a pin lift issue. The internal voltage regulators are directly connected on VSUP (one bonding wire per pin is used). Additionally, the ground connection is redundant as well to avoid any loss of ground.

All the voltages generated in the device are monitored by the voltage supervisor (under & overvoltage) owing to a dedicated internal voltage reference (different from the one used for the voltage regulators). The result is reported to the MCU through the SPI and delivered to the Fail-safe state machine (FSSM) for action, in case of a fault. All the safety relevant signals feed the FSSM, which handles the error handling and controls the fail-safe outputs.

There are two fail-safe outputs: RSTB (asserted low to reset the MCU), and FS0B (asserted low to control any fail-safe circuitry). The Fail-safe machine is in charge of bringing and maintaining the application in a Fail-safe state. Four sub Fail-safe states are implemented to handle the different kinds of failures, and to give a chance for the system to come back to a normal state.

6.5.1 Fail-safe machine state diagram

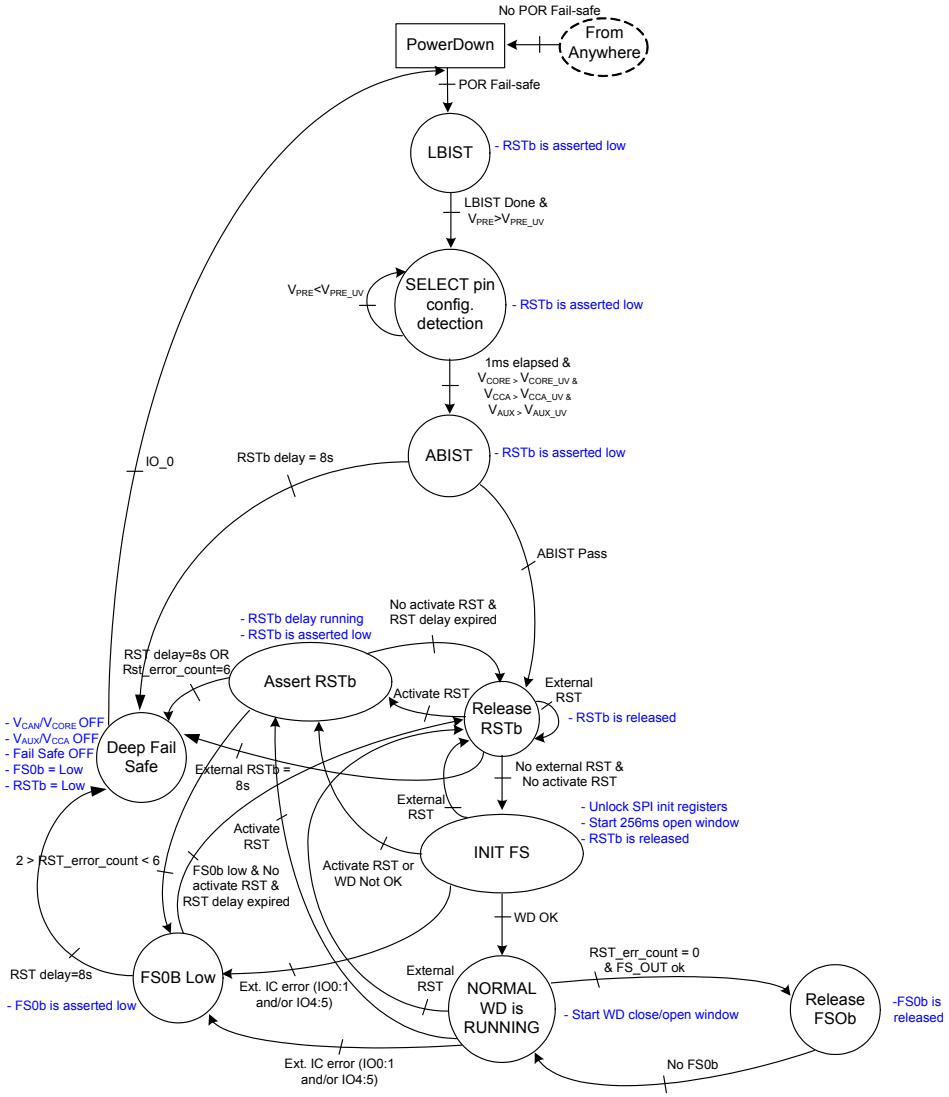


Figure 11. Detailed fail-safe state diagram

6.5.2 Watchdog operation

A windowed watchdog is implemented in the FS6407/FS6408 and is based on “question/answer” principle (Challenger). The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The error handling and watchdog operations are managed by the Fail-safe state machine. For debugging purpose, this functionality can be inhibited by setting the right voltage on the DEBUG pin at start-up.

The watchdog window duration is selectable through the SPI during the INIT FS phase or in Normal mode. The following values are available: 1.0 ms, 2.0 ms, 3.0 ms, 4.0 ms, 6.0 ms, 8.0 ms, 12 ms, 16.0 ms, 24 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, and 1024 ms. The watchdog can also be inhibited through the SPI register to allow “reprogramming” (ie.at vehicle level through CAN).

An 8-bit pseudo-random word is generated, due to a linear feedback shift register implemented in the FS6407/FS6408. The MCU can send the seed of the LFSR or use the LFSR generated by the FS6407/FS6408 during the INIT phase and performs a pre-defined calculation. The result is sent through the SPI during the “open” watchdog window and verified by the FS6407/FS6408. When the result is right, a new LFSR is generated and the watchdog window is restarted. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, and the LFSR value is not changed. Any access to the WD register during the “closed” watchdog window is considered a wrong WD refresh.

6.5.2.1 Normal operation (first watchdog refresh)

At power up, when the RSTB is released as high (after around 16 ms), the INIT phase starts for a maximum duration of 256 ms and this is considered as a fully open watchdog window. During this initialization phase the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the FS6407/FS6408 (0xB2), available in the WD_LFSR register (Table 74). Using this LFSR, the MCU performs a simple calculation based on this formula. As an example, the result of this calculation based on LFSR default value (0xB2) is 0x4D.

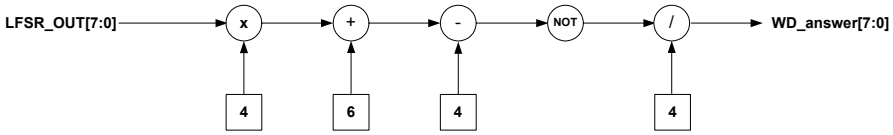


Figure 12. Watchdog answer calculation

The MCU sends the results in the WD answer register (Table 76). When the watchdog is properly refreshed during the open window, the 256 ms open window is stopped and the initialization phase is finished. A new LFSR is generated and available in the WD LFSR register, Table 73. If the watchdog refresh is wrong or if the watchdog is not refreshed during this 256 ms open window (INIT FS phase), the device asserts the reset low and the RSTB error counter is incremented by “1”.

After a good watchdog refresh, the device enters the Normal WD refresh mode, where open and closed windows are defined either by the configuration made during initialization phase in the watchdog window register (Table 72), or by the default value already present in this register (3.0 ms).

6.5.2.2 Normal watchdog refresh

The watchdog must be refreshed during every open window of the window period configured in the register Table 72. Any WD refresh restarts the window. This ensures the synchronization between MCU and FS6407/FS6408.

The duration of the “window” is selectable through the SPI with no access restriction, means the window duration can be changed in the INIT phase or Normal mode. Doing the change in normal operation allow the system integrator to configure the watchdog window duration on the fly:

- The new WD window duration (except after disable) is taken into account when a write in the WD_answer register occurs (good or bad WD answer) or when the previous WD window is finished without any writing (WD timeout)
- The new WD window duration after disable is taken into account when SPI command is validated

The duty cycle of the window is set to 50% and is not modifiable.

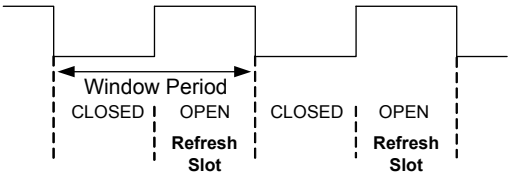


Figure 13. Windowed watchdog

6.5.2.3 Watchdog in debug mode

When the device is in debug mode (entered via the DEBUG pin), the watchdog continues to operate, but does not affect the device operation by asserting a reset or fail-safe pins. For the user, operation appears without the watchdog. If needed and to debug the watchdog itself, the user can operate as in Normal mode and check LFSR values, the watchdog refresh counter, the watchdog error counter, and reset counter. This allows the user to debug their software and ensure a good watchdog strategy in the application.

6.5.2.4 Wrong watchdog refresh handling

Error counters and strategy are implemented in the device to manage wrong watchdog refreshes from the MCU. According to consecutive numbers of wrong watchdog refreshes, the device can decide to assert the RSTB only, or to go in deep Fail-safe mode where only a Power On Reset or a transition on IO_O helps the system to recover.

6.5.2.5 Watchdog error counter

The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The WD error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures that a cyclic “OK/NOK” behavior converges to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable in the INIT_WD register, but only when device is in INIT FS mode.

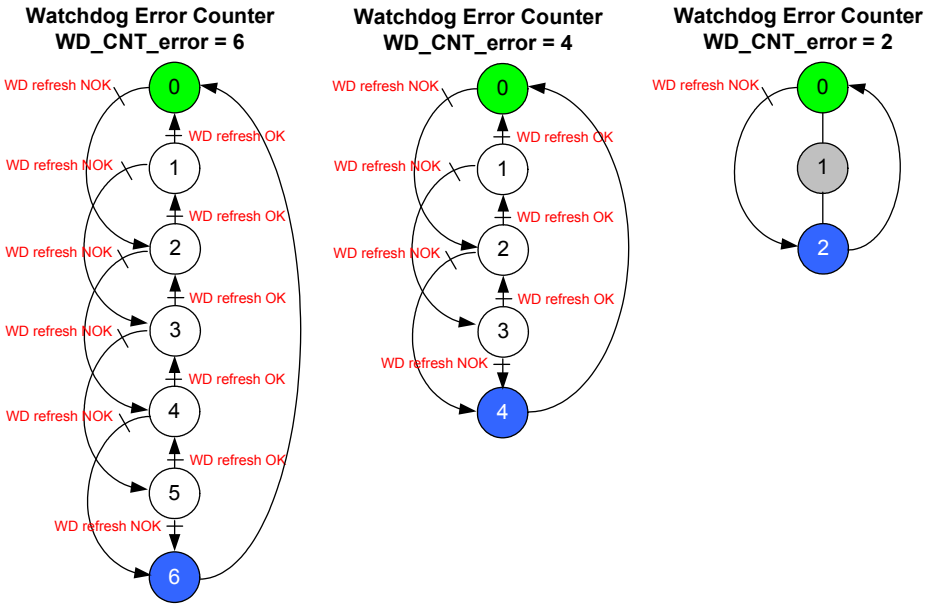


Figure 14. Watchdog error counter configuration (INIT_WD register, bits WD_CNT_error_1:0)

6.5.2.6 Watchdog refresh counter

The watchdog refresh counter is used to decrement the RST error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by “1”. Each time the watchdog refresh counter reaches “6” and if next WD refresh is also good, the RST error counter is decremented by “1” (case with WD_CNT_refresh_1:0 configured at 6).

Whatever the position is in the watchdog refresh counter, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to “0”. To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable in the INIT_WD register, but only when device is in INIT FS mode.

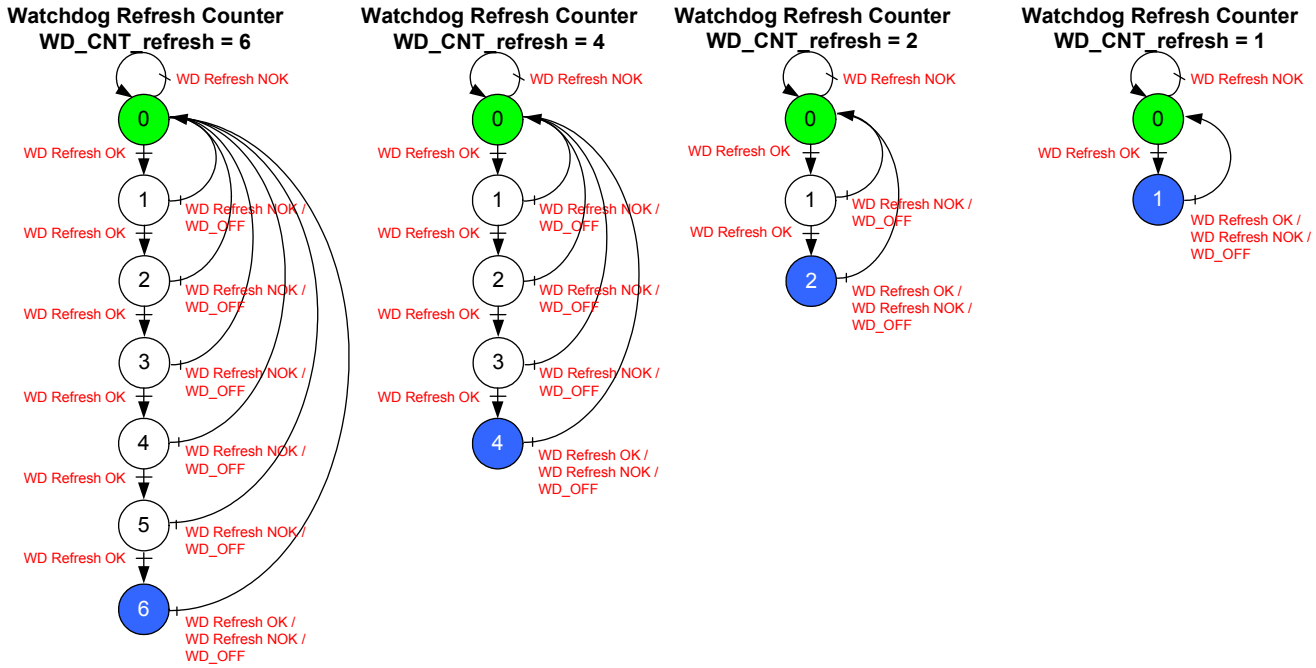


Figure 15. Watchdog refresh counter configuration (INIT_WD register, WD_CNT_refresh_1:0)

Table 10. Watchdog error table

		WINDOW	
		CLOSED	OPEN
SPI	BAD Key	WD_NOK	WD_NOK
	GOOD Key	WD_NOK	WD_OK
	None (time out)	No_issue	WD_NOK

Any access to the watchdog register during the “closed” watchdog window is considered as a wrong watchdog refresh. Watchdog timeout, meaning no WD refresh during closed or open windows, is considered as a wrong WD refresh.

6.5.3 Reset error counter

The reset error counter manages the reset events and counts the number of resets occurring in the application. This counter is incremented not only for the reset linked to consecutive wrong refresh watchdogs, but also for other sources of reset (undervoltage, overvoltage, external reset). The RST error counter is incremented by 1, each time a reset is generated.

The reset error counter has two output values (intermediate and final). The intermediate output value is used to handle the transition from reset (RSTB is asserted low) to reset and fail where RSTB and FS0B are activated. The final value is used to handle the transition from reset and fail to deep reset and fail (Deep Fail-safe mode), where regulators are off, RSTB and FS0B are activated, and a power on reset or a transition on IO_0 is needed to recover. The intermediate value of the reset error counter is configurable to “1” or “3” using the RSTB_err_FS bit in the INIT FSSM2 register (Table 70).

If RSTB_err_FS is set to “0”, it means the device activates FS0B when the reset error counter reaches level “3”.

If RSTB_err_FS is set to “1”, it means the device activates FS0B when the reset error counter reaches level “1”.

This configuration must be done during INIT FS phase.

The final value of the reset error counter is based on the intermediate configuration.

- RSTB_err_FS = 0 / Intermediate = 3; Final = 6 (Figure 16). When reset error counter reaches 6, the device goes into deep reset and fails.
- RSTB_err_FS = 1 / Intermediate = 1; Final = 2 (Figure 17). When reset error counter reaches 2, the device goes into deep reset and fails.

In any condition, if the RSTB is asserted LOW for a duration longer than eight seconds, the device goes into deep reset and fails.

Conditions leading to an increment of the RSTB error counter, and according to the product configuration are:

- Watchdog error counter = 6
- Watchdog refresh NOK during INIT phase or Watchdog timeout
- IO_23 error detection (FCCU)
- Undervoltage
- Overvoltage
- IO_1 FB_Core Delta
- FS0B shorted to VDD
- SPI DED
- Reset request by the SPI
- External reset

Conditions leading to a transition go to FS, according to the product configuration are:

- IO_01/IO_23/IO_45 error detection
- Undervoltage
- Overvoltage
- IO_1 FB_Core Delta
- Analog BIST fail
- SPI DED
- RSTB shorted to high

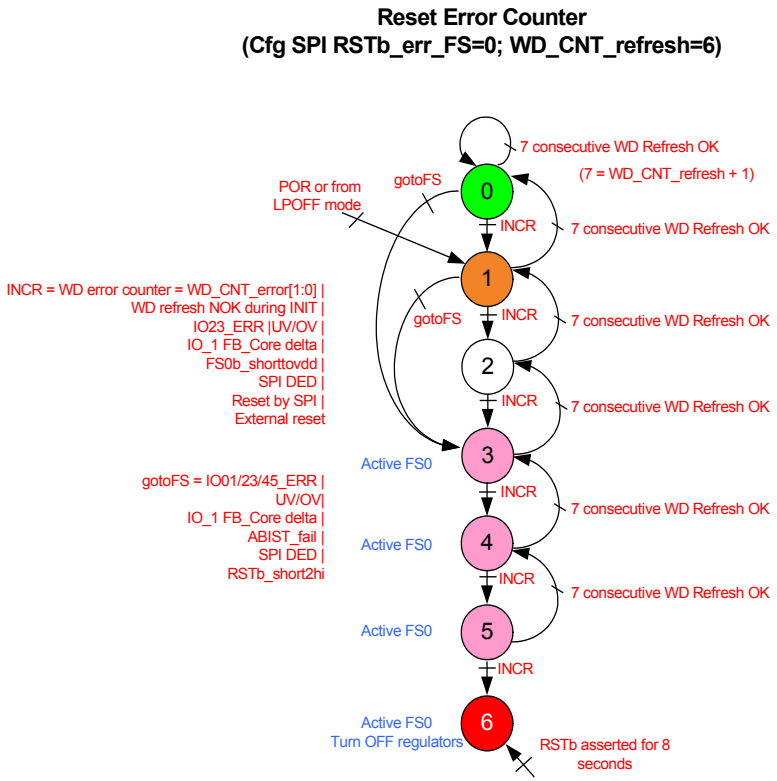


Figure 16. RSTB error counter (RSTB_err_FS = 0)

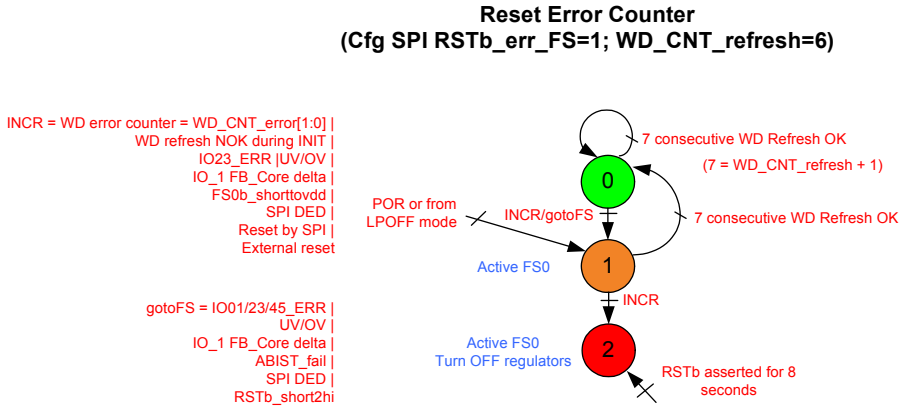


Figure 17. RSTB error counter(RSTB_err_FS = 1)

6.5.3.1 RST error counter at start-up or resuming from LPOFF mode

At start-up or when resuming from LPOFF mode the reset error counter starts at level 1 and FS0B is asserted low. To remove the activation of FS0B, the RST error counter must go back to value “0” (seven consecutive good watchdog refresh decreases the reset error counter down to 0) and a right command is sent to FS_OUT register (Figure 20).

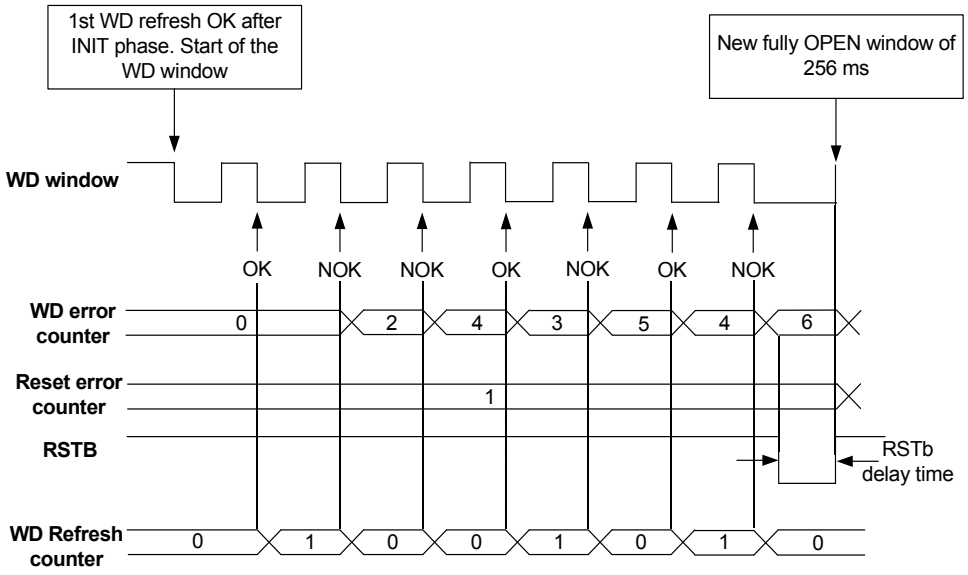


Figure 18. Example of WD operation generating a reset (WD_error_cnt = 6)

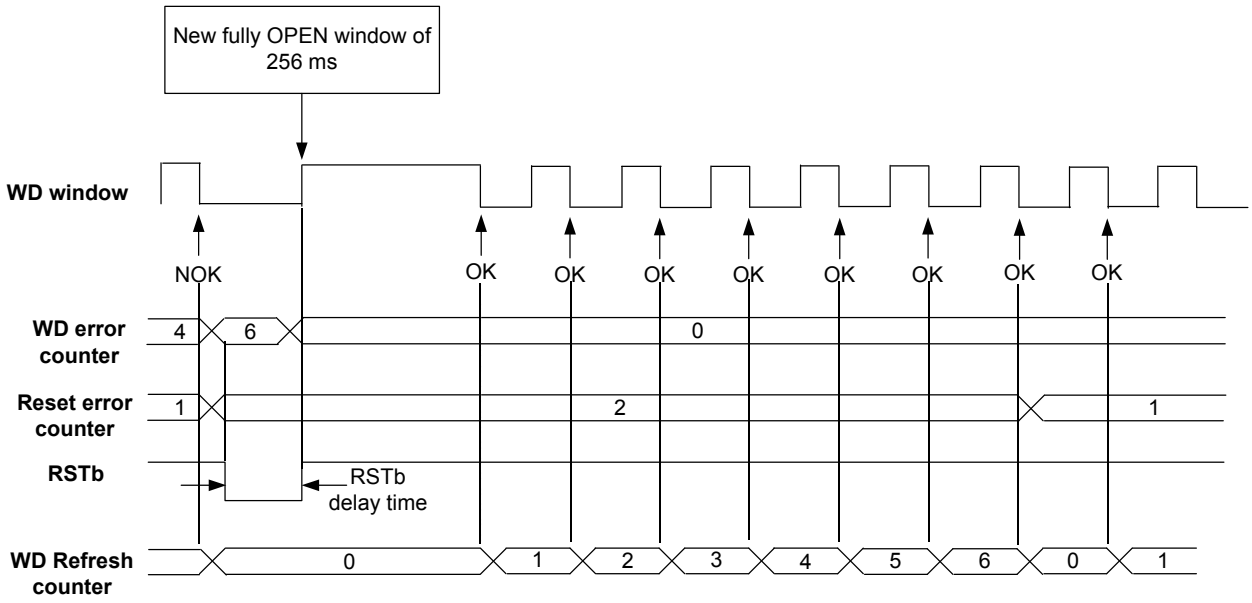


Figure 19. Example of WD operation leading a decrement of the reset error counter (WD_resfresh_cnt = 6)

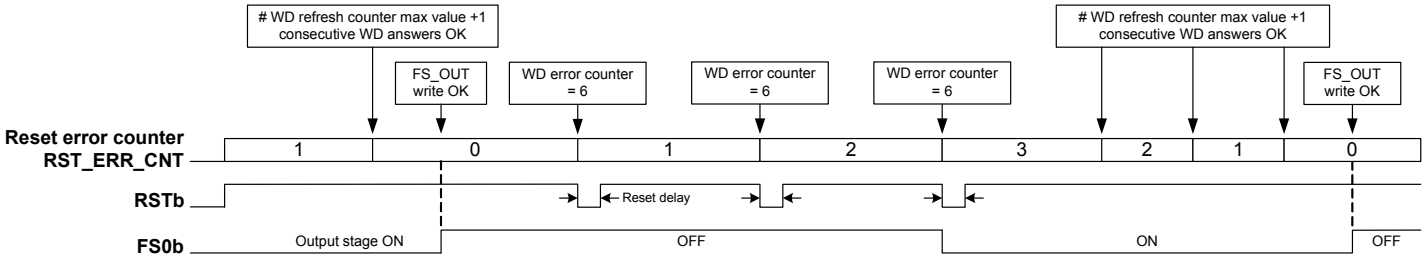


Figure 20. Reset error counter and FS0B deactivation sequence (RSTB_err_FS = 0 & WD_CNT_error1:0 = 6)

6.5.4 Fail-safe output (FS0B) deactivation

When the fail-safe output FS0B is asserted low by the device due to a fault, some conditions must be validated before allowing the FS0B pin to be deactivated by the device. These conditions are:

- Fault is removed
- Reset error counter must be at “0”
- FS_OUT register must be filled with the right value.

6.5.4.1 Faults triggering FS0B activation

The activation of the FS0B is clearly dependent on the product configuration, but the following items can be settled:

- IO_01/IO_23/IO_45 error detection
- Undervoltage
- Overvoltage
- IO_1 FB_Core Delta
- Analog BIST fail (not configurable)
- SPI DED (not configurable)
- RSTB shorted to high (not configurable)
- RSTB error counter level

6.5.5 SPI DED

Some SPI registers affect some safety critical aspects of the fail-safe functions, and thus are required to be protected against SEU (Single Event Upset). Only fail-safe registers are concerned. During INIT FS mode, access to fail-safe registers for product configuration is open. Then once the INIT FS phase is over, the Hamming circuitry is activated to protect registers content.

At this stage, if there is 1 single bit flip, the detection is made due to hamming code, and the error is corrected automatically (fully transparent for the user), and a flag is sent. If there are two errors (DED - Dual Error Detection), the detection is made due to hamming code but detected errors cannot be corrected. The flag is sent, RSTB and FS0B are activated.

6.5.6 FS_OUT register

When the fault is removed and the reset error counter changes back to level “0”, a right word must be filled in the FS_OUT register. The value is dependant on the current WD_LFSR. LSB and MSB must be swapped and negative operation per bit must be applied.

WD_LFSR_7:0=	b7	b6	b5	b4	b3	b2	b1	b0
FS_OUT_7:0 =	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$

Figure 21. FS_OUT register based on LFSR value

6.6 Input voltage range

Due to the flexibility of the pre-regulator, the device can cover a wide battery input voltage range. However, a more standard voltage range can still be covered using only the Buck configuration.

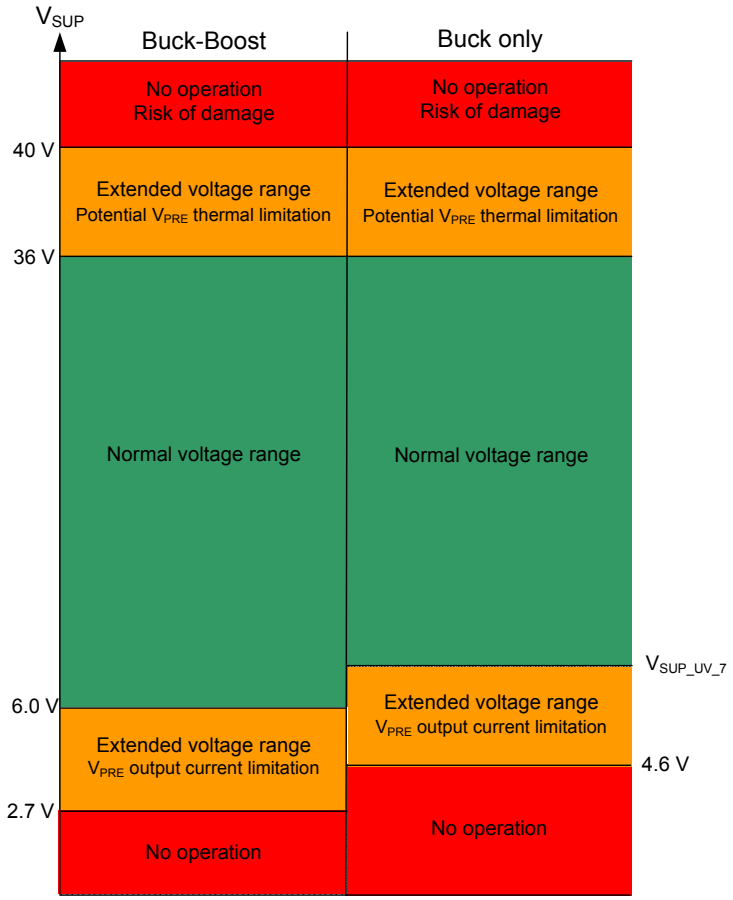


Figure 22. Input voltage range

- Thermal dissipation must be checked based on application use case to maintain junction temperature (T_J) <150 °C
- Buck only, $V_{SUP} < V_{SUP\_UV\_7}$:

CAN communication is guaranteed for V_{SUP} > 6.0 V.

For V_{CCA} and V_{AUX} 5.0 V configuration, undervoltage triggers at low V_{SUP} (refer to $V_{CCA\_UV\_5}$ and $V_{AUX\_UV\_5}$).

6.7 Power management operation

A thermal sensor is implemented as close as possible to the pass transistor of each regulator (VPRE, VCORE, VCCA, VCAN) and an associated individual thermal shutdown (TSD) protect these regulators independently. When the TSD threshold of a specific regulator is reached, this regulator only is switched OFF and the information is reported in the main state machine. The regulator restarts automatically when the junction temperature of the pass transistor decrease below the TSD threshold.

6.7.1 VPRE voltage pre-regulator

A highly flexible SMPS pre-regulator is implemented in the FS6407/FS6408. Depending on the input voltage requirement, the device can be configured as “non-inverting buck-boost converter” (Figure 24) or “standard buck converter” (Figure 23). An external logic level MOSFET (N-type) is required to operate in “non-inverting buck-boost converter”. The connection of the external MOSFET is detected automatically during the start-up phase.

The converter operates in Current Control mode in any configuration. The high-side switching MOSFET is integrated to make the current control easier. The PWM frequency is fixed at 440 kHz typical. The compensation network is fully integrated. VPRE output voltage is regulated between 6.0 V and 7.0 V.

If the full current capability is not used for VCORE, VCCA, VAUX and CAN_5V, additional external LDO can be connected to VPRE to fulfill application needs while the current load remains below the maximum current capability in all conditions.

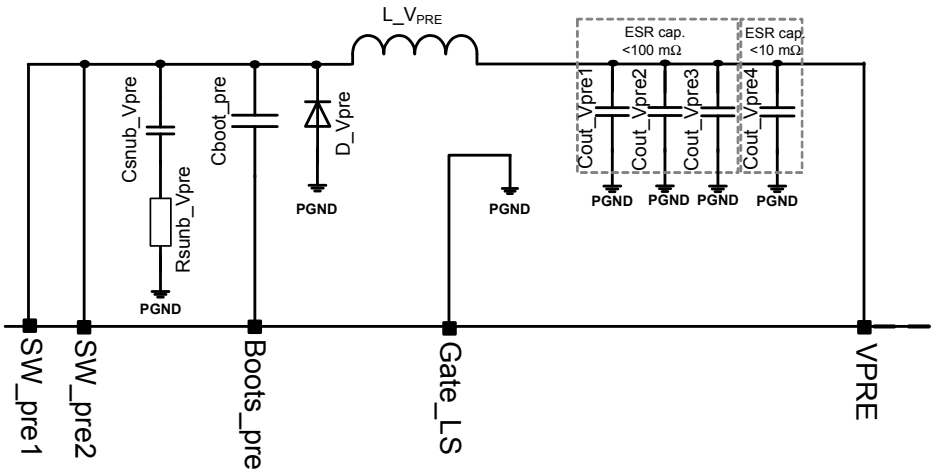


Figure 23. Pre-regulator: buck configuration

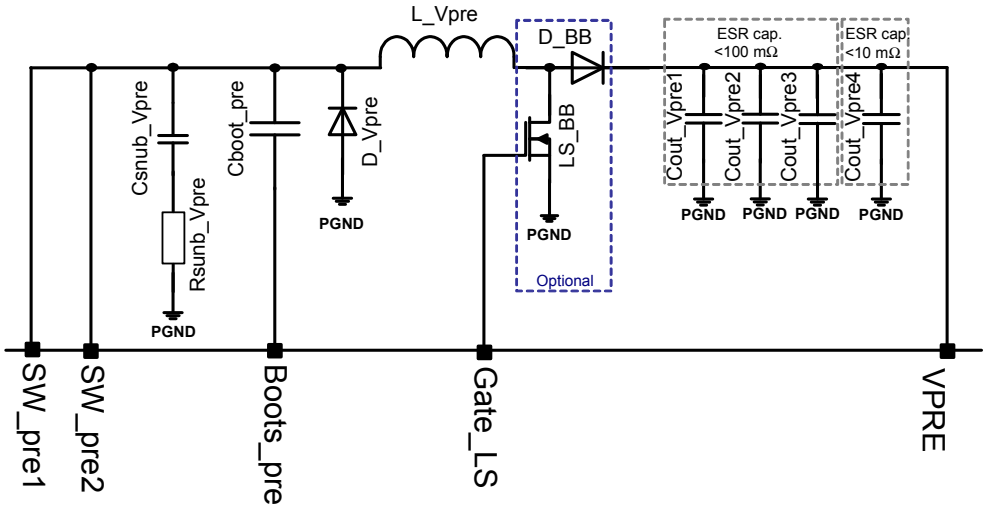


Figure 24. Pre-regulator: buck boost configuration

When the converter is set up to work in boost mode at low V_{SUP}, the transition between buck and boost mode is automatically handled by the device at $V_{SUP\_UV\_7}$ threshold. Transition between buck mode and boost mode is based on hysteresis (Figure 25).

- When VSUP > $V_{SUP\_UV\_7}$, the converter works in Buck mode and the VPRE output is regulated at 6.5 V typical
- When VSUP < $V_{SUP\_UV\_7}$, the converter works in Boost mode and the VPRE output is regulated at 6.3 V typical

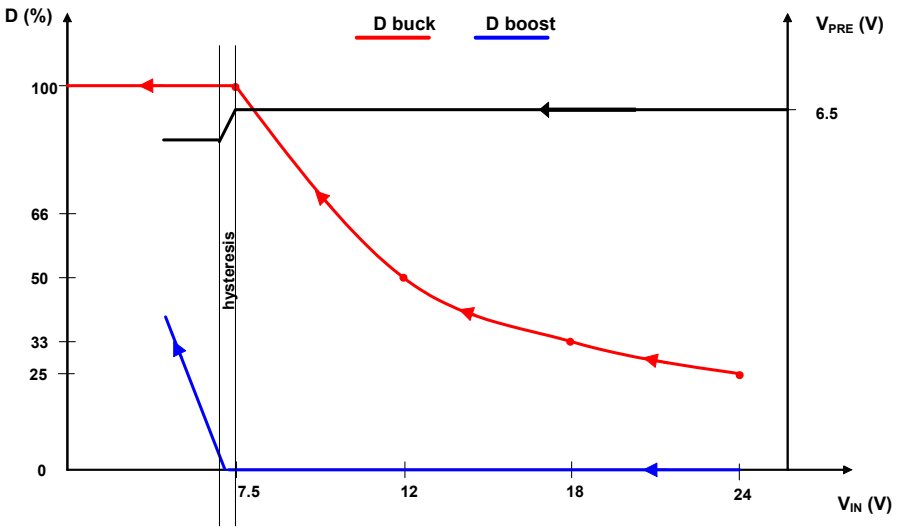


Figure 25. Transition between buck and boost

6.7.1.1 Power up and power down sequence

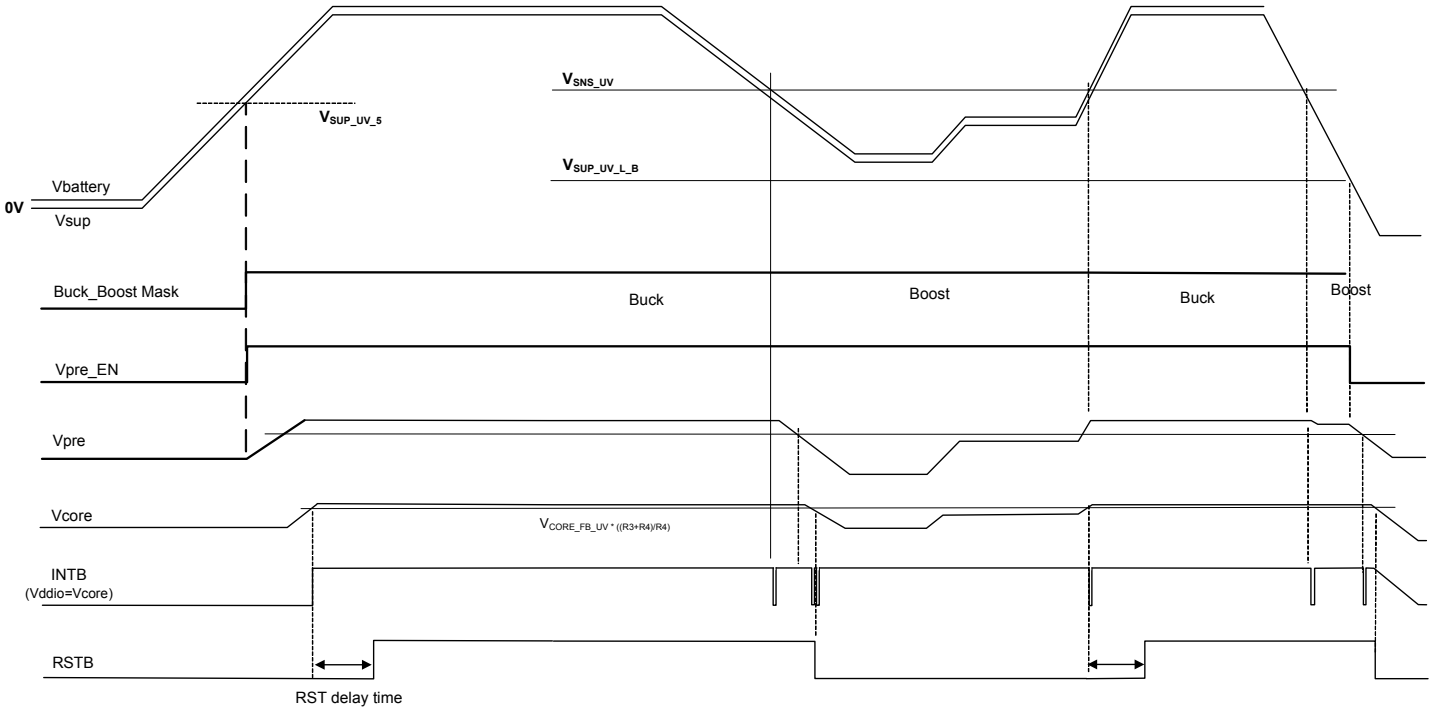


Figure 26. Buck configuration power up and power down

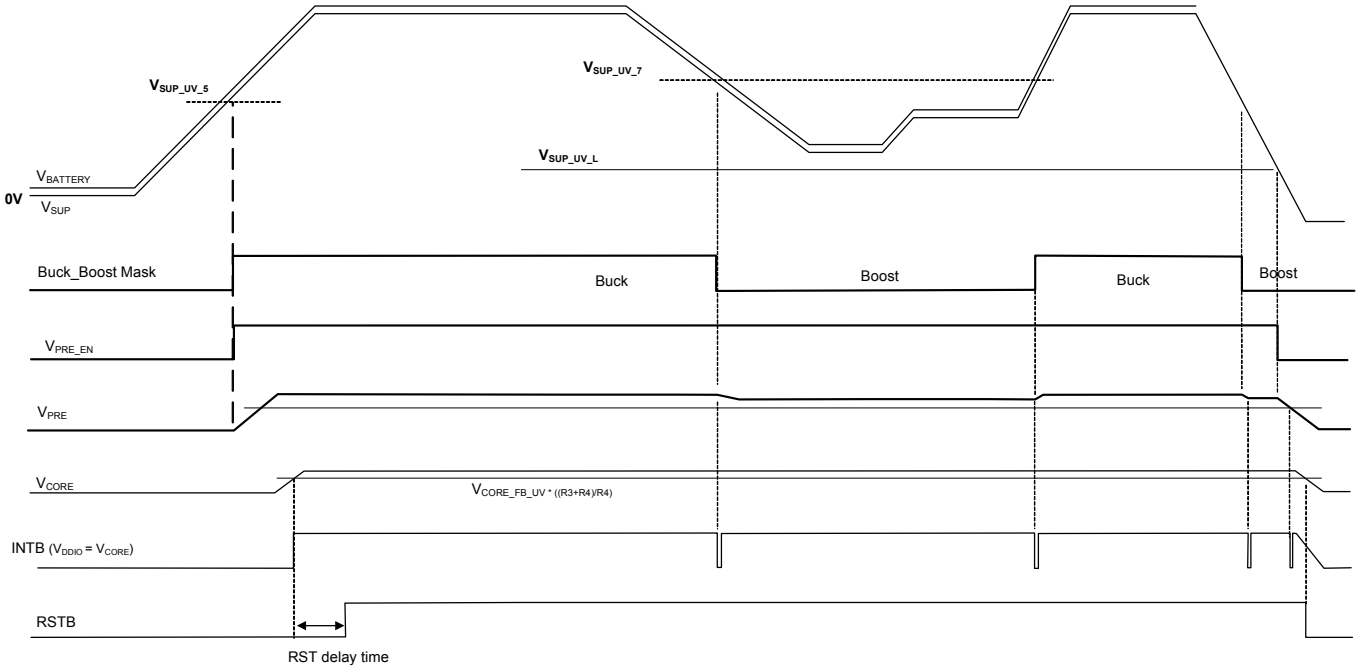


Figure 27. Buck boost configuration power-up and power-down

6.7.1.2 Low VSUP management

When VPRE is set up to work in buck only mode, the application can work down to VSUP = $V_{SUP\_UV\_L\_B}$ = 4.6V with a minimum of 500 mA current guaranteed on VPRE.

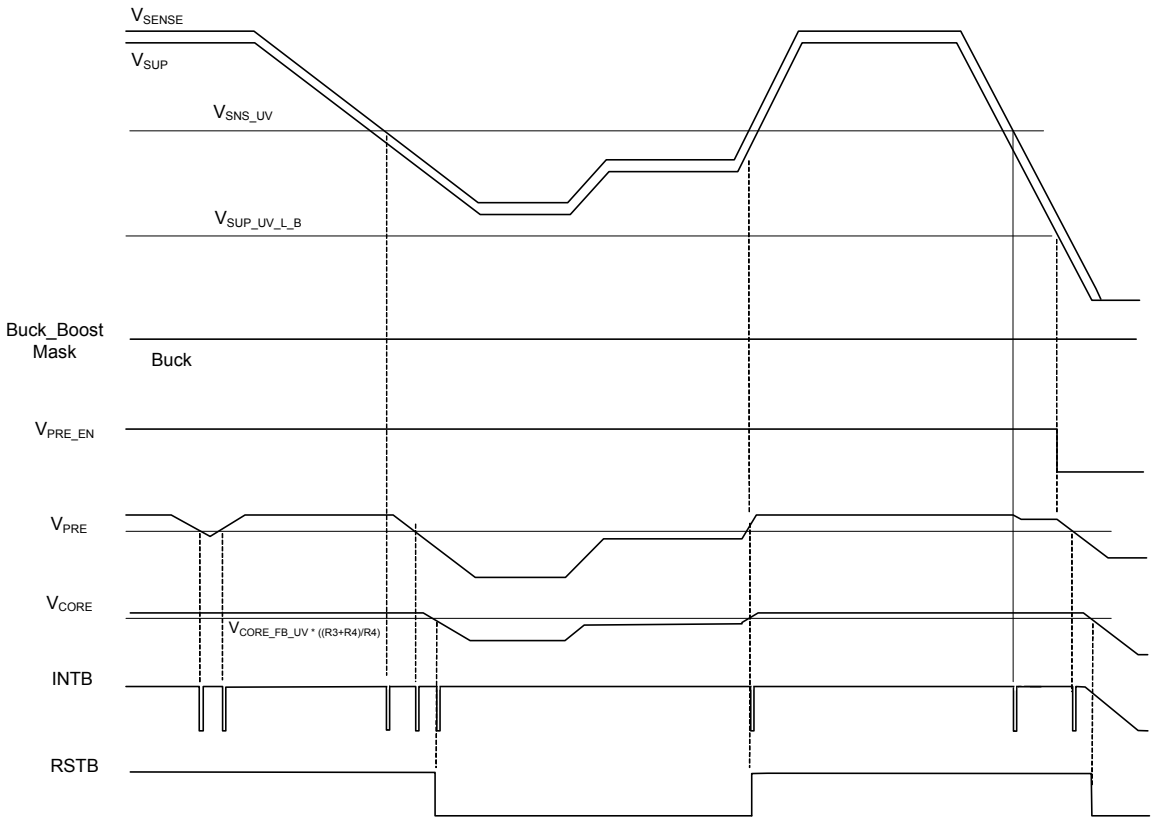


Figure 28. Behavior at low V_{SUP} (buck configuration)

When VPRE is set up to work in boost mode, the application can work down to V_{SUP} = $V_{SUP\_UV\_L}$ = 2.7 V with a minimum of 300 mA current guaranteed on VPRE.

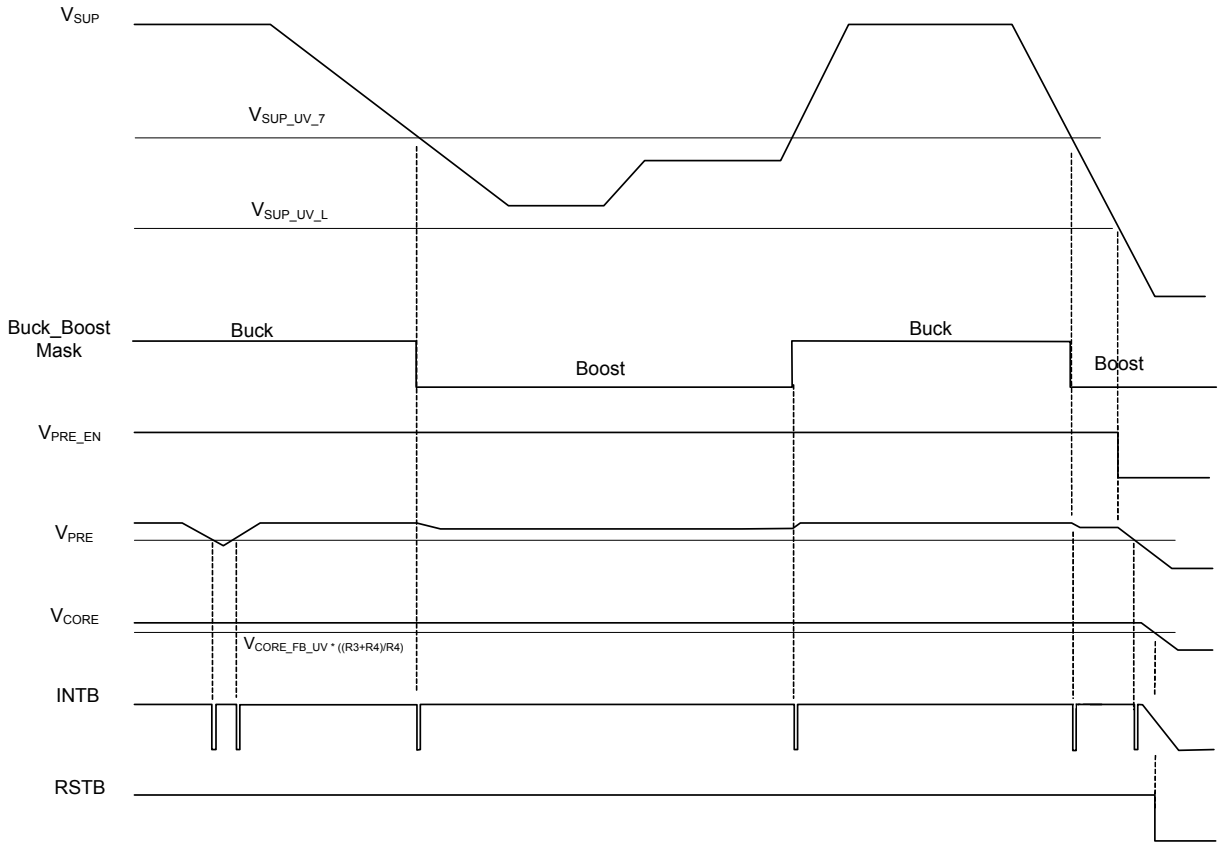


Figure 29. Behavior at low V_{SUP} (buck boost configuration)

6.7.1.3 Light load condition

In order to improve the converter efficiency and avoid any unwanted output voltage increase, the VPRE voltage regulator operates in Pulse Skipping mode during light load condition.

The transition between Normal mode and Pulse Skipping mode is based on the comparison between the error amplifier output (EA_out) and pre-defined thresholds $V_{PRE\_LL\_H}$ and $V_{PRE\_LL\_L}$. When the error amplifier output reaches $V_{PRE\_LL\_L}$, VPRE high-side transistor is switched OFF. When the error amplifier output reaches $V_{PRE\_LL\_H}$, VPRE high-side transistor is switched ON again for the next switching period (Figure 30).

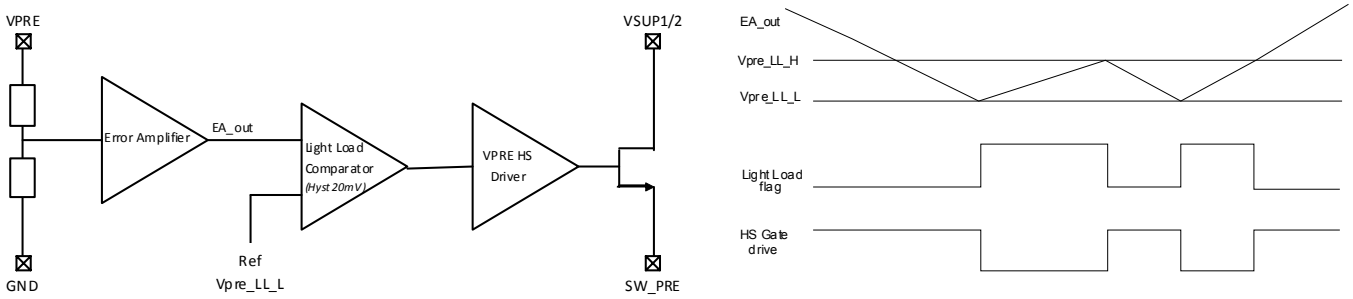


Figure 30. Description of light load condition

6.7.1.4 Overcurrent detection and current limitation

6.7.1.4.1 Overcurrent protection:

In order to ensure the integrity of the high-side MOSFET, an overcurrent detection is implemented. The regulator is switched OFF by the main state machine when the overcurrent detection threshold I_{PRE_OC} is reached three consecutive times. The overcurrent detection is blanked when the pass transistor is switched ON during T_{PRE_OC} to avoid parasitic switch OFF of the high-side gate driver.

The VPRE output voltage decrease causes an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device in Fail-safe state. The overcurrent protects the regulator in case of SW_PRE pin shorted to GND. The overcurrent works in Buck mode only.

6.7.1.4.2 Current limitation:

A current limitation is also implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below I_{PRE_LIM}. The current limitation is blanked when the pass transistor is switched ON during $T_{PRE\_BLK\_LIM}$ to allow short-circuit detection on SW_PRE pin.

When I_{PRE_LIM} threshold is reached during Buck mode, the high-side integrated MOSFET is switched OFF. When I_{PRE_LIM} threshold is reached during Boost mode, the external low-side MOSFET is switched OFF. In both cases, the MOSFET is not switched ON again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the VPRE output voltage to fall down gradually. This may cause an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device into Fail-safe state. The current limitation does not switch OFF the regulator. The current limitation protects the regulator when VPRE pin is shorted to GND.

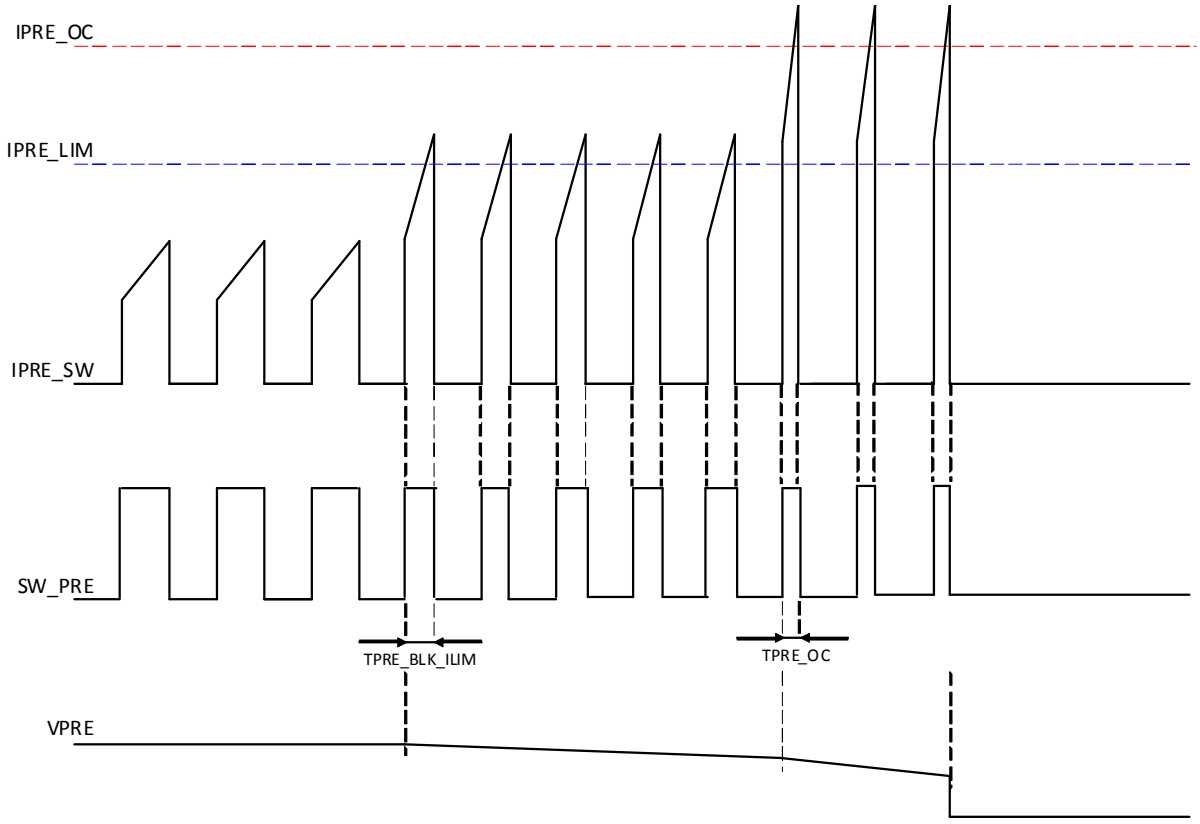


Figure 31. Overcurrent and current limitation scheme

6.7.1.5 VPRE voltage monitoring

The overvoltage detection switches OFF the regulator. The undervoltage detector is disabled when the regulator is switched OFF reporting an undervoltage. Diagnostic is reported in the dedicated register and generate an Interrupt.

The undervoltage detection does not switches OFF the regulator. However, V_{PRE} decrease may induce an undervoltage on a regulator attached to V_{PRE} (VCORE, VCCA, VAUX, or CAN_5V), and bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

6.7.1.6 V_{PRE} efficiency

V_{PRE} efficiency versus current load is given for information based on typical external component criteria described in the table close to the graph and at three different V_{SUP} voltages (24 V, 32 V, and 36 V) covering typical industrial operating range. The efficiency is valid in Buck mode only and above 200 mA load on VPRE to be in continuous mode in the 22 µH inductor. The efficiency is calculated and has to be verified by measurement at application level.

Ext. Devices	
Cout	57 µF
ESR Cout	100.0 mΩ
L coil	22.0 µH
DCR coil	60.0 mΩ
Vdiode	0.35 V
MOSFET switch	
Rdson	200.0 mΩ
Cg	600 pF
Tsw_on	30.00 ns
Tsw_off	30.00 ns
Overdrive	10.0 V
Converter	
Vpre	6.50 V
Freq	440 kHz

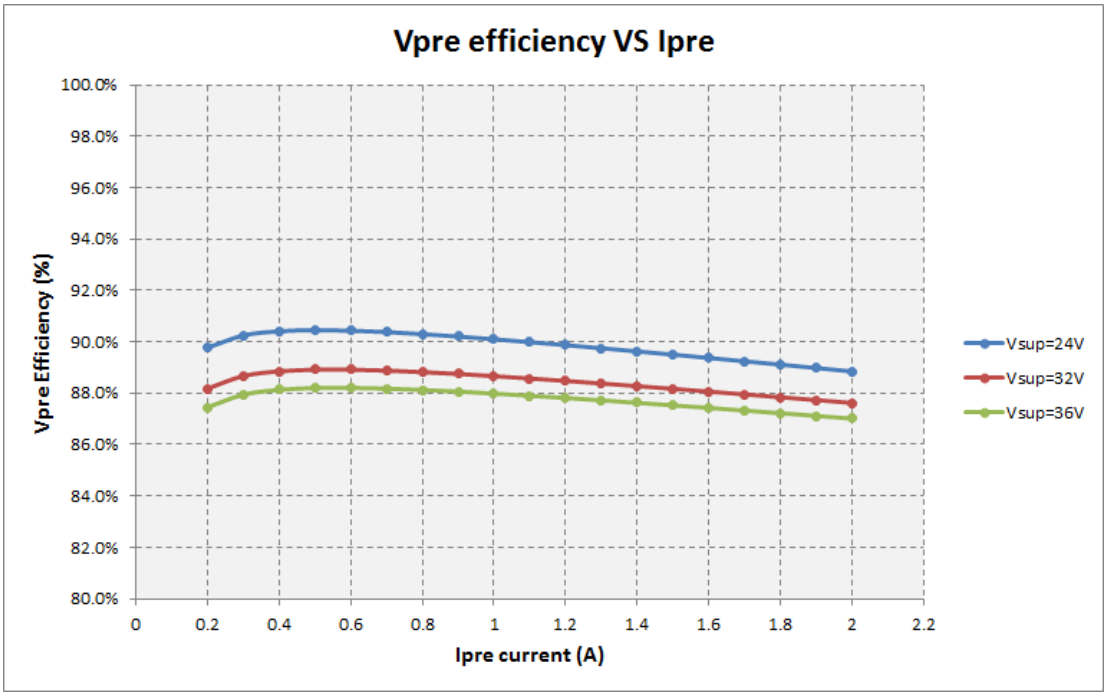


Figure 32. V_{PRE} efficiency

6.7.2 VCORE voltage regulator

This voltage regulator is a step-down DC-DC converter operating in Voltage Control mode. The high-side switching MOSFET is integrated in the device and the PWM frequency is fixed at 2.4 MHz typical. The output voltage is configurable from 1.2 V to 3.3 V range and adjustable around these voltages with an external resistor divider (R3/R4) connected between V_{CORE} and the feedback pin (FB_CORE) (Figure 33).

VCORE = V_{CORE_FB} x ((R3 + R4) / R4)

The voltage accuracy is ±2.0% (without the external resistor bridge R3/R4 accuracy) and the max output current is 1.5 A. The stability of the overall converter is done by an external compensation network (R1/C1/R2/C2) connected to the pin COMP_CORE. It is recommended to use 1.0% accuracy resistors and set R4 = 8.06 kΩ and adjust R3 to obtain the final VCORE voltage needed for the MCU core supply.

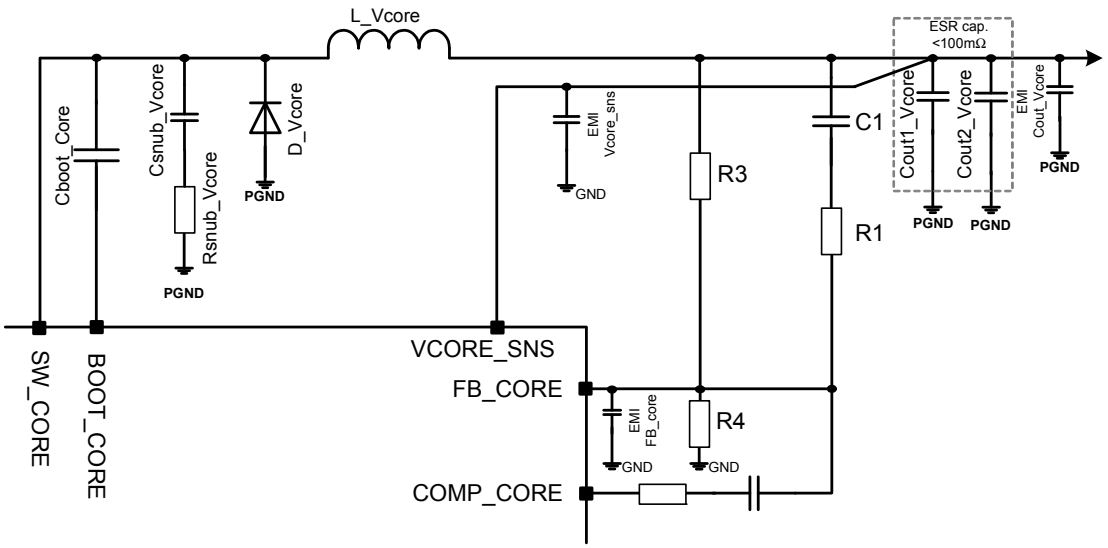


Figure 33. VCORE buck regulator

6.7.2.1 Light load condition

In order to improve the converter efficiency and avoid any unwanted output voltage increase, VCORE voltage regulator operates in Pulse Skipping mode during light load condition. The principle is the same as the VPRE implementation described in details in Light load condition.

6.7.2.2 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below I_{CORE_LIM}. The current limitation is banked when the pass transistor is switched ON during $T_{CORE\_BLK\_LIM}$ to avoid parasite detection. When I_{CORE_LIM} threshold is reached, the high-side integrated MOSFET is switched OFF. The MOSFET is not switched ON again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the VCORE output voltage to fall down gradually, which may cause an undervoltage condition and bring the device into the Fail-safe state. The current limitation does not switch OFF the regulator.

6.7.2.3 Voltage monitoring

The overvoltage detection switches OFF the regulator. The regulator remains ON in case of undervoltage detection. Diagnostic is reported in the dedicated register, generate an Interrupt and may bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

6.7.2.4 V_{CORE} efficiency

V_{CORE} efficiency versus current load is given for information based on typical external component criteria described in the table close to the graph and at two different VCORE voltages (3.3 V, and 1.2 V) covering most of the 32-bit MCU supply range. The efficiency is valid above 200 mA load on V_{CORE} in order to be in continuous mode in the 2.2 µH inductor. The efficiency is calculated and has to be verified by measurement at application level. One of the major contributor degrading the efficiency at V_{CORE} = 1.2 V is the external diode during the recirculation phase. Lower the diode forward voltage (V_F) is, the better the efficiency.

Ext. Devices	
Cout	20 µF
ESR Cout	5.0 mΩ
L coil	2.2 µH
DCR coil	20.0 mΩ
Vdiode	0.35 V
MOSFET switch	
Rdson	200.0 mΩ
Cg	300 pF
Tsw_on	12.00 ns
Tsw_off	12.00 ns
Overdrive	10.0 V
Converter	
Vcore	3.30 V
Freq	2400 kHz

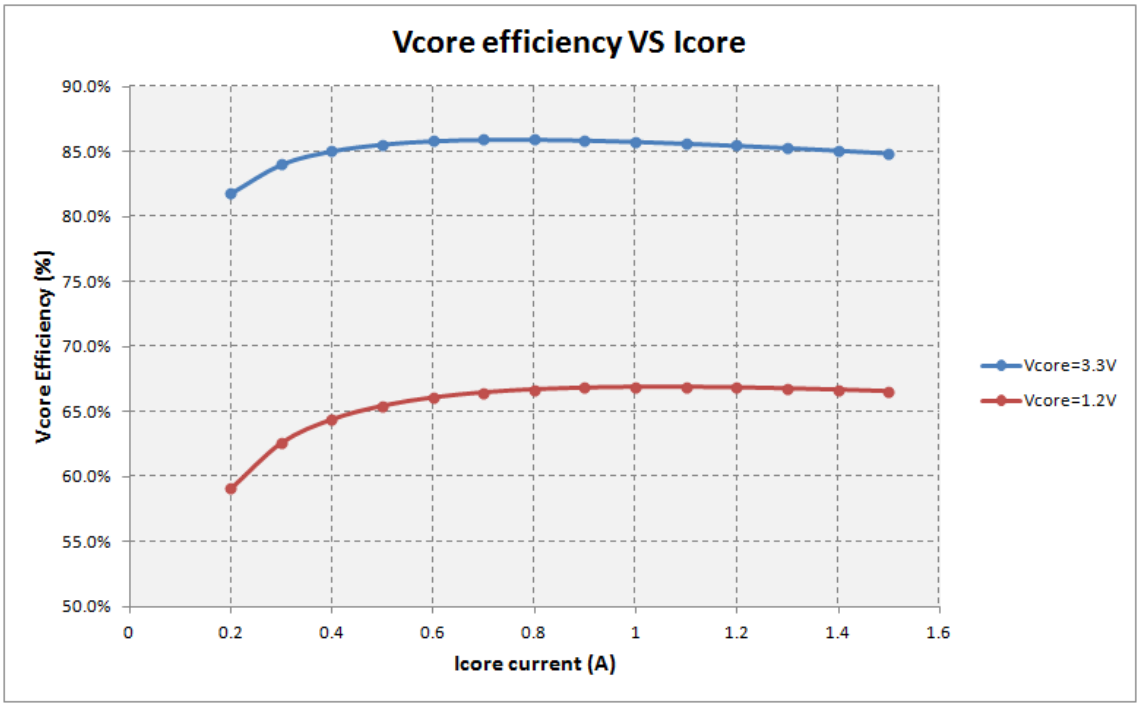


Figure 34. V_{CORE} efficiency

6.7.3 Charge pump and bootstrap

Both switching MOSFETs of VPRE and VCORE SMPS are driven by external bootstrap capacitors. Additionally, a charge pump is implemented to ensure 100% duty cycle for both converters. Each converter uses a 100 nF external capacitor minimum to operate properly.

6.7.4 VCCA voltage regulator

VCCA is a linear voltage regulator mainly dedicated to supply the MCU I/Os, especially the ADC. The output voltage is selectable at 5.0 V or 3.3 V. Since this output voltage can be used to supply MCU I/Os, the output voltage selection is done using an external resistor connected to the SELECT pin and ground if VAUX is used. When VAUX is not used, the resistor is connected between the SELECT pin and VPRE.

When VCCA is used with the internal MOS transistor, VCCA_E pin must be connected to VPRE. The voltage accuracy is ±1.0% for 5.0 V configuration and ±1.5% for 3.3 V configuration with an output current capability at 100 mA.

When VCCA is used with an external PNP transistor to boost the current capability up to 300 mA, the connection is detected automatically during the start-up sequence of the FS6407/FS6408. In such condition, the internal pass transistor is switched OFF and all the current is driven through the external PNP to reduce the internal power dissipation. The output voltage accuracy with an external PNP is reduced to ±3.0% at 300 mA current load. The VCCA output voltage is used as a reference for the auxiliary voltage supply (V_{AUX}) when VAUX is configured as a tracking regulator.

6.7.4.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the internal MOSFET or external PNP transistor. By default, the current limitation threshold is selected based on the auto detection of the external PNP during start up phase.

- When the internal MOSFET transistor is used, the current is limited to $I_{CCA\_LIM\_INT}$ and the regulator is kept ON
- When the external PNP transistor is used, the current is limited to $I_{CCA\_LIM\_OUT}$ and the regulator is switch OFF after a dedicated duration $T_{CCA\_LIM\_OFF}$ under current limitation. A SPI command is needed to restart the regulator.

In case of external PNP configuration only, the lowest current limitation threshold can be selected by SPI in the register INIT VREG 2 instead of the highest one. In order to limit the power dissipation in the external PNP transistor in case of short circuit to GND of VCCA pin, a current limitation foldback scheme is implemented to reduce the current limitation to $I_{CCA\_LIM\_FB}$ when V_{CCA} is below $V_{CCA\_LIM\_FB}$.

6.7.4.2 Voltage monitoring

The overvoltage detection switches OFF the regulator. The regulator remains ON during undervoltage detection. A diagnostic is reported in the dedicated register, generating an Interrupt, and may bring the application into Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

6.7.5 VAUX voltage regulator

VAUX is a highly flexible linear voltage regulator which can be used either as an auxiliary supply dedicated to additional device in the ECU or as a sensor supply. An external PNP transistor must be used (no internal current capability). If VAUX is not used in the application, the VAUX_E and SELECT pins must be connected to VPRE to not populate the external PNP, as described in Figure 51.

If VAUX is used as an auxiliary supply, the output voltage is selectable between 5.0 V and 3.3 V. Since this voltage rail can be used to supply MCU IOs, the selection is done with an external resistor connected between the SELECT pin and ground. In such case, the voltage accuracy is ±3.0% with a maximum output current capability at 300 mA. If VAUX is used as a sensor supply rail, the output voltage is selectable between 5.0 V and 3.3 V. VCCA can be used as reference for the sensor supply used as tracker. The selection is done during the INIT phase and secured (bit $V_{AUX\_TRK\_EN}$ in the register INIT VREG2). The tracking accuracy is ±15 mV.

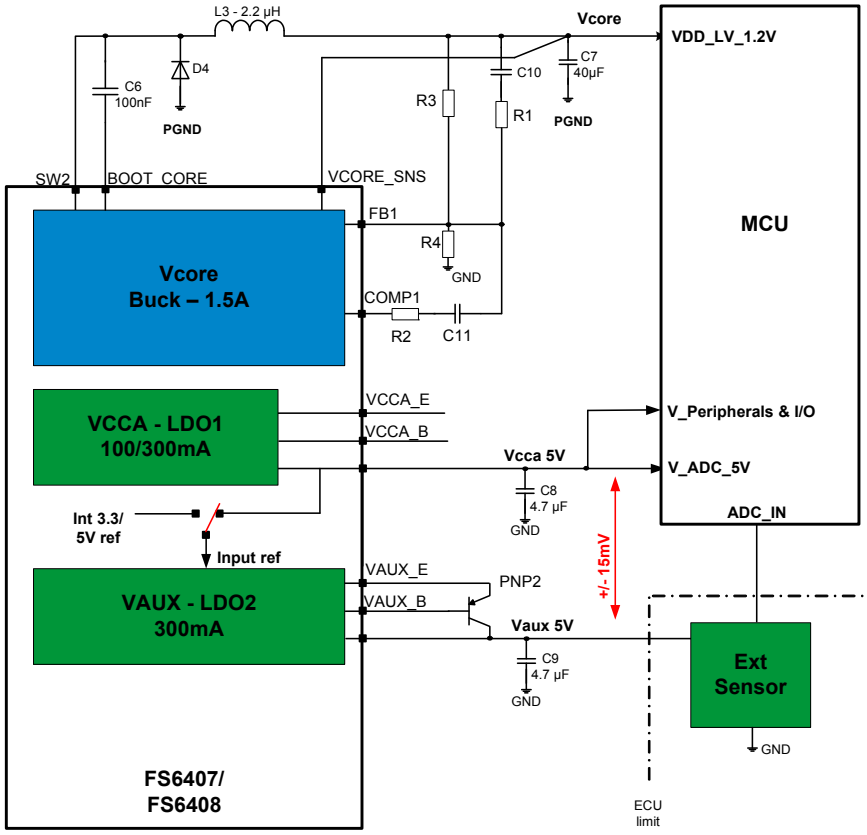


Figure 35. Example of V_{AUX} used in tracker mode

6.7.5.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the external PNP transistor. The current is limited to I_{AUX_LIM} and the regulator is switch OFF after a dedicated duration $T_{AUX\_LIM\_OFF}$ under current limitation. A SPI command is needed to restart the regulator. To limit the power dissipation in the external PNP transistor in case of a short-circuit to GND of the VAUX pin, a current limitation foldback scheme is implemented to reduce the current limitation to $I_{AUX\_LIM\_FB}$ when V_{AUX} is below $V_{AUX\_LIM\_FB}$.

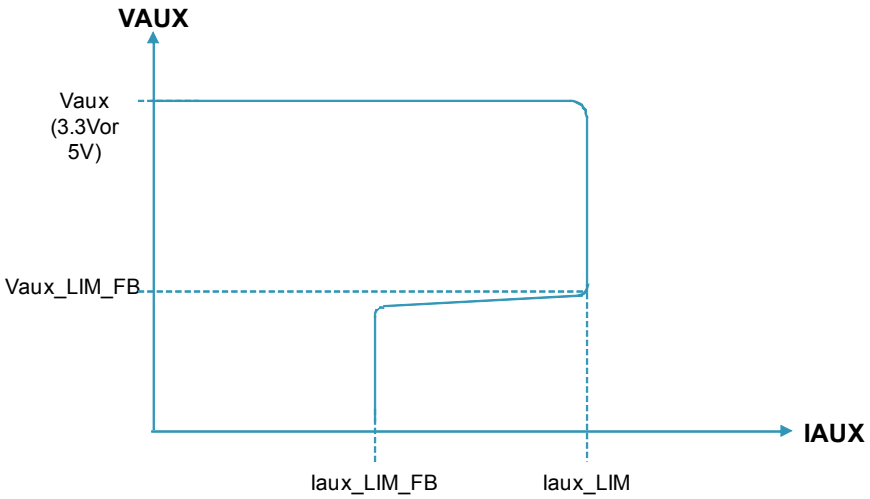


Figure 36. V_{AUX} current limitation scheme with foldback mechanism

6.7.5.2 Voltage monitoring

The overvoltage detection switches OFF the regulator. The regulator remains ON in case of an undervoltage detection. A diagnostic is reported in the dedicated register, generating an Interrupt, and may bring the application into Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

6.7.6 CAN_5V voltage regulator

The CAN_5V voltage regulator is a linear regulator fully dedicated to the internal HSCAN interface. By default, the CAN_5V regulator and the undervoltage detector are enabled, and the overvoltage detector is disabled. The overvoltage detector can be enabled by the SPI during INIT_MAIN sate.

If the overvoltage detector is enabled, the CAN_5V regulator switches OFF when an overvoltage is detected. The undervoltage detector is disabled when the regulator is switched OFF reporting an undervoltage. A diagnostic is reported in the dedicated register, generating an Interrupt. The CAN_5V regulator is not a safety regulator. Consequently, the CAN_5V voltage monitoring (overvoltage, undervoltage) never asserts RSTB or the FS0B Fail-safe pins.

If the FS6407/FS6408 internal CAN transceiver is not used in the application, the CAN_5V regulator can be used to supply an external load, provided the current load remains below the maximum current capability in all conditions. In that case, the internal CAN transceiver must be put in Sleep mode without wake-up capability.

6.7.7 Power dissipation

The FS6407/FS6408 provides high performance SMPS and Linear regulators to supply high end MCU in industrial applications. Each regulator can deliver:

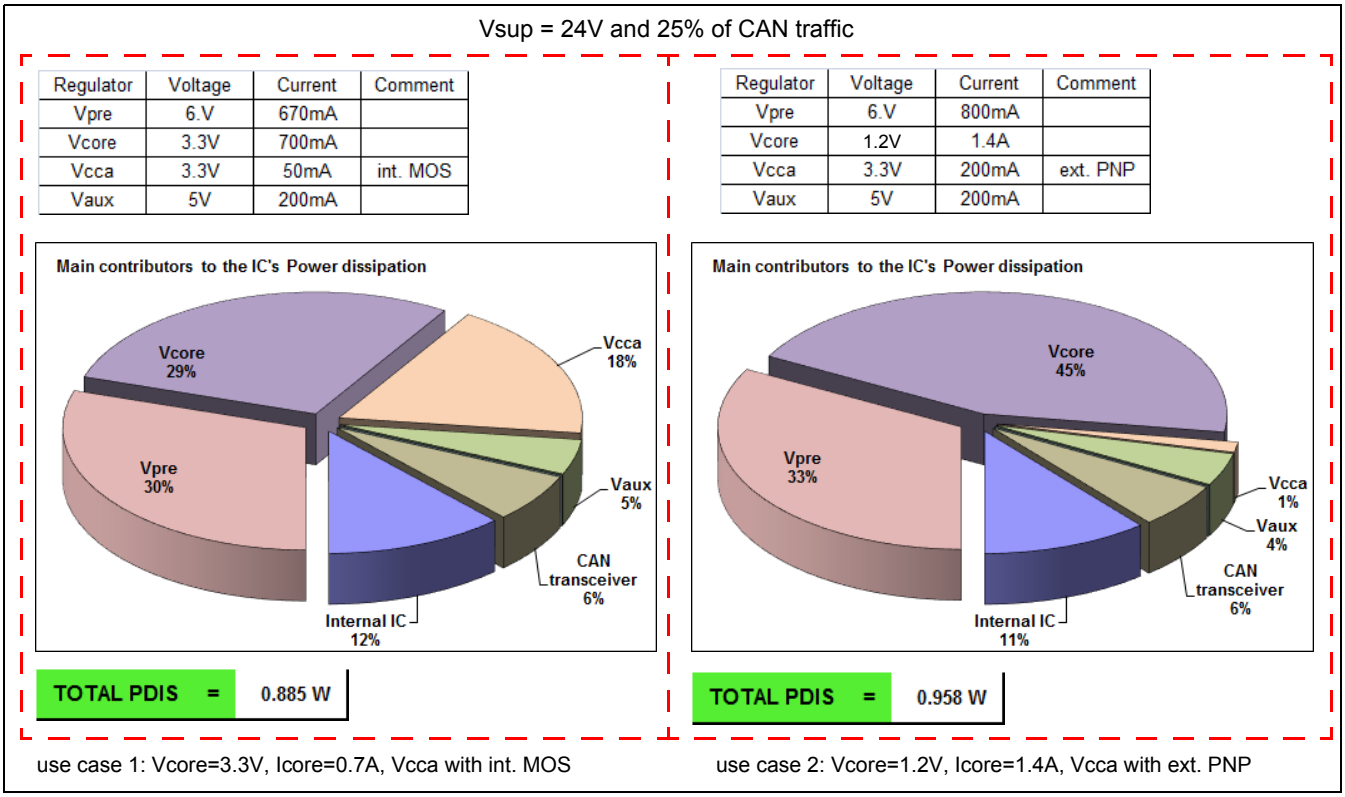
- V_{PRE} (6. 5V) up to 2.0 A
- V_{CORE} (from 1.2 V to 3.3 V range) up to 0.8 A (FS6407) or up to 1.5 A (FS6408)
- V_{CCA} (3.3 V or 5.0 V) up to 100 mA (with internal MOS) or up to 300 mA (with external PNP)
- V_{AUX} (3.3 V or 5.0 V) up to 300 mA (with external PNP)
- V_{CAN} (5.0 V) up to 100 mA

A thermal dissipation analysis has to be performed based on application use case to ensure the maximum silicon junction temperature does not exceed 150 °C.

Two use cases covering the two main V_{CORE} voltage configurations are provided in Figure 37.

- use case 1: V_{CORE} = 3.3 V, I_{CORE} = 0.7 A, V_{CCA} with int. MOS
- use case 2: V_{CORE} = 1.2 V, I_{CORE} = 1.4 A, V_{CCA} with ext. PNP

Both use cases have a total internal power dissipation below 0.9 W. A junction to ambient thermal resistivity of 30 °C/W allows the application to work up to 125 °C ambient temperature. A good soldering of the package expose pad is highly recommended to achieve such thermal performance.



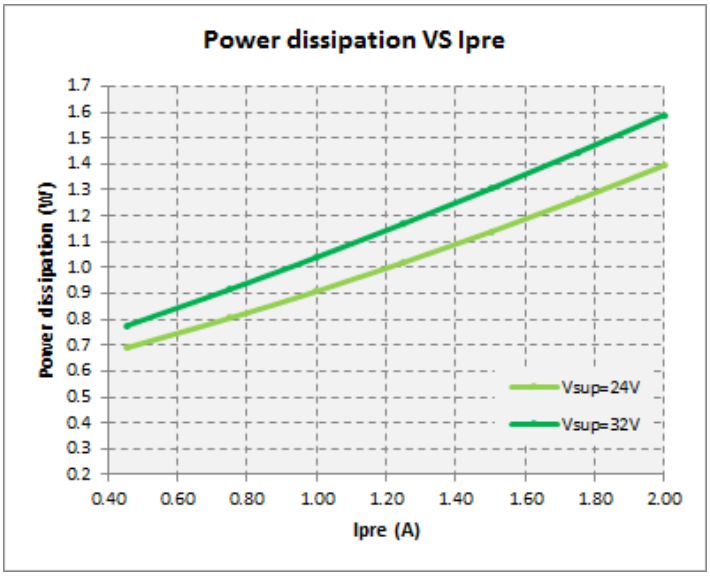
1) CAN transceiver dissipation includes CAN_5V regulator dissipation.

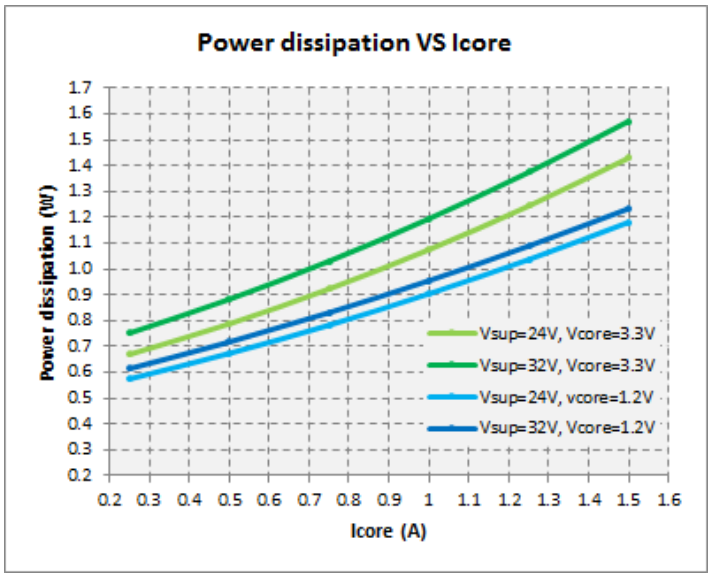
2) 25% CAN traffic means the CAN bus is dominant for 25% of time and recessive for the remaining 75%.

Figure 37. Power dissipation use case

The main contributors to the device power dissipation are VPRE, VCORE, and VCCA (when used with internal PMOS) regulators. In comparison, the power dissipation from the Internal IC, VAUX and CAN transceiver are negligible. VPRE power dissipation is mainly induced by the loading of the regulators it is supplying, mainly VCORE, VCCA and VAUX, which are application dependant. The total device power dissipation, depending on the variation of these three regulators, is detailed in Figure 38 with the environmental conditions in the associated table.

	Pdis VS Icore	Pdis VS Icca	Pdis VS Ipre
Vpre	6.5V	6.5V	6.5V
Ipre	Icore + Icca + Iaux + Ican	Icore + Icca + Iaux + Ican	From 0.5 to 2A
Vcore	3.3V and 1.2V	3.3V	3.3V
Icore	from 0.25 to 1.5A	0.7A	0.3A
Vcca	3.3V	3.3V and 5V	3.3V
Icca	50mA	20 to 100mA	50mA
Vaux	3.3V	3.3V	3.3V
Iaux	200mA	200mA	200mA
CAN_5V	5V	5V	5V
Ican	33mA	33mA	33mA





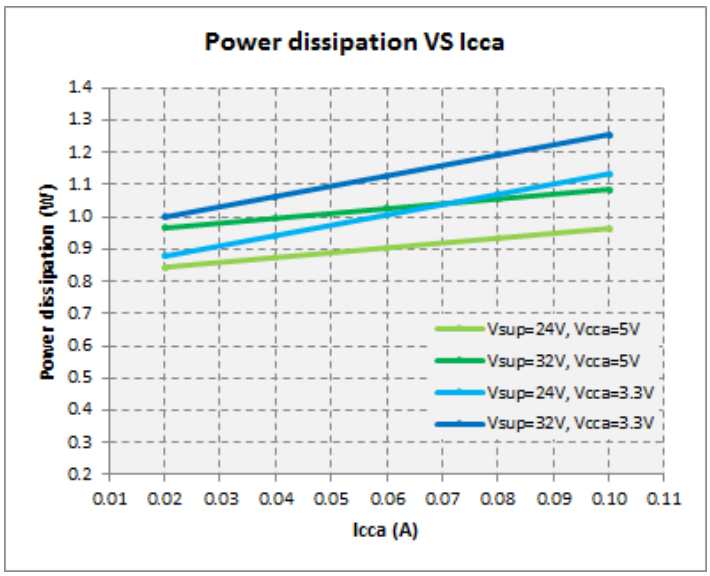


Figure 38. Power dissipation versus I_{CORE}, I_{CCA}, or I_{PRE}

6.7.8 Start-up sequence

To provide a safe and well known start-up sequence, the FS6407/FS6408 includes an undervoltage lock-out. This undervoltage lock-out is only applicable when the device is under a Power-On-Reset condition, which means the initial condition is VSUP < $V_{SUP\_UV\_L}$ (i.e. below 2.7 V max). In all the other conditions (i.e. LPOFF), the device is able to operate (and therefore to restart) down to $V_{SUP\_UV\_L}$. The other different voltage rails automatically start, as described in Figure 39.

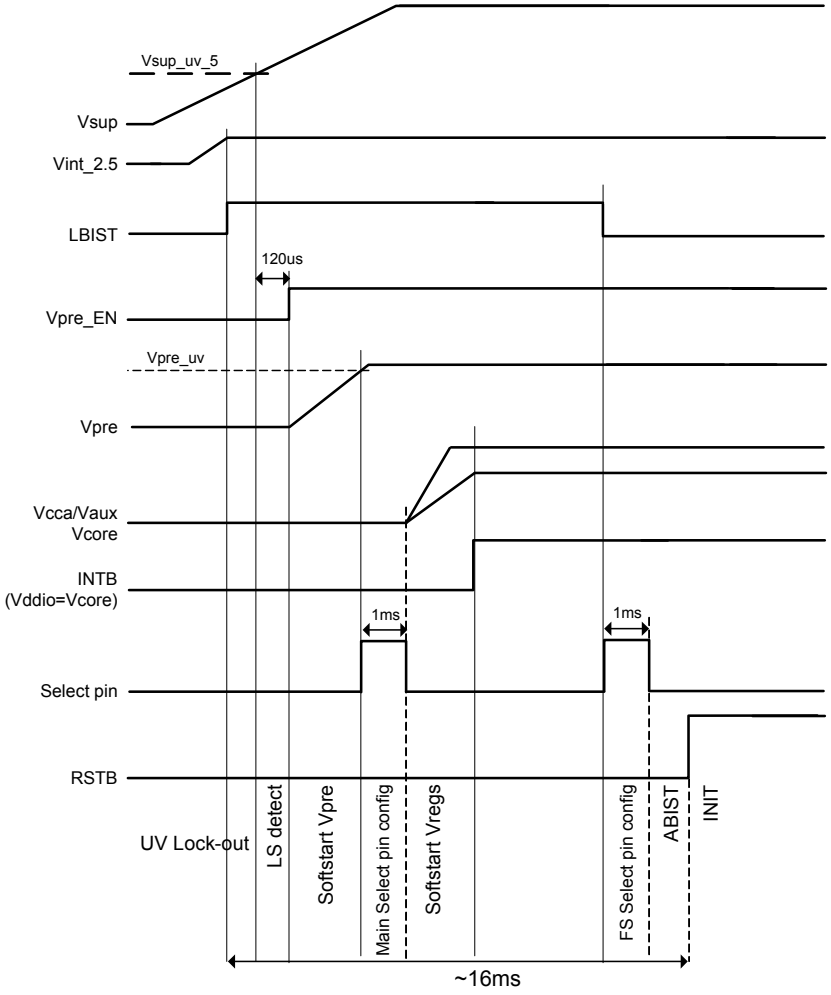


Figure 39. Start-up scheme

The final value of VAUX and VCCA depends on the hardware configuration (resistor values on the SELECT pin). The typical start up sequence takes around 16 ms to release RSTB. RSTB can be pulled low after those 16 ms by the MCU, if it is not ready to run after power up. If an internal or external fault happen during this start up phase (ABIST fault due to regulator shorted for example), the 8.0 s timer monitoring the RSTB pin low, finally sends the device in Deep Fail-safe mode after 8.0 s.

6.8 CAN transceiver

The high speed CAN (Controller Area Network) transceiver provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. It offers excellent EMC and ESD performance and meets the ISO 11898-2 and ISO11898-5 standards.

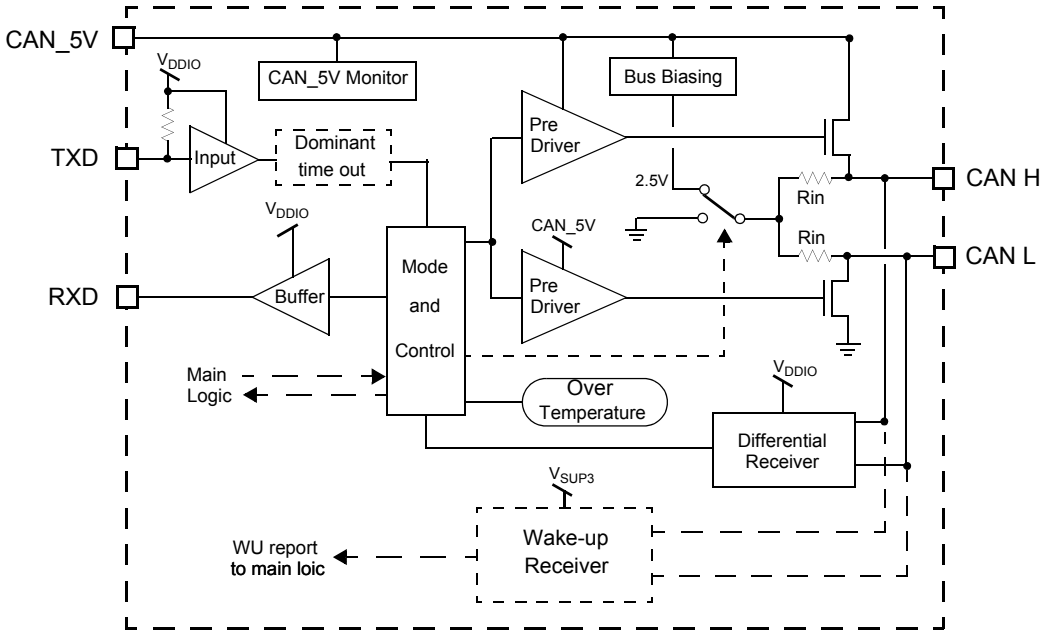


Figure 40. CAN simplified block diagram

6.8.1 Operating modes

6.8.1.1 Normal mode

When CAN mode bits configuration is “11” (CAN in normal operation), the device is able to transmit information from TXD to the bus and report the bus level to the RXD pin. When TXD is high, CANH and CANL drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXD is low, CANH and CANL drivers are ON and the bus is in the dominant state. When CAN mode bits configuration is “01” (CAN in listen only), the device is only able to report the bus level to the RXD pin. TXD driver is OFF and the device is NOT able to transmit information from TXD to the bus. TXD is maintained high by internal pull-up resistor $TXD_{PULL\text{-}UP}$ connected to VDDIO.

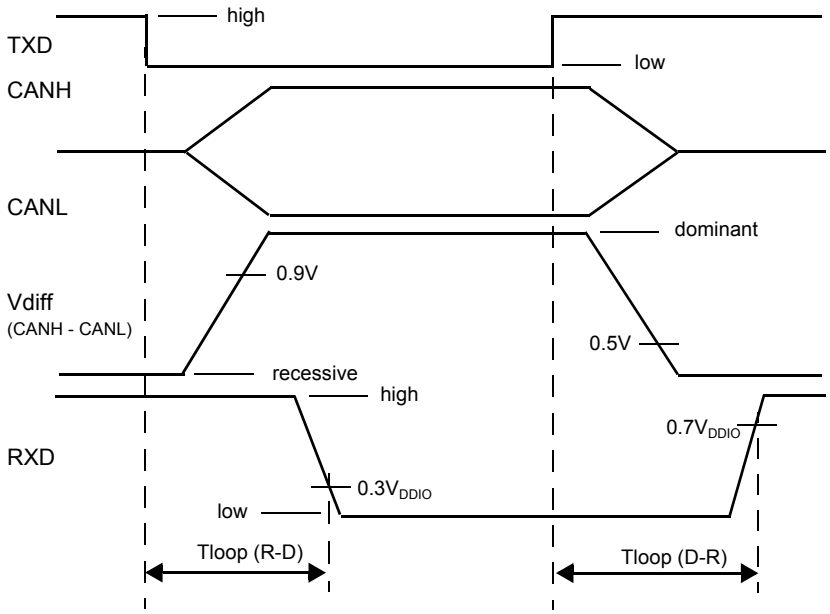


Figure 41. CAN timing diagram

6.8.1.2 Sleep mode

When the device is in LPOFF mode, the CAN transceiver is automatically set in Sleep mode with or without wake-up capability, depending on the CAN mode bits configuration. In that case, the CANH and CANL pins are pulled down to GND via the internal R_{IN} resistor, the TXD and RXD pins are pulled down to GND, both driver and receiver are OFF.

The CAN mode is automatically changed to sleep with wake-up capability, if not configured to sleep without wake-up capability when the device enters is LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored (Figure 42).

CAN state before entering LPOFF		CAN state in LPOFF		CAN state after LPOFF	
CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state
0	Sleep, no wake-up capability	0	Sleep, no wake-up capability	0	Sleep, no wake-up capability
1	Listen Only	10	Sleep, wake-up capability	1	Listen Only
10	Sleep, wake-up capability			10	Sleep, wake-up capability
11	Normal			11	Normal

Figure 42. CAN transition when device goes to LPOFF

6.8.2 Fault detection

6.8.2.1 TXD permanent dominant (timeout)

If TXD is set low for a time longer than t_{DOUT} parameter, the CAN drivers are disabled, and the CAN bus returns to recessive state. The CAN receiver continues to operate. This prevent the bus to be set in dominant state permanently in case a failure set the TXD input to low level permanently.

The CAN_mode MSB bit is set to 0 and the flag TXD_dominant is reported in the Diag CAN1 register. The device recovers from this error detection after setting the CAN_mode to Normal operation and when a high level is detected on TXD. The TXD failure detection is operating when the CAN transceiver is in Normal mode and Listen Only mode.

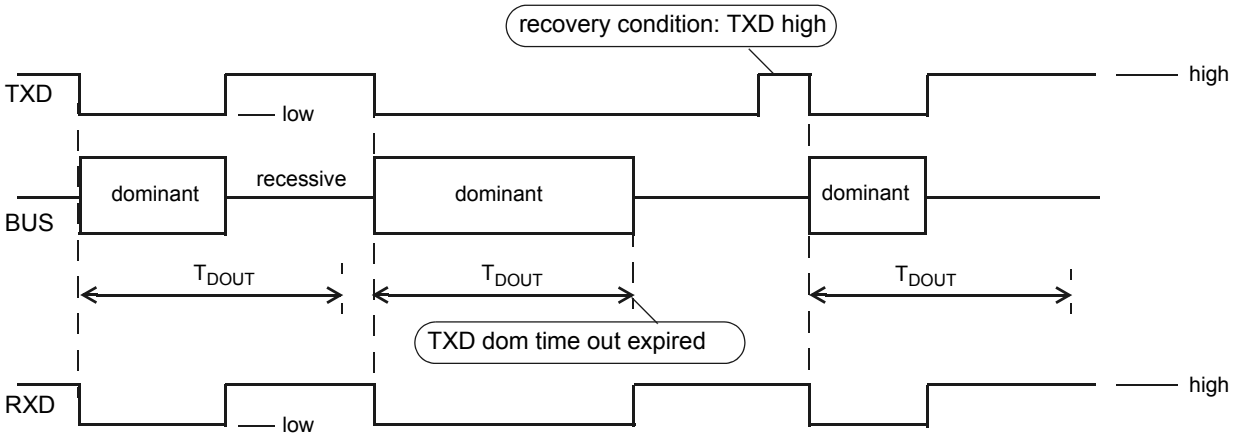


Figure 43. TXD dominant timeout detection

6.8.2.2 RXD permanent recessive

If RXD is detected high for seven consecutive receive/dominant cycles, the CAN drivers and receiver are disabled, and the CAN bus returns to recessive state. This prevent a CAN protocol controller to start CAN message on TXD pin, while RXD is shorted to a recessive level, and seen from a CAN controller as a bus idle state.

The CAN_mode MSB bit is set to 0 and the flag RXD_recessive is reported in the Diag CAN1 register. The device recovers from this error detection after setting the CAN_mode to Normal operation. The RXD failure detection is operating when the CAN transceiver is in Normal mode and Listen Only mode.

6.8.2.3 CAN bus short-circuits

CANL short to GND and CANL short to battery are detected and reported to the device main logic. The CAN driver and receiver are not be disabled. CANH short to GND and CANH short to battery are detected and reported to the device main logic. The CAN driver and receiver are not be disabled. The CANH and CANL failure detection is operating when the CAN transceiver is in Normal mode.

If the CAN bus is dominant for a time longer than t_{DOM}, due for instance to an external short-circuit from another CAN node, the flag CAN_dominant is reported in the Diag CAN1 register. This failure does not disable the bus driver. The CAN bus dominant failure detection is operating when the CAN transceiver is in Normal mode and Listen Only mode.

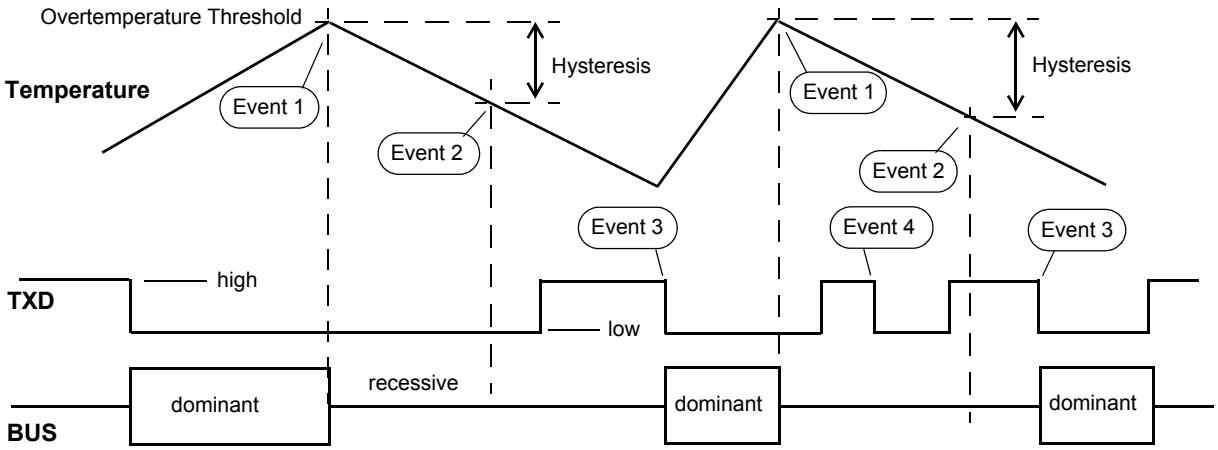
6.8.2.4 CAN current limitation

The current flowing in and out of the CANH and CANL driver is limited to 100 mA, in case of a short-circuit (parameters $I_{CANL-SK}$ and $I_{CANH-SC}$).

6.8.2.5 CAN overtemperature

If the driver temperature exceeds the TSD (T_{OT}), the CAN drivers are disabled, and the CAN bus returns to recessive state. The CAN receiver continues to operate. The CAN_mode MSB bit is set to 0 and the flag CAN_OT is reported in the Diag CAN register.

An hysteresis is implemented in this protection feature. The device overtemperature and recovery conditions are shown in Figure 44. The CAN drivers remain disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the CAN_mode to Normal operation and when a high level is detected on TXD.



Event 1: over temperature detection. CAN driver disable.
Event 2: temperature falls below “overtemp. threshold minus hysteresis” => CAN driver remains disable.
Event 3: temperature below “overtemp. threshold minus hysteresis” and TxD high to low transition => CAN driver enable.
Event 4: temperature above “overtemp. threshold minus hysteresis” and TxD high to low transition => CAN driver remains disable.

Figure 44. Overtemperature behavior

6.8.2.6 Distinguish CAN diagnostics and CAN errors

The CAN errors can generate an interruption while the CAN diagnostics are reported in the digital for information only. The interruption generated by the CAN errors can be inhibited setting INT_inh_CAN bit at “1” in the “INIT INT” register. The list of CAN Diagnostic and CAN Error bits are provided in Table 11.

Table 11. CAN diagnostic and CAN error bits

Register	Bit	Flag Type	Effect
DIAG CAN1	CANH_batt	Diagnostic	No impact on CAN transceiver
	CANH_gnd	Diagnostic	No impact on CAN transceiver
	CANL_batt	Diagnostic	No impact on CAN transceiver
	CANL_gnd	Diagnostic	No impact on CAN transceiver
	CAN_dominant	Error	Turn OFF CAN transceiver
	RXD_recessive	Error	Turn OFF CAN transceiver
	TXD_dominant	Error	Turn OFF CAN transceiver
DIAG CAN	CAN_OT	Error	Turn OFF CAN transceiver
	CAN_OC	Diagnostic	No impact on CAN transceiver

6.8.3 Wake-up mechanism

The device include bus monitoring circuitry to detect and report bus wake-ups when the device is in LPOFF and CAN mode configuration is different than Sleep/NO wake-up capability. Two wake-up detection are implemented: single dominant pulse and multiple dominants pulses. The wake-up mechanism is selected by the SPI in the main logic and wake-up events are reported. The event must occur within the t_{3PTOX} timeout. t_{3PTOX} = t_{3PTO1} or t_{3PTO2}, depending on the SPI selection.

6.8.3.1 Single pulse detection

To activate the wake-up report, 1 event must occur on the CAN bus:

- event 1: a dominant level for a time longer that t_{1PWU}

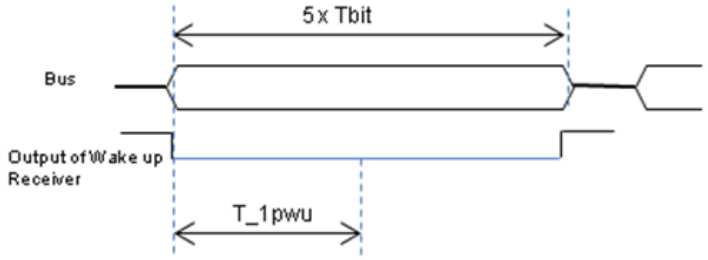


Figure 45. Single pulse wake-up pattern illustration

6.8.3.2 Multiple pulse detection

In order to activate wake-up report, three events must occur on the CAN bus:

- event 1: a dominant level for a time longer that t_{1PWU} followed by
- event 2: a recessive level (event 2) longer than t_{3PWU} followed by
- event 3: a dominant level (event 3) longer than t_{3PWU}.

The three events and the timeout function avoid a permanent dominant state on the bus generates permanent wake-up situation, which would prevent system to enter in low-power mode.

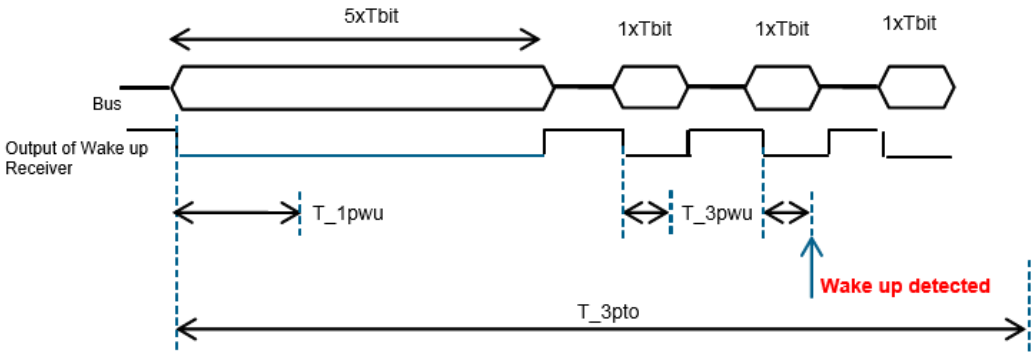


Figure 46. Multiple pulse wake-up pattern illustration

7 Serial peripheral interface

7.1 High level overview

7.1.1 SPI

The device is using a 16-bit SPI, with the following arrangement:

MOSI, Master Out Slave In bits:

- Bit 15 read/write
- Bit 14 Main or fail-safe register target
- bit 13 to 9 (A4 to A0) to select the register address. Bit 8 is a parity bit in write mode, Next bit (=0) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0(Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

Figure 47 is an overview of the SPI implementation.

7.1.2 Parity bit 8 calculation

The parity is used for write to register command (bit 15,14 = 01). It is calculated based on the number of logic ones contained in bits 15-9, 7-0 sequence (this is the whole 16-bits of the write command except bit 8).

Bit 8 must be set to 0 if the number of 1 is odd.

Bit 8 must be set to 1 if the number of 1 is even.

7.1.3 Device status on MISO

When a write operation is performed to store data or control bit into the device, MISO pin reports a 16-bit fixed device status composed of two bytes: Device Fixed Status (bits 15 to 8) + extended Device Status (bits 7 to 0). In a read operation, MISO reports the fixed device status (bits 15 to 8), and the next eight bits are content of the selected register. A standard serial peripheral interface (SPI) is integrated to allow bi-directional communication between the FS6407/FS6408 and the MCU. The SPI is used for configuration and diagnostic purposes.

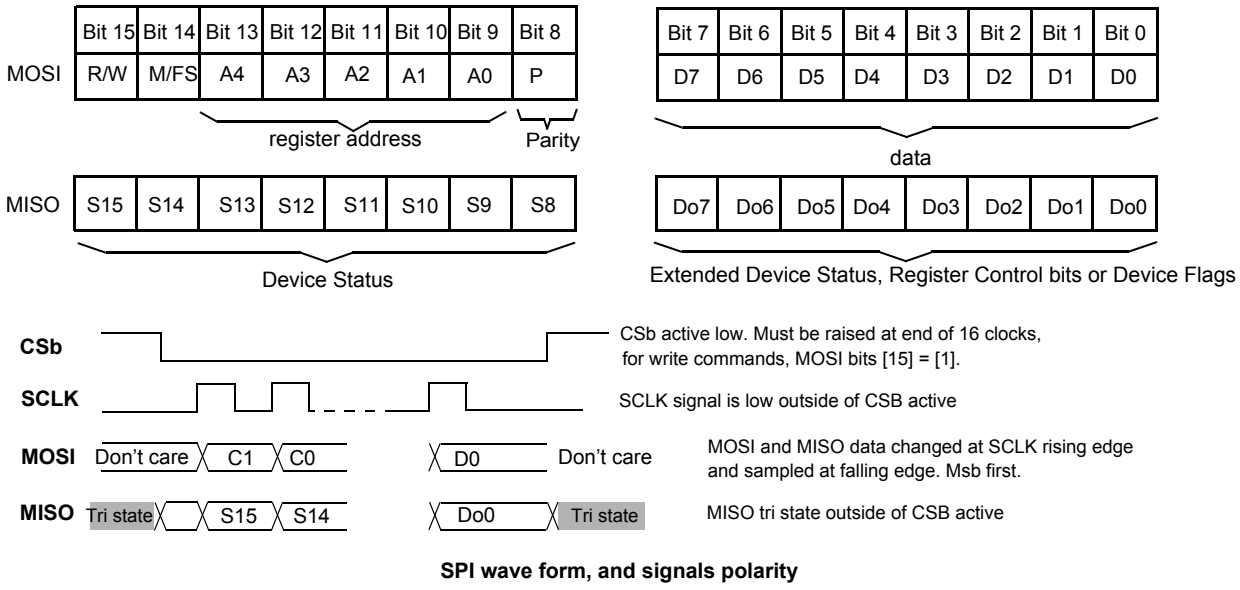


Figure 47. SPI overview

The device contains several registers. Their address is coded on 7 bits (bits 15 to 9). Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior. Every register can also be read back to ensure its content (default setting or value previously written) are correct.

7.1.4 Register description

Although the minimum time between two NCS low sequences is defined by t_{ONNCS} (Figure 48), two consecutive accesses to the fail-safe registers must be done with a 3.5 µs minimum NCS high time in between. Although the minimum time between two fail-safe registers accesses is 3.5 µs, some SPI accesses to the main registers can be done in between (Figure 48).

7.2 Detail operation

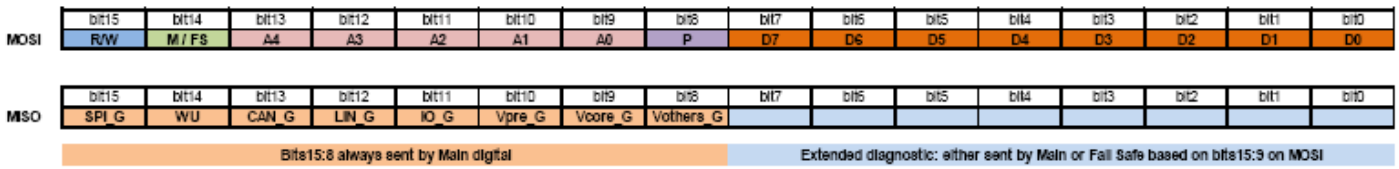


Figure 48. MOSI / MISO SPI command organization

Table 12. MOSI bits description

R / W	Description	Set if it is a READ or WRITE Command
	0	READ
	1	WRITE
M / FS	Description	Split the addresses between Fail-safe state machine and main Logic
	0	Main
	1	Fail-safe
A4:0	Description	Set the address to Read or Write
	0	See Register Mapping
	1	
P	Description	Parity bit (only use in Write mode). Set to 0 in Read mode
	0	Number of “1” (bit15:9 and bit 7:0) is odd
	1	Number of “1” (bit15:9) and bit 7:0) is even
D7:0	Description	Data in Write mode. Must be set to 00h in Read mode
	0	See Register Details
	1	

Table 13. MISO bits description

SPI_G	Description	Report an error in the SPI communication
	0	No Failure
	1	Failure
	Reset Condition	Power On Reset / When initial event cleared on read
WU	Description	Report a wake-up event. Logical OR of all wake-up sources
	0	No WU event
	1	WU event
	Reset Condition	Power On Reset / When initial event cleared on read
CAN_G	Description	Report a CAN event (Diagnostic)
	0	No event
	1	CAN event
	Reset Condition	Power On Reset / When initial event cleared on read
IO_G	Description	Report a change in IOs state
	0	No IO transition
	1	IO transition
	Reset Condition	Power On Reset / when initial event cleared on read
VPRE_G	Description	Report an event from $V_{PRE\text{-}REGULATOR}$ and battery monitoring (status change or failure)
	0	No event
	1	Event occurred
	Reset Condition	Power On Reset / when initial event cleared on read
VCORE_G	Description	Report an event from V_{CORE} regulator (status change or failure)
	0	No event
	1	Event occurred
	Reset Condition	Power On Reset / when initial event cleared on read
VOTHERS_G	Description	Report an event from V_{CCA}, V_{AUX}, or V_{CAN} regulators (status change or failure)
	0	No event
	1	Event occurred
	Reset Condition	Power On Reset / when initial event cleared on read

SPI_G = SPI_err or SPI_clk or SPI_Req or SPI_Parity or SPI_FS_err or SPI_FS_clk or SPI_FS_Req or SPI_FS_Parity

WU_G = IO_5_WU or IO_4_WU or IO_3_WU or IO_2_WU or IO_1_WU or IO_0_WU or PHY_WU

CAN_G = CANH_BATT or CANH_GND or CANL_BATT or CANL_GND or CAN_dominant or RXD_recessive or TXD_dominant or CAN_OT or CAN_OC

IO_G = IO_5 or IO_4 or IO_3 or IO_2 or IO_1 or IO_0

Vpre_G = VSNS_UV or VSUP_UV_7 or ILIM_PRE or TWARN_PRE or BOB or VPRE_STATE_flag or VPRE_OV or VPRE_UV

Vcore_G = ILIM_CORE or TWARN_CORE or VCORE_STATE_flag or VCORE_OV or VCORE_UV

Vothers_G = ILIM_CCA or TWARN_CCA or TSD_CCA or ILIM_CCA_OFF or VCCA_UV or VCCA_OV or ILIM_AUX or VAUX_TSD or ILIM_AUX_OFF or VAUX_OV or VAUX_UV or ILIM_CAN or VCAN_UV or VCAN_OV or TSD_CAN

7.2.1 Register address table

Table 14 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for main logic.

Table 14. Register mapping of main logic

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
NOT USED	0	0	0	0	0	0	#0(00h)	N/A	N/A
INIT Vreg 1	0	0	0	0	0	1	#1(01h)	Write during INIT phase then read only	Table 17
INIT Vreg2	0	0	0	0	1	0	#2(02h)	Write during INIT phase then read only	Table 19
INIT CAN	0	0	0	0	1	1	#3(03h)	Write during INIT phase then read only	Table 21
INIT IO_WU1	0	0	0	1	0	0	#4(04h)	Write during INIT phase then read only	Table 23
INIT IO_WU2	0	0	0	1	0	1	#5(05h)	Write during INIT phase then read only	Table 25
INIT INT	0	0	0	1	1	0	#6(06h)	Write during INIT phase then read only	Table 27
NOT USED	0	0	0	1	1	1	#7(07h)	N/A	N/A
HW Config	0	0	1	0	0	0	#8(08h)	Read only	Table 29
WU Source	0	0	1	0	0	1	#9(09h)	Read only	Table 31
NOT USED	0	0	1	0	1	0	#10(0Ah)	N/A	N/A
IO_input	0	0	1	0	1	1	#11(0Bh)	Read only	Table 33
Status Vreg#1	0	0	1	1	0	0	#12(0Ch)	Read only	Table 35
Status Vreg#2	0	0	1	1	0	1	#13(0Dh)	Read only	Table 37
Diag Vreg#1	0	0	1	1	1	0	#14(0Eh)	Read only	Table 39
Diag Vreg#2	0	0	1	1	1	1	#15(0Fh)	Read only	Table 41
Diag Vreg#3	0	1	0	0	0	0	#16(10h)	Read only	Table 43
Diag CAN1	0	1	0	0	0	1	#17(11h)	Read only	Table 45
Diag CAN	0	1	0	0	1	0	#18(12h)	Read only	Table 47
Diag SPI	0	1	0	0	1	1	#19(13h)	Read only	Table 49
NOT USED	0	1	0	1	0	0	#20(14h)	N/A	N/A
MODE	0	1	0	1	0	1	#21(15h)	Write during Normal and Read	Table 51
Vreg Mode	0	1	0	1	1	0	#22(16h)	Write during Normal and Read	Table 53
IO_OUT/AMUX	0	1	0	1	1	1	#23(17h)	Write during Normal and Read	Table 55
CAN Mode	0	1	1	0	0	0	#24(18h)	Write during Normal and Read	Table 57
CAN Mode 2	0	1	1	0	0	1	#25(19h)	Write during Normal and Read	Table 59

Table 15 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for fail-safe logic

Table 15. Register mapping of fail-safe logic

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT Supervisor#1	1	0	0	0	0	1	#33(21h)	Write during INIT phase then Read only	Table 61
INIT Supervisor#2	1	0	0	0	1	0	#34(22h)	Write during INIT phase then Read only	Table 63
INIT Supervisor#3	1	0	0	0	1	1	#35(23h)	Write during INIT phase then Read only	Table 65
INIT FSSM#1	1	0	0	1	0	0	#36(24h)	Write during INIT phase then Read only	Table 67

Table 15. Register mapping of fail-safe logic (continued)

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT FSSM#2	1	0	0	1	0	1	#37(25h)	Write during INIT phase then Read only	Table 69
WD_Window	1	0	0	1	1	0	#38(26h)	Write (No restriction) and Read	Table 71
WD_LFSR	1	0	0	1	1	1	#39(27h)	Write (No restriction) and Read	Table 73
WD_answer	1	0	1	0	0	0	#40(28h)	Write (No restriction) and Read	Table 75
FS_OUT	1	0	1	0	0	1	#41(29h)	Write (No restriction)	Table 77
RSTb request	1	0	1	0	1	0	#42(2Ah)	Write (No restriction)	Table 79
INIT WD	1	0	1	0	1	1	#43(2Bh)	Write during INIT phase then Read only	Table 81
Diag FS1	1	0	1	1	0	0	#44(2Ch)	Read only	Table 83
WD_Counter	1	0	1	1	0	1	#45(2Dh)	Read only	Table 85
Diag_FS2	1	0	1	1	1	0	#46(2Eh)	Read only	Table 87

7.2.2 Secured SPI command

Some SPI commands must be secured to avoid unwanted change of the critical bits. In the fail-safe machine and in the main state machine, the secured bits are calculated from the data bits sent as follows:

Table 16. Secured SPI

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data 3	Data 2	Data 1	Data 0	Secure 3	Secure2	Secure 1	Secure 0

- Secure 3 = NOT(Bit5)
- Secure 2 = NOT(Bit4)
- Secure 1 = Bit7
- Secure 0 = Bit6

7.3 Detail of register mapping

7.3.1 Init VREG 1

Table 17. INIT VREG1 register configuration

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	0	0	0	0	0	0	0	Vcore_FB
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Reserved	Reserved	Reserved	0	0	Reserved	Vcore_FB

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Reserved	Reserved	Reserved	0	0	Reserved	Vcore_FB

Table 18. Description and configuration of the bits (default value in bold)

Vcore_FB	Description	Configure the monitoring of the second V_{CORE} resistor string
	0	**No Monitoring (IO_1 is used as analog & digital input)**
	1	Monitoring enabled (IO_1 can NOT be used for analog/digital input neither for WU from LPOFF)
	Reset condition	Power On Reset

7.3.2 Init Vreg 2

Table 19. INIT VREG2 register configuration

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	1	0	P	0	Tcca_lim_off	Icca_lim	0	0	Taux_lim_off	Vaux_trk_EN	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Tcca_lim_off	Icca_lim	0	0	Taux_lim_off	Vaux_trk_EN	reserved

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Tcca_lim_off	Icca_lim	0	0	Taux_lim_off	Vaux_trk_EN	reserved

Table 20. INIT VREG2. Description and configuration of the bits (default value in bold)

$T_{CCA\_LIM\_OFF}$	Description	Configure the current limitation duration before regulator is switched off. Only used for external PNP
	0	10 ms
	1	**50 ms**
	Reset condition	Power On Reset
I_{CCA_LIM}	Description	Configure the current limitation threshold. Only available for external PNP
	0	**$I_{CCA\_LIM\_OUT}$**
	1	$I_{CCA\_LIM\_INT}$
	Reset condition	Power On Reset
$T_{AUX\_LIM\_OFF}$	Description	Configure the current limitation duration before regulator is switched off. Only used for external PNP
	0	10 ms
	1	**50 ms**
	Reset condition	Power On Reset
$V_{AUX\_TRK\_EN}$	Description	Configure V_{AUX} regulator as a tracker
	0	**No tracking. HW configuration is used**
	1	Tracking enabled
	Reset condition	Power On Reset

7.3.3 Init CAN

Table 21. INIT CAN register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	1	1	P	0	CAN_wu_conf	0	0	CAN_wu_TO	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	CAN_wu_conf	Reserved	Reserved	CAN_wu_TO	Reserved	Reserved	Reserved

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	CAN_wu_conf	Reserved	Reserved	CAN_wu_TO	Reserved	Reserved	Reserved

Table 22. INIT CAN. Description and configuration of the bits (default value in bold)

CAN_wu_conf	Description	Define the CAN wake-up mechanism
	0	**3 dominant pulses**
	1	Single dominant pulse
	Reset condition	Power On Reset
CAN_wu_to	Description	Define the CAN wake-up timeout (in case of CAN_wu_conf = 0)
	0	**120 µs**
	1	360 µs
	Reset condition	Power On Reset

7.3.4 INIT IO_WU1

Table 23. INIT IO_WU1 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	0	0	P	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU_2_1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU-2-1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU-2-1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0

Table 24. INIT IO_WU1. Description and configuration of the bits (default value in bold)

WU_0_1:0	Description	Wake-up configuration for IO_0
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset
WU_1_1:0	Description	Wake-up configuration for IO_1
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset

Table 24. INIT IO_WU1. Description and configuration of the bits (default value in bold) (continued)

WU_2_1:0	Description	Wake-up configuration for IO_2
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset
INT_inh_IO_1	Description	Inhibit the INT pulse for IO_1. IO_1 masked in IO_G. Avoid INT when used in FS
	0	**INT NOT masked**
	1	INT masked
	Reset condition	Power On Reset
INT_inh_IO_0	Description	Inhibit the INT pulse for IO_0. IO_0 masked in IO_G. Avoid INT when used in FS
	0	**INT NOT masked**
	1	INT masked
	Reset condition	Power On Reset

7.3.5 INIT IO_WU2

Table 25. INIT IO_WU2 register description

Write

	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	1	0	1	P	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45

Read

	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45

Table 26. INIT IO_WU2. Description and configuration of the bits (default value in bold)

WU_3_1:0	Description	Wake-up configuration for IO_3
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset

Table 26. INIT IO_WU2. Description and configuration of the bits (default value in bold) (continued)

WU_4_1:0	Description	Wake-up configuration for IO_4
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset
WU_5_1:0	Description	Wake-up configuration for IO_5
	00	**NO wake-up capability**
	01	Wake-up on rising edge only
	10	Wake-up on falling edge only
	11	Wake-up on any edge
	Reset condition	Power On Reset
INT_inh_IO_45	Description	Inhibit the INT pulse for IO_4 & IO_5. IO_4 & IO_5 masked in IO_G. Avoid INT when used in FS
	0	**INT NOT masked**
	1	INT masked
	Reset condition	Power On Reset
INT_inh_IO_23	Description	Inhibit the INT pulse for IO_2 & IO_3. IO_2 & IO_3 masked in IO_G. Avoid INT when used in FS
	0	INT NOT masked
	1	**INT masked**
	Reset condition	Power On Reset

7.3.6 INIT INT

Table 27. INIT INT register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	1	0	P	INT_duration	0	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	INT_inh_CAN

MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	INT_duration	Reserved	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	INT_inh_CAN

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	INT_duration	Reserved	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	INT_inh_CAN

Table 28. INIT INT. Description and configuration of the bits (default value in bold)

INT_duration	Description	Define the duration of the INTerrupt pulse
	0	**100 µs**
	1	25 µs
	Reset condition	Power On Reset
INT_inh_all	Description	Inhibit ALL the INT
	0	**All INT sources**
	1	All INT INHIBITED
	Reset condition	Power On Reset
INT_inh_Vsns	Description	Inhibit the INT for V_{SNS_UV}
	0	**All INT sources**
	1	V_{SNS_UV} INT INHIBITED
	Reset condition	Power On Reset
INT_inh_Vpre	Description	Inhibit the INT for V_{PRE} status event (cf. register status Vreg1)
	0	**All INT sources**
	1	V_{PRE} status changed INHIBITED
	Reset condition	Power On Reset
INT_inh_Vcore	Description	Inhibit the INT for V_{CORE} status event (cf. register status Vreg2)
	0	**All INT sources**
	1	V_{CORE} status changed INHIBITED
	Reset condition	Power On Reset
INT_inh_Vothers	Description	Inhibit the INT for V_{CCA} / V_{AUX} and V_{CAN} status event (cf. register status Vreg2)
	0	**All INT sources**
	1	V_{CCA} / V_{AUX} / V_{CAN} status changed INHIBITED
	Reset condition	Power On Reset
INT_inh_CAN	Description	Inhibit the INT for CAN error bits
	0	**All INT sources**
	1	CAN error bits changed INHIBITED
	Reset condition	Power On Reset

7.3.7 HW config

Table 29. HW config. register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Others_G	LS_detect	Vaux not used	Vcca_PNP_detect	Vcca_HW	Vaux_HW	1	0	DBG

Table 30. HW config. description and configuration of the bits (default value in bold)

LS_detect	Description	Report the hardware configuration of V_{PRE} (Buck only or Buck-Boost)
	0	**Buck-Boost**
	1	Buck only
	Reset condition	Power On Reset / Refresh after LPOFF
V_{AUX} not used	Description	Report if V_{AUX} is used
	0	V_{AUX} is used (external PNP is assumed to be connected, V_{AUX} can be switched OFF/ON through SPI)
	1	V_{AUX} is not used
	Reset condition	Power On Reset / Refresh after LPOFF
$V_{CCA\_PNP\_DETECT}$	Description	Report the connection of an external PNP on V_{CCA}
	0	External PNP connected
	1	Internal MOSFET
	Reset condition	Power On Reset / Refresh after LPOFF
V_{CCA_HW}	Description	Report the hardware configuration for V_{CCA}
	0	**3.3 V**
	1	5.0 V
	Reset condition	Power On Reset / Refresh after LPOFF
V_{AUX_HW}	Description	Report the hardware configuration for V_{AUX}
	0	5.0 V
	1	**3.3 V**
	Reset condition	Power On Reset / Refresh after LPOFF
DBG	Description	Report the configuration of the DEBUG mode
	0	Normal operation
	1	DEBUG mode selected
	Reset condition	Power On Reset / Refresh after LPOFF

7.3.8 WU source

Table 31. WU source register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_5_WU	IO_4_WU	IO_3_WU	IO_2_WU	IO_1_WU	IO_0_WU	0	Phy_WU

Table 32. WU source. Description and configuration of the bits (default value in bold)

IO_5_WU	Description	Report a wake-up event from IO_5
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_4_WU	Description	Report a wake-up event from IO_4
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_3_WU	Description	Report a wake-up event from IO_3
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_2_WU	Description	Report a wake-up event from IO_2
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_1_WU	Description	Report a wake-up event from IO_1
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_0_WU	Description	Report a wake-up event from IO_0
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read
Phy_WU	Description	Report a wake-up event from CAN
	0	**No Wake-up**
	1	WU event detected
	Reset condition	Power On Reset / Read CAN_wu

7.3.9 IO input

Table 33. IO input register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_5	IO_4	0	IO_3	IO_2	0	IO_1	IO_0

Table 34. IO input. Description and configuration of the bits

IO_5	Description	Report IO_5 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_4	Description	Report IO_4 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_3	Description	Report IO_3 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_2	Description	Report IO_2 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_1	Description	Report IO_1 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_0	Description	Report IO_0 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset

7.3.10 Status VREG1

Table 35. STATUS VREG1 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Ilim_pre	Twarn_pre	BoB	Vpre_state	0	0	0

Table 36. Status VREG1. Description and configuration of the bits (default value in bold)

I_{LIM_PRE}	Description	Report a current limitation condition on V_{PRE}
	0	**No current limitation ($I_{PRE\_PK} < I_{PRE\_LIM}$)**
	1	Current limitation ($I_{PRE\_PK} > I_{PRE\_LIM}$)
	Reset condition	Power On Reset / Read
T_{WARN_PRE}	Description	Report a thermal warning from V_{PRE}
	0	**No thermal warning ($T_J < T_{WARN\_PRE}$)**
	1	Thermal warning ($T_J > T_{WARN\_PRE}$)
	Reset condition	Power On Reset / Read
BoB	Description	Report a running mode of V_{PRE}
	0	**Buck**
	1	Boost
	Reset condition	Power On Reset
V_{PRE_STATE}	Description	Report the activation state of V_{PRE} SMPS
	0	SMPS OFF
	1	**SMPS ON**
	Reset condition	Power On Reset

7.3.11 Status VREG2

Table 37. STATUS VREG2 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Ilim_core	Twarn_core	Vcore_state	Twarn_cca	Ilim_cca	Ilim_aux	Ilim_can	0

Table 38. Status VREG2. Description and configuration of the bits (default value in bold)

I_{LIM_CORE}	Description	Report a current limitation condition on V_{CORE}
	0	**No current limitation ($I_{CORE\_PK} < I_{CORE\_LIM}$)**
	1	Current limitation ($I_{CORE\_PK} > I_{CORE\_LIM}$)
	Reset condition	Power On Reset / Read
T_{WARN_CORE}	Description	Report a thermal warning from V_{CORE}
	0	**No thermal warning ($T_J < T_{WARN\_CORE}$)**
	1	Thermal warning ($T_J > T_{WARN\_CORE}$)
	Reset condition	Power On Reset / Read
V_{CORE_STATE}	Description	Report the activation state of V_{CORE} SMPS
	0	SMPS OFF
	1	**SMPS ON**
	Reset condition	Power On Reset

Table 38. Status VREG2. Description and configuration of the bits (default value in bold)(continued)

T_{WARN_CCA}	Description	Report a thermal warning from V_{CCA}. Available only for internal pass MOSFET
	0	**No thermal warning ($T_J < T_{WARN\_CCA}$)**
	1	Thermal warning ($T_J > T_{WARN\_CCA}$)
	Reset condition	Power On Reset
I_{LIM_CCA}	Description	Report a current limitation condition on V_{CCA}
	0	**No current limitation ($I_{CCA} < I_{CCA\_LIM}$)**
	1	Current limitation ($I_{CCA} > I_{CCA\_LIM}$)
	Reset condition	Power On Reset / Read
I_{LIM_AUX}	Description	Report a current limitation condition on V_{AUX}
	0	**No current limitation ($I_{AUX} < I_{AUX\_LIM}$)**
	1	Current limitation ($I_{AUX} > I_{AUX\_LIM}$)
	Reset condition	Power On Reset / Read
I_{LIM_CAN}	Description	Report a current limitation condition on V_{CAN}
	0	**No current limitation ($I_{CAN} < I_{CAN\_LIM}$)**
	1	Current limitation ($I_{CAN} > I_{CAN\_LIM}$)
	Reset condition	Power On Reset / Read

7.3.12 Diag VREG1

Table 39. DIAG VREG1 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Vsns_uv	Vsup_uv_7	Tsd_pre	Vpre_OV	Vpre_uv	Tsd_core	Vcore_FB_OV	Vcore_FB_uv

Table 40. Diag VREG1. Description and configuration of the bits (default value in bold)

V_{SNS_UV}	Description	Detection of $V_{BATTERY}$ below V_{SNS_UV}
	0	$V_{BAT} > V_{SNS\_UV}$
	1	**$V_{BAT} < V_{SNS\_UV}$**
	Reset condition	Power On Reset / Read
$V_{SUP\_UV\_7}$	Description	Detection of V_{SUP} below $V_{SUP\_UV\_7}$
	0	$V_{SUP} > V_{SUP\_UV\_7}$
	1	**$V_{SUP} < V_{SUP\_UV\_7}$**
	Reset condition	Power On Reset / Read
T_{SD_PRE}	Description	Thermal shutdown of V_{PRE}
	0	**No TSD ($T_J < T_{SD\_PRE}$)**
	1	TSD occurred ($T_J > T_{SD\_PRE}$)
	Reset condition	Power On Reset / Read

Table 40. Diag VREG1. Description and configuration of the bits (default value in bold) (continued)

V_{PRE_OV}	Description	V_{PRE} overvoltage detection
	0	**No overvoltage ($V_{PRE} < V_{PRE\_OV}$)**
	1	Overvoltage detected ($V_{PRE} > V_{PRE\_OV}$)
	Reset condition	Power On Reset
V_{PRE_UV}	Description	V_{PRE} undervoltage detection
	0	No undervoltage (VPRE > VPRE_UV)
	1	**Undervoltage detected ($V_{PRE} < V_{PRE\_UV}$)**
	Reset condition	Power On Reset / Read
T_{SD_CORE}	Description	Thermal shutdown of V_{CORE}
	0	**No TSD ($T_J < T_{SD\_CORE}$)**
	1	TSD occurred ($T_J > T_{SD\_CORE}$)
	Reset condition	Power On Reset / Read
$V_{CORE\_FB\_OV}$	Description	V_{CORE} overvoltage detection
	0	**No overvoltage ($V_{CORE\_FB} < V_{CORE\_FB\_OV}$)**
	1	Overvoltage detected ($V_{CORE\_FB} > V_{CORE\_FB\_OV}$)
	Reset condition	Power On Reset / Read
$V_{CORE\_FB\_UV}$	Description	V_{CORE} undervoltage detection
	0	No undervoltage ($V_{CORE\_FB} > V_{CORE\_FB\_UV}$)
	1	**Undervoltage ($V_{CORE\_FB} < V_{CORE\_FB\_UV}$)**
	Reset condition	Power On Reset / Read

7.3.13 Diag VREG2

Table 41. DIAG VREG2 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Tsd_Can	Vcan_OV	Vcan_uv	0	Tsd_aux	Ilim_aux_off	Vaux_OV	Vaux_uv

Table 42. Diag VREG2. Description and configuration of the bits (default value in bold)

T_{SD_CAN}	Description	Thermal shutdown of V_{CAN}
	0	**NO TSD ($T_J < T_{SD\_CAN}$)**
	1	TSD occurred ($T_J > T_{SD\_CAN}$)
	Reset condition	Power On Reset / Read
V_{CAN_OV}	Description	V_{CAN} Overvoltage detection
	0	**No Overvoltage ($V_{CAN} < V_{CAN\_OV}$)**
	1	Overvoltage detected ($V_{CAN} > V_{CAN\_OV}$)
	Reset condition	Power On Reset / Read

Table 42. Diag VREG2. Description and configuration of the bits (default value in bold) (continued)

V_{CAN_UV}	Description	V_{CAN} undervoltage detection
	0	No undervoltage ($V_{CAN} > V_{CAN\_UV}$)
	1	**Undervoltage detected ($V_{CAN} < V_{CAN\_UV}$)**
	Reset condition	Power On Reset / Read
T_{SD_AUX}	Description	Thermal shutdown of V_{AUX}
	0	**No TSD ($T_J < T_{SD\_AUX}$)**
	1	TSD occurred ($T_J > T_{SD\_AUX}$)
	Reset condition	Power On Reset
$I_{LIM\_AUX\_OFF}$	Description	Maximum current limitation duration
	0	**$T_{\_LIMITATION} < T_{AUX\_LIM\_OFF}$**
	1	$T_{\_LIMITATION} > T_{AUX\_LIM\_OFF}$
	Reset condition	Power On Reset / Read
V_{AUX_OV}	Description	V_{AUX} overvoltage detection
	0	**No overvoltage ($V_{AUX} < V_{AUX\_OV}$)**
	1	Overvoltage detected ($V_{AUX} > V_{AUX\_OV}$)
	Reset condition	Power On Reset / Read
V_{AUX_UV}	Description	V_{AUX} undervoltage detection
	0	No undervoltage ($V_{AUX} > V_{AUX\_UV}$)
	1	**Undervoltage detected ($V_{AUX} < V_{AUX\_UV}$)**
	Reset condition	Power On Reset / Read

7.3.14 Diag VREG3

Table 43. DIAG VREG3 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Tsd_cca	0	Ilim-cca_off	0	Vcca_OV	0	Vcca_UV	0

Table 44. Diag VREG3. Description and configuration of the bits (default value in bold)

T_{SD_CCA}	Description	Thermal shutdown of V_{CCA}
	0	**NO TSD ($T_J < T_{SD\_CCA}$)**
	1	TSD occurred ($T_J > T_{SD\_CCA}$)
	Reset condition	Power On Reset / Read
$I_{LIM\_CCA\_OFF}$	Description	Maximum current limitation duration. Available only when an external PNP is connected
	0	**$T_{\_LIMITATION} < T_{CCA\_LIM\_OFF}$**
	1	$T_{\_LIMITATION} > T_{CCA\_LIM\_OFF}$
	Reset condition	Power On Reset / Read

Table 44. Diag VREG3. Description and configuration of the bits (default value in bold) (continued)

V_{CCA_OV}	Description	V_{CCA} overvoltage detection
	0	**No overvoltage ($V_{CCA} < V_{CCA\_OV}$)**
	1	Overvoltage detected ($V_{CCA} > V_{CCA\_OV}$)
	Reset condition	Power On Reset / Read
V_{CCA_UV}	Description	V_{CCA} undervoltage detection
	0	No undervoltage ($V_{CCA} > V_{CCA\_UV}$)
	1	**Undervoltage detected ($V_{CCA} < V_{CCA\_UV}$)**
	Reset condition	Power On Reset

7.3.15 Diag CAN1

Table 45. DIAG CAN1 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CANH_batt	CANH_gnd	CANL_batt	CANL_gnd	CAN_dominant	0	RXD_recessive	TXD_dominant

Table 46. Diag CAN1. Description and configuration of the bits (default value in bold)

CANH_batt	Description	CANH short-circuit to battery detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
CANH_gnd	Description	CANH short-circuit to GND detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
CANL_batt	Description	CANL short-circuit to battery detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
CANL_gnd	Description	CANL short-circuit to GND detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
CAN_dominant	Description	CAN Bus dominant clamping detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read

Table 46. Diag CAN1. Description and configuration of the bits (default value in bold) (continued)

RXD_recessive	Description	RXD recessive clamping detection (short-circuit to 5.0 V)
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
TXD_dominant	Description	TXD dominant clamping detection (short-circuit to GND)
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read

7.3.16 Diag CAN

Table 47. DIAG CAN register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	0	Reserved	Reserved	0	CAN_OT	CAN_OC

Table 48. Diag CAN. Description and configuration of the bits (default value in bold)

CAN_OT	Description	CAN overtemperature detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read
CAN_OC	Description	CAN overcurrent detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power On Reset / Read

7.3.17 Diag SPI

Table 49. DIAG SPI register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_err	0	SPI_clk	0	SPI_req	0	SPI_parity	0

Table 50. Diag SPI. Description and configuration of the bits (default value in blue)

SPI_err	Description	Secured SPI communication check
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset / Read
SPI_CLK	Description	SCLK error detection
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or > 16)
	Reset condition	Power On Reset / Read
SPI_req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address)
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset / Read
SPI_parity	Description	SPI parity bit error detection
	0	**Parity bit OK**
	1	Parity bit error
	Reset condition	Power On Reset / Read

7.3.18 Mode

Table 51. MODE register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	0	1	P	0	0	Goto_LPOFF	INT_request	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	INIT	Normal	Reserved	Reserved

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	INIT	Normal	Reserved	Reserved

Table 52. MODE. Description and configuration of the bits (default value in bold)

Goto_LPOFF	Description	Configure the device in Low Power mode V_{REG} OFF (LPOFF)
	0	**No action**
	1	LPOFF mode
	Reset condition	Power On Reset
INIT	Description	Report if INIT mode of the main logic state machine is entered
	0	Not in INIT mode
	1	**INIT MODE**
	Reset condition	Power On Reset
Normal	Description	Report if Normal mode of the main logic state machine is entered
	0	**Not in Normal mode**
	1	Normal mode
	Reset condition	Power On Reset
INT_request	Description	Request for an INT pulse
	0	No Request
	1	Request for an INT pulse
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

7.3.19 Vreg mode

Table 53. VREG MODE register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN

Table 54. VREG MODE. Description and configuration of the bits (default value in bold)

V_{CORE_EN}	Description	V_{CORE} control (Switch OFF NOT recommended if V_{CORE} is SAFETY critical)
	0	DISABLED
	1	**ENABLED**
	Reset condition	Power On Reset
V_{CCA_EN}	Description	V_{CCA} control (Switch OFF NOT recommended if V_{CCA} is SAFETY critical)
	0	DISABLED
	1	**ENABLED**
	Reset condition	Power On Reset
V_{AUX_EN}	Description	V_{AUX} control (Switch OFF NOT recommended if V_{AUX} is SAFETY critical)
	0	DISABLED
	1	**ENABLED**
	Reset condition	Power On Reset
V_{CAN_EN}	Description	V_{CAN} control
	0	DISABLED
	1	**ENABLED**
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

7.3.20 IO_OUT-AMUX

Table 55. IO_OUT-AMUX register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	1	P	IO_out_4_EN	IO_out_4	IO_out_5_EN	IO_out_5	0	Amux_2	Amux_1	Amux_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_out_4_EN	IO_oout_4	IO_out_5_EN	IO_out_5	Reserved	Amux_2	Amux_1	Amux_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_out_4_EN	IO_out_4	IO_out_5_EN	IO_out_5	Reserved	Amux_2	Amux_1	Amux_0

Table 56. IO_OUT-AMUX. Description and configuration of the bits (default value in bold)

IO_out_4_EN	Description	Enable the output gate driver capability for IO_4
	0	**High-impedance (IO_4 configured as input)**
	1	ENABLED (IO_4 configured as output gate driver)
	Reset condition	Power On Reset
IO_out_4	Description	Configure IO_4 output gate driver state
	0	**LOW**
	1	HIGH
	Reset condition	Power On Reset
IO_out_5_EN	Description	Enable the output gate driver capability for IO_5
	0	**High-impedance (IO_5 configured as input)**
	1	ENABLED (IO_5 configured as output gate driver)
	Reset condition	Power On Reset
IO_out_5	Description	Configure IO_5 output gate driver state
	0	**LOW**
	1	HIGH
	Reset condition	Power On Reset
AMUX_2:0	Description	Select AMUX output
	000	**Vref**
	111	Die Temperature Sensor
	Reset condition	Power On Reset

7.3.21 CAN mode

Table 57. CAN MODE register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	0	0	P	CAN_mode_1	CAN_mode_0	CAN_auto_dis	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CAN_mode_1	CAN_mode_0	CAN_auto_dis	Reserved	Reserved	Reserved	CAN_wu	Reserved

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CAN_mode_1	CAN_mode_0	CAN_auto_dis	Reserved	Reserved	Reserved	CAN_wu	Reserved

Table 58. CAN MODE. Description and configuration of the bits (default value in bold)

CAN_mode_1:0	Description	Configure the CAN mode
	00	Sleep / NO wake-up capability
	01	LISTEN ONLY
	10	**Sleep / Wake-up capability**
	11	Normal operation mode
	Reset condition	Power On Reset
CAN_auto_dis	Description	Automatic CAN Tx disable
	0	NO auto disable
	1	**Reset CAN_mode from "11" to "01" on CAN over temp or TXD dominant or RXD recessive event**
	Reset condition	Power On Reset
CAN_wu	Description	Report a wake-up event from the CAN
	0	**No wake-up**
	1	Wake-up detected
	Reset condition	Power On Reset / Read

Notes

22. CAN mode is automatically configured to "sleep + wake-up capability[10]" if CAN mode was different than "sleep + no wake-up capability [00]" before the device enters in LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored.

7.3.22 Can_Mode_2

Table 59. CAN_MODE_2 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	0	1	P	0	0	0	Vcan_OV_Mon	secure_3	secure_2	secure_1	secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	Vcan_OV_Mon	Reserved	Reserved	Reserved

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	Vcan_OV_Mon	Reserved	Reserved	Reserved

Table 60. CAN_MODE_2. Description and configuration of the bits (default value in bold)

Vcan_OV_Mon	Description	VCAN OV Monitoring
	0	**OFF. V_{CAN} OV is not monitored. Flag is ignored**
	1	ON. V_{CAN} OV flag is under monitoring. In case of OV the V_{CAN} regulator is switched OFF.
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

7.3.23 INIT SUPERVISOR1

Table 61. INIT SUPERVISOR1 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	0	1	P	Vcore_FS1	Vcore_FS_0	Vcca_FS_1	Vcca_FS_0	secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	Vcore_FS1	Vcore_FS_0	Vcca_FS_1	Vcca_FS_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	Vcore_FS1	Vcore_FS_0	Vcca_FS_1	Vcca_FS_0

Table 62. INIT SUPERVISOR1. Description and configuration of the bits (default value in bold)

Vcore_FS1:0	Description	V_{CORE} safety input.
	00	No effect of $V_{CORE\_FB\_OV}$ and $V_{CORE\_FB\_UV}$ on RSTb and FSxx
	01	$V_{CORE\_FB\_OV}$ DOES HAVE an impact on RSTb and FSxx. $V_{CORE\_FB\_UV}$ DOES HAVE an impact on RSTb only
	10	$V_{CORE\_FB\_OV}$ DOES HAVE an impact on RSTb and FSxx. No effect of $V_{CORE\_FB\_UV}$ on RSTb and FSxx
	11	**Both $V_{CORE\_FB\_OV}$ and $V_{CORE\_FB\_UV}$ DO HAVE an impact on RSTb and FSxx**
	Reset condition	Power On Reset
Vcca_FS1:0	Description	V_{CCA} safety input.
	00	No effect of V_{CCA_OV} and V_{CCA_UV} on RSTb and FSxx
	01	V_{CCA_OV} DOES HAVE an impact on RSTb and FSxx. V_{CCA_UV} DOES HAVE an impact on RSTb only
	10	V_{CCA_OV} DOES HAVE an impact on RSTb and FSxx. No effect of V_{CCA_UV} on RSTb and FSxx
	11	**Both V_{CCA_OV} and V_{CCA_UV} DO HAVE an impact on RSTb and FSxx**
	Reset condition	Power On Reset

Table 62. INIT SUPERVISOR1. Description and configuration of the bits (default value in bold) (continued)

Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns Fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in Normal mode, wrong address), concerns fail-safe logic only.
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.24 INIT SUPERVISOR2

Table 63. INIT SUPERVISOR2 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	0	P	Vaux_FS1	Vaux_FS_0	0	DIS_8s	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	DIS_8s	Vaux_FS1	Vaux_FS_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	DIS_8s	Vaux_FS1	Vaux_FS_0

Table 64. INIT SUPERVISOR2. Description and configuration of the bits (default value in bold)

Vaux_FS1:0	Description	V_{AUX} safety input.
	00	No effect of V_{AUX_OV} and V_{AUX_UV} on RSTb and FSxx
	01	V_{AUX_OV} DOES HAVE an impact on RSTb and FSxx. V_{AUX_UV} DOES HAVE an impact on RSTb only
	10	V_{AUX_OV} DOES HAVE an impact on RSTb and FSxx. No effect of V_{AUX_UV} on RSTb and FSxx
	11	**Both V_{AUX_OV} and V_{AUX_UV} DO HAVE an impact on RSTb and FSxx**
	Reset condition	Power On Reset
DIS_8s	Description	Disable the 8.0 s timer used to enter Deep Fail-safe mode
	0	**ENABLED**
	1	DISABLED
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only.
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.25 INIT SUPERVISOR3

Table 65. INIT SUPERVISOR3 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	1	P	0	Vcca_5D	Vaux_5D	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	Reserved	Vcca_5D	Vaux_5D

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	Reserved	Vcca_5D	Vaux_5D

Table 66. INIT SUPERVISOR3. Description and configuration of the bits (default value in bold)

V_{CCA_5D}	Description	Configure the V_{CCA} undervoltage in degraded mode. Only valid for 5.0 V
	0	**Normal 5.0 V undervoltage detection threshold ($V_{CCA\_UV\_5}$)**
	1	Degraded mode, i.e lower undervoltage detection threshold applied ($V_{CCA\_UV\_D}$)
	Reset condition	Power On Reset
V_{AUX_5D}	Description	Configure the V_{AUX} undervoltage in degraded mode. Only valid for 5.0 V
	0	**Normal 5.0 V undervoltage detection threshold ($V_{AUX\_UV\_5}$)**
	1	Degraded mode, i.e lower undervoltage detection threshold applied ($V_{AUX\_UV\_5D}$)
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

Table 66. INIT SUPERVISOR3. Description and configuration of the bits (default value in bold) (continued)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.26 Init FSSM1

Table 67. INIT FSSM1 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	0	P	IO_01_FS	IO_1_FS	IO_45_FS	RSTb_low	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	IO_01_FS	IO_1_FS	IO_45_FS	RSTb_low

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	IO_01_FS	IO_1_FS	IO_45_FS	RSTb_low

Table 68. INIT FSSM1. Description and configuration of the bits (default value in bold)

IO_01_FS	Description	Configure the couple of IO_1:0 as safety inputs
	0	**NOT SAFETY**
	1	SAFETY CRITICAL
	Reset condition	Power On Reset
IO_1_FS	Description	Configure IO_1 as safety inputs
	0	**NOT SAFETY**
	1	SAFETY CRITICAL (External resistor bridge monitoring active)
	Reset condition	Power On Reset
IO_45_FS	Description	Configure the couple of IO_5:4 as safety inputs
	0	**NOT SAFETY**
	1	SAFETY CRITICAL
	Reset condition	Power On Reset

Table 68. INIT FSSM1. Description and configuration of the bits (default value in bold) (continued)

RSTb_low	Description	Configure the Rstb LOW duration time
	0	**10 ms**
	1	1.0 ms
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.27 Init FSSM2

Table 69. INIT FSSM2 register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	P	RSTb_ err_FS	IO_23_ FS	PS	0	Secure _3	Secure _2	Secure _1	Secure _0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _req	SPI_FS _Parity	RSTb_ err_FS	IO_23_ FS	PS	0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _req	SPI_FS _Parity	RSTb_ err_FS	IO_23_ FS	PS	0

Table 70. INIT FSSM2. Description and configuration of the bits (default value in bold)

IO_23_FS	Description	Configure the couple of IO_3:2 as safety inputs for FCCU monitoring
	0	NOT SAFETY
	1	**SAFETY CRITICAL**
	Reset condition	Power On Reset
RSTb_err_FS	Description	Configure the values of the RSTb error counter
	0	**intermediate = 3; final = 6**
	1	intermediate = 1; final = 2
	Reset condition	Power On Reset
PS	Description	Configure the F_{CCU} polarity
	0	**Fccu_eaout_1:0 active HIGH**
	1	Fccu_eaout_1:0 active LOW
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset

Table 70. INIT FSSM2. Description and configuration of the bits (default value in bold) (continued)

SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.28 WD window

Table 71. WD WINDOW register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	0	P	WD_window3	WD_window2	WD_window1	WD_window0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	WD_window3	WD_window2	WD_window1	WD_window0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	WD_window3	WD_window2	WD_window1	WD_window0

Any WRITE command to the WD_window in the Normal mode must be followed by a READ command to verify the correct change of the WD window duration

Table 72. WD Window. Description and configuration of the bits (default value in bold)

WD_Window_3:0	Description	Configure the watchdog window duration. Duty cycle if set to 50%
	0000	DISABLE
	0001	1.0 ms
	0010	2.0 ms
	0011	**3.0 ms**
	0100	4.0 ms
	0101	6.0 ms
	0110	8.0 ms
	0111	12 ms
	1000	16 ms
	1001	24 ms
	1010	32 ms
	1011	64 ms
	1100	128 ms
	1101	256 ms
	1110	512 ms
	1111	1024 ms
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK bit.
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.29 WD_LFSR

Table 73. WD LFSR register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	1	P	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0

Table 74. WD LFSR. Description and configuration of the bits (default value in bold)

WD_LFSR_7:0	Description	WD 8 bits LFSR value. Used to write the seed at any time
	0...	bit7:bit0: 10110010 default value at start-up or after a Power on reset: 0xB2 (23), (24)
	1...	
	Reset condition	Power On Reset

Notes

23. Value Bit7:Bit0: 1111 1111 is prohibited.
24. During a write command, MISO reports the previous register content.

7.3.30 WD answer

Table 75. WD answer register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	0	P	WD_answer_7	WD_answer_6	WD_answer_5	WD_answer_4	WD_answer_3	WD_answer_2	WD_answer_1	WD_answer_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb	FS0	WD	FS0_G	IO_FS_G	0	FS_ECC	FS_reg_Ecc

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb	FS0	WD	FS0_G	IO_FS_G	0	FS_ECC	FS_reg_Ecc

Table 76. WD answer. Description and configuration of the bits (default value in bold)

WD_answer_7:0	Description	WD answer from the MCU
	0...	Answer = (NOT(((LFSR x 4)+6)-4))/4
	1...	
	Reset condition	Power On Reset / RSTb LOW
RSTb	Description	Report a reset event
	0	**No Reset**
	1	Reset occurred
	Reset condition	Power On Reset / Read
FS0b	Description	Report a fail-safe event
	0	No fail-safe
	1	**Fail safe event occurred / Also default state at power-up after LPOFF as FS0b is asserted low**
	Reset condition	Power On Reset / Read
WD	Description	Report a watchdog refresh ERROR
	0	**WD refresh OK**
	1	WRONG WD refresh
	Reset condition	Power On Reset / Read
FS0_G	Description	Report a fail-safe output failure
	0	**No failure**
	1	Failure
	Reset condition	Power On Reset / Read
IO_FS_G	Description	Report an IO monitoring error
	0	**No error**
	1	Error detected
	Reset condition	Power On Reset
FS_ECC	Description	Report an error code correction on fail-safe state machine
	0	**No ECC**
	1	ECC done
	Reset condition	Power On Reset / Read
FS_req_ECC	Description	Report an error code correction on fail-safe registers
	0	**No ECC**
	1	ECC done
	Reset condition	Power On Reset / Read

FS0_G = RSTB_short_high or FS0B_short_high or FS0B_short_low

IO_FS_G = IO_01_fail or IO_1_fail or IO_23_fail or IO_45_fail

Values of the three registers WD_answer, WD_counter, and DIAG_FS2 are updated at the end of any SPI access to one of these registers. To always get up to date values, it is recommended to make two consecutive SPI accesses to these registers. Example: read WD_answer, read again WD_answer, read WD_counter, read DIAG_FS2. The first read updates the three registers and the second read report the latest information.

7.3.31 Fail-safe out (FS_out)

Table 77. Fail-safe out register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	1	P	FS_out_7	FS_out_6	FS_out_5	FS_out_4	FS_out_3	FS_out_2	FS_out_1	FS_out_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	0	0	0	0

Table 78. Fail-safe out. Description and configuration of the bits (default value in bold)

FS_out_7:0	Description	Secured 8 bits word to release the FS0b
	0...	Depend on LFSR_out value and calculation
	1...	
	Reset condition	Power On Reset -> Default = 00h

7.3.32 RSTB request

Table 79. RSTB request register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	0	P	0	0	RSTb_request	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	0	0	0	0

Table 80. RSTB request. Description and configuration of the bits (Default value in bold)

RSTb_request	Description	Request a RSTb low pulse
	0	**No request**
	1	Request a RSTb low pulse
	Reset condition	Power On Reset / When RSTb done
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

7.3.33 INIT_WD

Table 81. INIT WD register description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	1	P	WD_CNT_error_1	WD_CNT_error_0	WD_CNT_refresh_1	WD_CNT_refresh_0	secure 3	secure 2	secure 1	secure 0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	WD_CNT_error_1	WD_CNT_error_0	WD_CNT_refresh_1	WD_CNT_refresh_0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	WD_CNT_error_1	WD_CNT_error_0	WD_CNT_refresh_1	WD_CNT_refresh_0

Table 82. INIT WD. Description and configuration of the bits (default value in bold)

WD_CNT_error_1:0	Description	Configure the maximum value of the WD error counter
	00	**6**
	01	6
	10	4
	11	2
	Reset Condition	Power On Reset
WD_CNT_refresh_1:0	Description	Configure the maximum value of the WD refresh counter
	00	**6**
	01	4
	10	2
	11	1
	Reset Condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power On Reset

Table 82. INIT WD. Description and configuration of the bits (default value in bold) (continued)

SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK bit.
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit ERROR
	Reset condition	Power On Reset

7.3.34 Diag FS1

Table 83. DIAG FS1 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb_ext	RSTb_diag	0	FS0b_diag_1	FS0b_diag_0	0	0	0

Table 84. Diag FS1. Description and configuration of the bits (default value in bold)

RSTb_diag	Description	Report a RSTb short-circuit to HIGH
	0	**No Failure**
	1	Short-circuit HIGH
	Reset condition	Power On Reset / Read
RSTb_ext	Description	Report an external RSTb
	0	**No external RSTb**
	1	External RSTb
	Reset condition	Power On Reset / Read
FS0b_diag_1:0	Description	Report a failure on FS0b
	00	**No Failure**
	01	Short-circuit LOW / open load
	1X	Short-circuit HIGH
	Reset condition	Power On Reset / Read

7.3.35 WD counter

Table 85. WD counter register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WD_err_2	WD_err_1	WD_err_0	0	WD_refresh_2	WD_refresh_1	WD_refresh_0	0

Table 86. WD counter. Description and configuration of the bits (default value in bold)

WD_err_2:0	Description	Report the value of the watchdog error counter
	000	From 0 to 5 (6 generates a Reset and this counter is reset to 0)
	to 110	
	Reset condition	Power On Reset
WD_refresh_2:0	Description	Report the value of the watchdog refresh counter
	000	From 0 to 6 (7 generate a decrease of the RST_err_cnt and this counter is reset to 0)
	to 111	
	Reset condition	Power On Reset

7.3.36 Diag FS2

Table 87. DIAG FS2 register description

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb_err_2	RSTb_err_1	RSTb_err_0	0	IO_45_fail	IO_23_fail	IO_1_Fail	IO_01_fail

Table 88. Diag FS2. Description and configuration of the bits (default value in bold)

RSTb_err_2:0	Description	Report the value of the RSTb error counter
	000 **001** **…** 110	Error counter is set to 1 by default
	Reset condition	Power On Reset
IO_45_fail	Description	Report an error in the IO_45 protocol
	0	**No error**
	1	Error detected
	Reset condition	Power On Reset / Read

Table 88. Diag FS2. Description and configuration of the bits (default value in bold) (continued)

IO_23_fail	Description	Report an error in the FCCU protocol
	0	**No error**
	1	Error detected
	Reset condition	Power On Reset / Read
IO_1_fail	Description	Report an error in the IO_1 monitoring (external resistor string monitoring)
	0	**No error**
	1	Error detected
	Reset condition	Power On Reset
IO_01_fail	Description	Report an error in the IO_01 protocol
	0	**No error**
	1	Error detected
	Reset condition	Power On Reset / Read

8 List of interruptions and description

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. It is possible to mask some Interruption source (see Detail of register mapping).

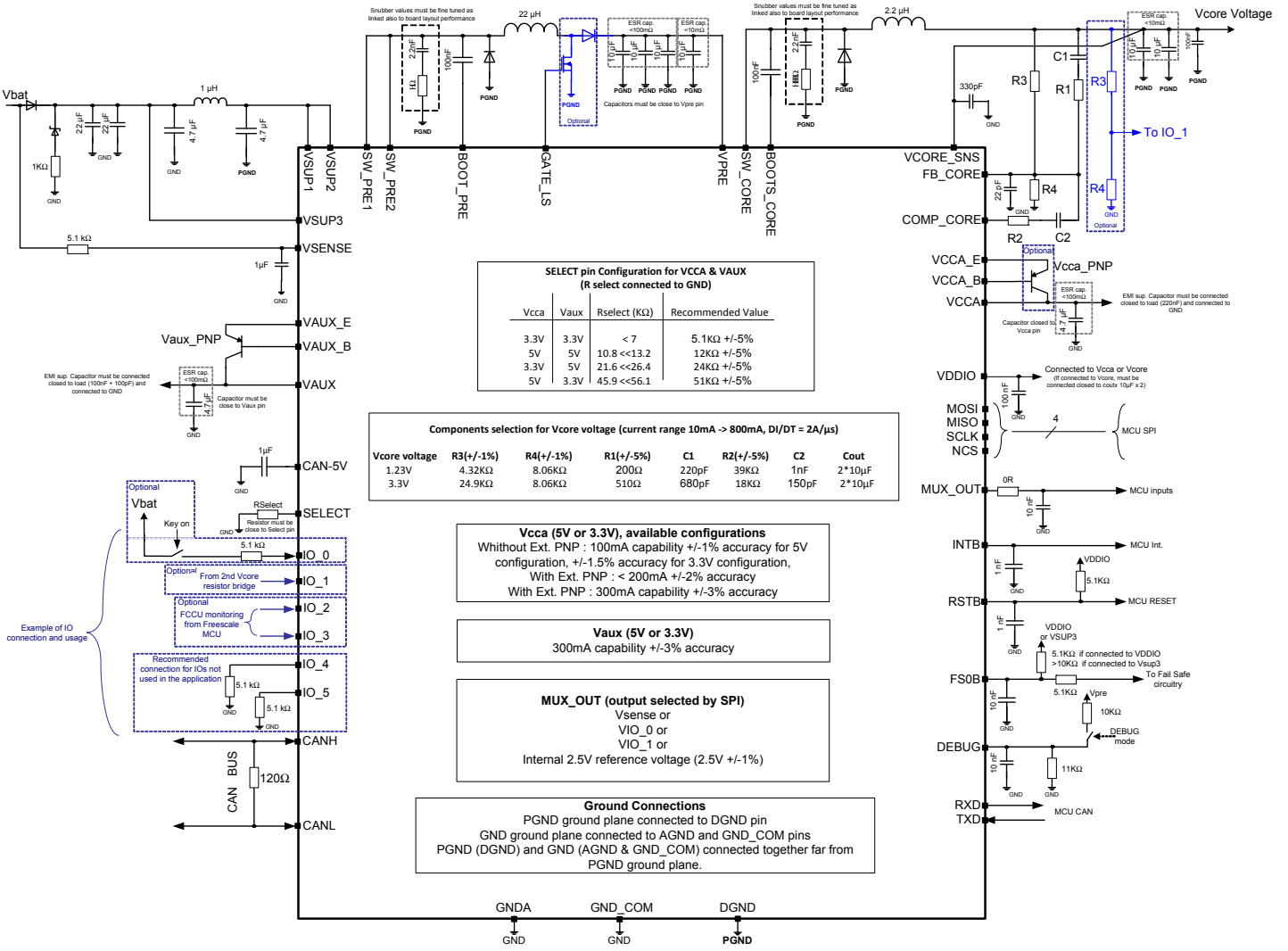
Table 89. Interruptions list

Event	Description
V_{SNS_UV}	Detection of $V_{BATTERY}$ below 8.5 V
$V_{SUP\_UV\_7}$	Detection of V_{SUP} below 7.0 V (after reverse current protection diode)
I_{LIM_PRE}	Pre-regulator Current Limitation
T_{WARN_PRE}	Temperature warning on the pass transistor
BoB	Return the running state of V_{PRE} converter (Buck or Boost mode)
V_{PRE_STATE} ($V_{PRE\_SMPS\_EN}$)	Return the activation state of V_{PRE} DC/DC converter
V_{PRE} OV	Report a V_{PRE} overvoltage detection
V_{PRE} UV	Report a V_{PRE} undervoltage detection
I_{LIM_CORE}	V_{CORE} Current limitation
T_{WARN_CORE}	Temperature warning on the pass transistor
V_{CORE_STATE} ($V_{CORE\_SMPS\_EN}$)	Return the activation state of V_{CORE} DC/DC converter
V_{CORE} OV	Report a V_{CORE} overvoltage detection
V_{CORE} UV	Report a V_{CORE} undervoltage detection
I_{LIM_CCA}	V_{CCA} Current limitation
T_{WARN_CCA}	Temperature warning on the pass transistor (Internal Pass transistor only)
TSD_{VCCA}	Temperature shutdown of the VCCA
$I_{LIM\_CCA\_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
V_{CCA} OV	Report a V_{CCA} overvoltage detection
V_{CCA} UV	Report a V_{CCA} undervoltage detection
I_{LIM_AUX}	V_{AUX} Current limitation
$I_{LIM\_AUX\_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
V_{AUX} OV	Report a V_{AUX} overvoltage detection
V_{AUX} UV	Report a V_{AUX} undervoltage detection
TSD_{VAUX}	Temperature shutdown of the VAUX
I_{LIM_CAN}	V_{CAN} Current limitation
V_{CAN} OV	Report a V_{CAN} overvoltage detection
V_{CAN} UV	Report a V_{CAN} undervoltage detection
TSD_{CAN}	Temperature shutdown on the pass transistor. Auto restart when $T_J < (TSD_{CAN} - TSD_{CAN\_HYST})$.
IO_0	Report IO_0 digital state change
IO_1	Report IO_1 digital state change
IO_2	Report IO_2 digital state change
IO_3	Report IO_3 digital state change
IO_4	Report IO_4 digital state change
IO_5	Report IO_5 digital state change
IO_0_WU	Report IO_0 WU event

Table 89. Interruptions list (continued)

IO_1_WU	Report IO_1 WU event
IO_2_WU	Report IO_2 WU event
IO_3_WU	Report IO_3 WU event
IO_4_WU	Report IO_4 WU event
IO_5_WU	Report IO_5 WU event
CAN_WU	Report a CAN wake-up event
CAN_OT	CAN overtemperature detection
RXD_recessive	CAN RXD recessive clamping detection (short-circuit to 5.0 V)
TXD_dominant	CAN TXD dominant clamping detection (short circuit to GND)
CAN_dominant	CAN bus dominant clamping detection
INT_Request	MCU request for an Interrupt pulse
SPI_err	Secured SPI communication check
SPI_CLK	Report a wrong number of CLK pulse different than 16 during the NCS low pulse in Main state machine
SPI_Req	Invalid SPI access (Wrong write or read, write to INIT registers in normal mode, wrong address)
SPI_Parity	Report a Parity error in Main state machine

9 Typical applications



Vcca	Vaux	Rselect (KΩ)	Recommended Value
3.3V	3.3V	< 7	5.1KΩ +/-5%
5V	5V	10.8 <<13.2	12KΩ +/-5%
3.3V	5V	21.6 <<26.4	24KΩ +/-5%
5V	3.3V	45.9 <<56.1	51KΩ +/-5%

Vcore voltage	R3(+/-1%)	R4(+/-1%)	R1(+/-5%)	C1	R2(+/-5%)	C2	Cout
1.23V	4.32KΩ	8.06KΩ	200Ω	220pF	39KΩ	1nF	2*10µF
3.3V	24.9KΩ	8.06KΩ	510Ω	680pF	18KΩ	150pF	2*10µF

Figure 49. FS6407/FS6408 simplified application schematic with non-inverting buck-boost configuration

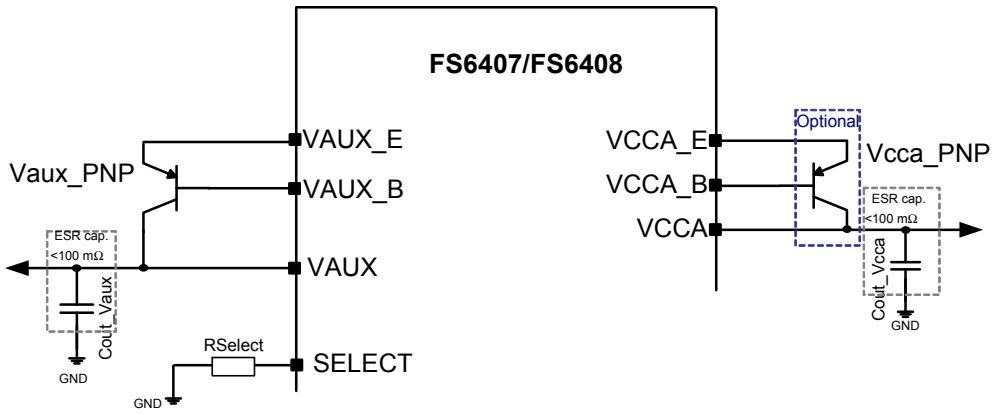


Figure 50. V_{AUX}/V_{CCA} connection

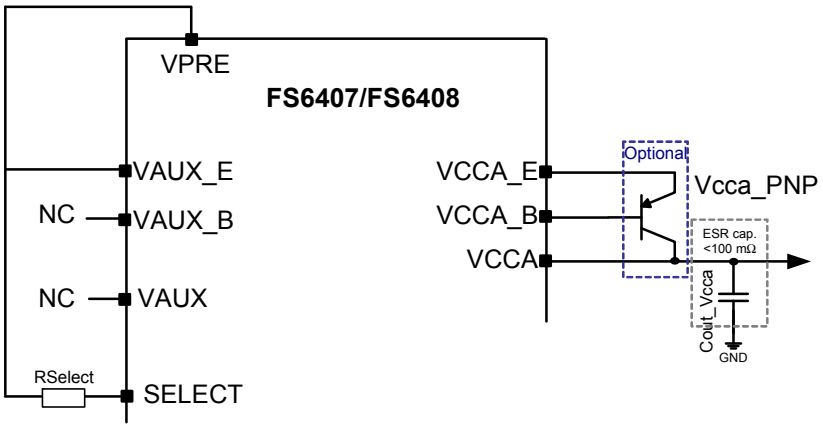


Figure 51. VCCA connection, V_{AUX} not used

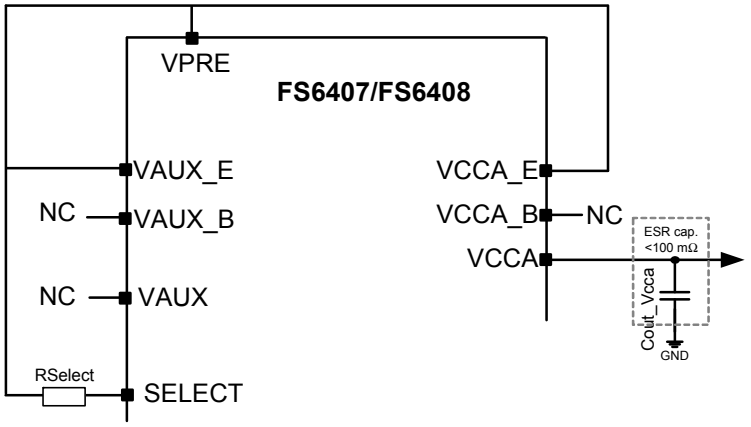


Figure 52. V_{AUX} not used, V_{CCA} configuration up to 100 mA

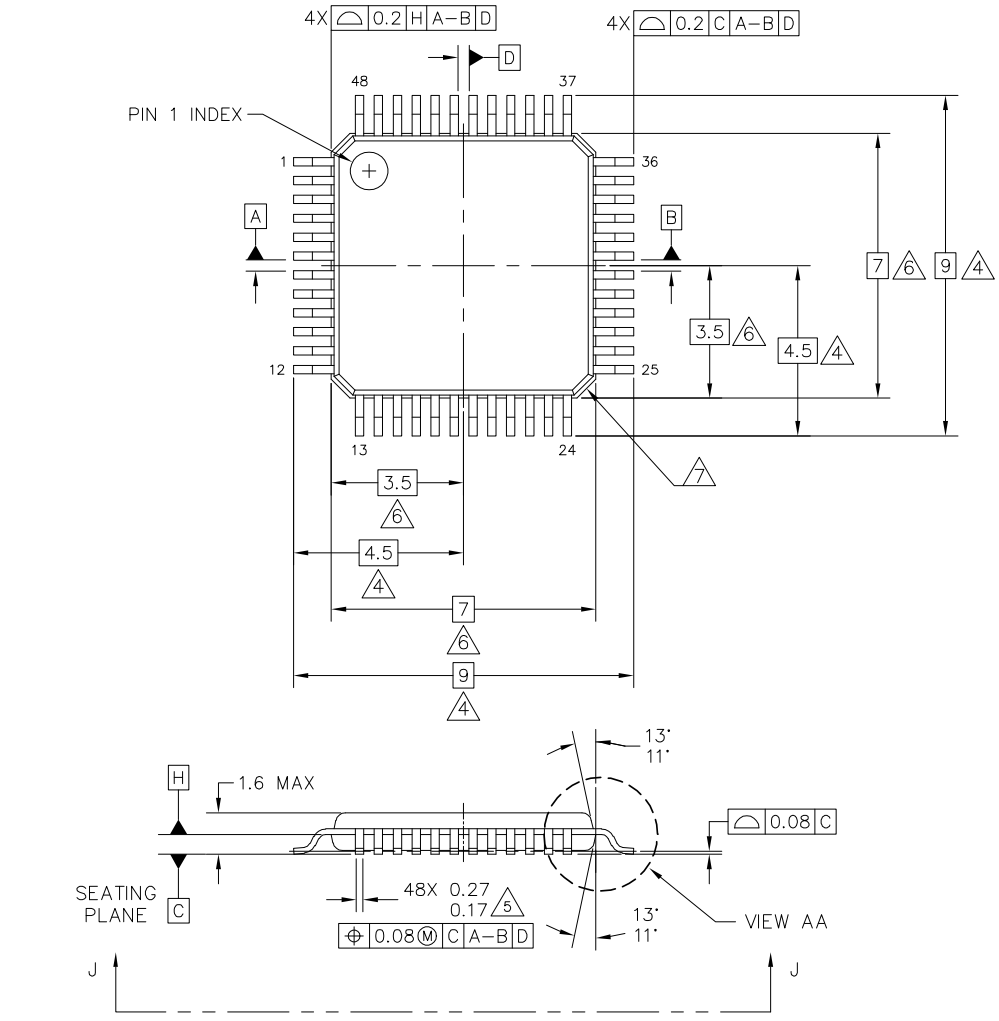
10 Packaging

10.1 Package mechanical dimensions

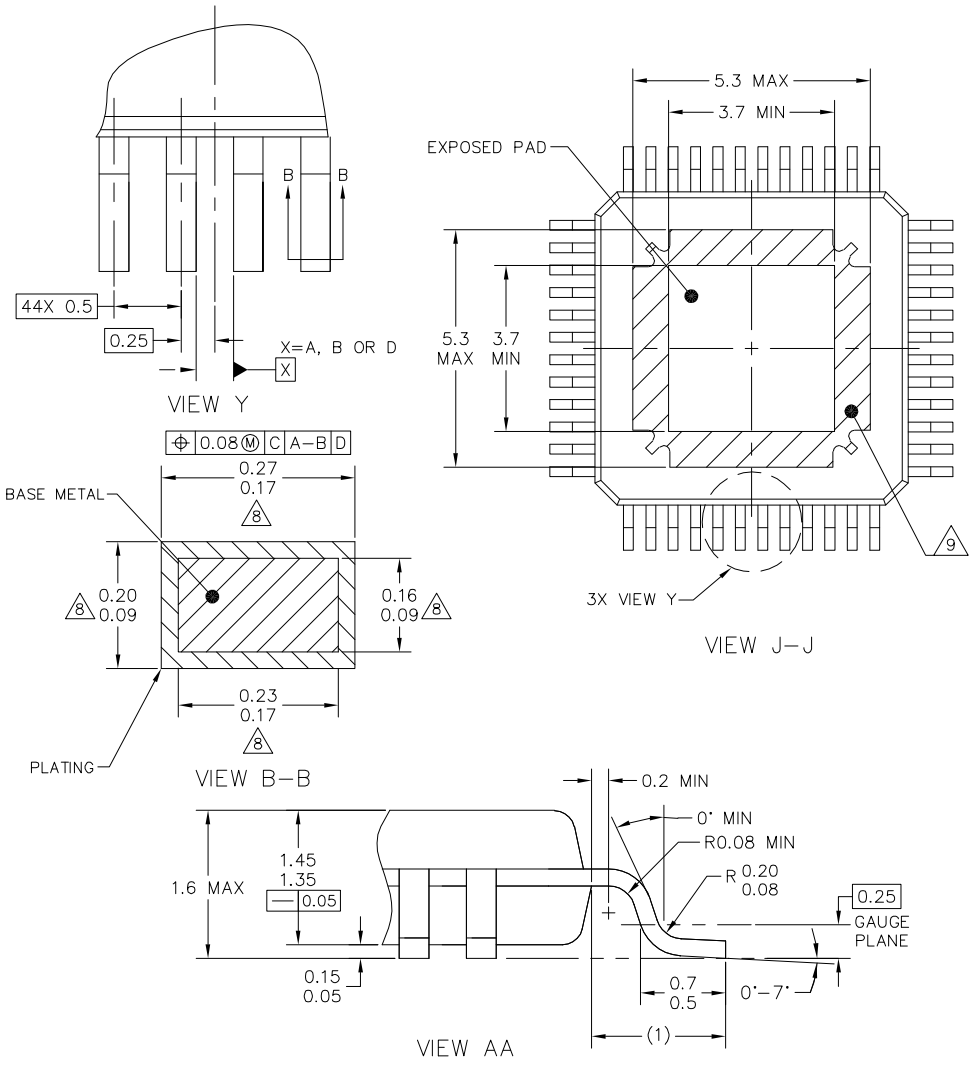
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www. NXP.com and perform a keyword search for the drawing's document number.

Table 90. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 x 7.0, 48-Pin LQFP Exposed Pad, with 0.5 mm pitch, and a 4.5 x 4.5 exposed pad	AE	98ASA00173D



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003-02	30 JUN 2011
	STANDARD: JEDEC MS-026 BBC	



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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003–02	30 JUN 2011
	STANDARD: JEDEC MS–026 BBC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.

9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A	
	CASE NUMBER: 2003-02	30 JUN 2011	
	STANDARD: JEDEC MS-026 BBC		

11 References

The following are URLs where you can obtain information on related NXP products and application solutions

Support pages	Description	URL
AN4766	MC33907_08 System Basis Chip: Recommendations for PCB layout and external components	https://www.nxp.com/webapp/Download?colCode=AN4766
AN4661	Designing the VCORE Compensation Network For The MC33907/MC33908 System Basis Chips	http://www.nxp.com/files/analog/doc/app_note/AN4661.pdf
AN4442	Integrating the MPC5643L and MC33907/08 for Safety Applications	http://www.nxp.com/files/analog/doc/app_note/AN4442.pdf
AN4388	Quad Flat Package (QFP)	http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
AN4843	Low-power Wireless Charging Using the NXP WCT1001A Controller	http://www.nxp.com/files/microcontrollers/doc/app_note/AN4843.pdf
AN5099	Integrating the MPC5744P and MC33907/08 for Safety Applications	http://www.nxp.com/files/microcontrollers/doc/app_note/AN5099.pdf
MC33907-MC33908PDTCALC	MC33907_8 Power Dissipation Tool	http://www.nxp.com/files/software_development_tools/calculators/MC33907-MC33908-PDT-CALC.xlsx
V_{CORE} Compensation Network Simulation Tool		Upon demand
MC33907_8SMUG	MC33907_8NAE, MC33907/8NAE Safety Manual	https://www.nxp.com/webapp/Download?colCode=MC33907NL-33908NLSMUG
FMEDA	MC33907_8 FMEDA	Upon demand
KIT34FS6407EVB	Evaluation Board	http://www.nxp.com/products/analog-power-management/transceivers/can-physical-interfaces/evaluation-board-mc34fs6407-safe-dc-dc-up-to-800-ma:KIT34FS6407EVB
KIT34FS6408EVB	Evaluation Board	http://www.nxp.com/products/analog-power-management/transceivers/can-physical-interfaces/evaluation-board-mc34fs6407-safe-dc-dc-up-to-800-ma:KIT34FS6408EVB
KIT33908MBEVBE	Evaluation Mother Board (EVM)	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908MBEVBE
KITMPC5643DBEVM	Evaluation Daughter Board (Qorivva MPC5643L)	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KITMPC5643DBEVM
KITMPC5744DBEVM	Evaluation daughter board - MPC5744P, 32-bit Microcontroller	http://www.nxp.com/products/power-architecture-processors/mpc5xxx-5xxx-32-bit-mcus/mpc57xx-mcus/evaluation-daughter-board- NXP-mpc5744p-32-bit-microcontroller:KITMPC5744DBEVM
MC34FS6407 Product Summary Page		http://www.nxp.com/products/analog-power-management/transceivers/can-physical-interfaces/safe-sbc-with-buck-and-boost-dc-dc-up-to-800-ma-on-vcore:MC34FS6407
MC34FS6408 Product Summary Page		http://www.nxp.com/products/analog-power-management/transceivers/can-physical-interfaces/safe-sbc-with-buck-and-boost-dc-dc-up-to-800-ma-on-vcore:MC34FS6408
Analog Home Page		http://www.nxp.com/analog

12 Revision history

Revision	Date	Description of changes
1.0	10/2014	• Initial release
2.0	3/2015	• Overall description improvement
3.0	9/2015	• Changed PC parts to MC in the Orderable Part Variations table • Changed document classification to Advance Information • Changed max. ambient temperature to 125 °C • Updated the min. value for t_{3PTO1} in Table 5 • Updated the min. value for t_{3PTO2} in Table 5 • Updated the min. and typ. value for f_{SW_PRE} in Table 5 • Updated the max. value for $t_{PRE\_UV\_4p3}$ in Table 5 • Updated the min. and max. value for t_{PRE_TSD} in Table 5 • Updated the values for f_{SW_CORE} in Table 5 • Updated the min. and max. value for t_{CORE_TSD} in Table 5 • Updated the min. and max. value for t_{CCA_TSD} in Table 5 • Updated the min. and max. value for t_{AUX_TSD} in Table 5 • Updated the max. value for t_{CAN_TSD} in Table 5 • Updated links in References table
	9/2015	• Updated Table 56
	7/2016	• Updated to NXP document form and style

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